

## N-Channel 30-V (D-S) MOSFET

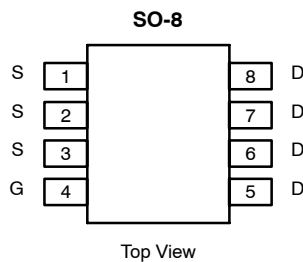
PRODUCT SUMMARY		
$V_{DS}$ (V)	$r_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)
30	0.0135 @ $V_{GS} = 10$ V	10
	0.020 @ $V_{GS} = 4.5$ V	8

### FEATURES

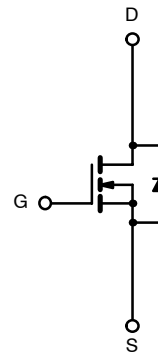
- TrenchFET® Power MOSFET
- 100%  $R_g$  Tested

### APPLICATIONS

- Battery Switch



Ordering Information: Si4410BDY  
Si4410BDY-T1 (with Tape and Reel)



ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)					
Parameter	Symbol	10 secs	Steady State	Unit	
Drain-Source Voltage	$V_{DS}$	30		V	
Gate-Source Voltage	$V_{GS}$	$\pm 20$			
Continuous Drain Current ( $T_J = 150^\circ\text{C}$ ) <sup>a</sup>	$I_D$	$T_A = 25^\circ\text{C}$	10	7.5	A
		$T_A = 70^\circ\text{C}$	8	6	
Pulsed Drain Current (10 $\mu\text{s}$ Pulse Width)	$I_{DM}$	50			
Continuous Source Current (Diode Conduction) <sup>a</sup>	$I_S$	2.3	1.26		
Maximum Power Dissipation <sup>a</sup>	$P_D$	$T_A = 25^\circ\text{C}$	2.5	1.4	W
		$T_A = 70^\circ\text{C}$	1.6	0.9	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to 150		$^\circ\text{C}$	

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient <sup>a</sup>	$R_{thJA}$	$t \leq 10$ sec	40	50	$^\circ\text{C}/\text{W}$
		Steady State	70	90	
Maximum Junction-to-Foot (Drain)	$R_{thJF}$	25	30		

Notes

a. Surface Mounted on 1" x 1" FR4 Board.

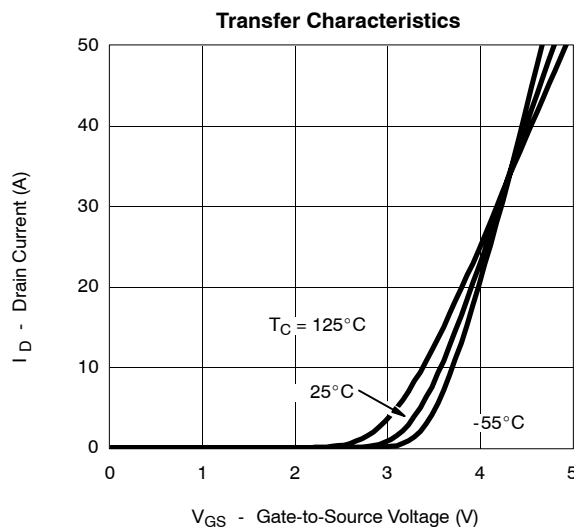
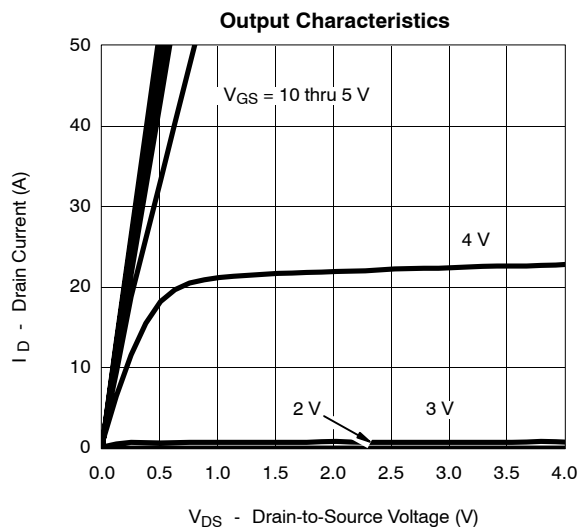
## SPECIFICATIONS (T<sub>J</sub> = 25 °C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>Static</b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	1.0		3.0	V
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V			1	μA
		V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C			5	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≥ 5 V, V <sub>GS</sub> = 10 V	20			A
Drain-Source On-State Resistance <sup>a</sup>	r <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 10 A		0.011	0.0135	Ω
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 5 A		0.0165	0.020	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 10 A		25		S
Diode Forward Voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>S</sub> = 2.3 A, V <sub>GS</sub> = 0 V		0.76	1.1	V
<b>Dynamic<sup>b</sup></b>						
Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 5 V, I <sub>D</sub> = 10 A		13	20	nC
Total Gate Charge	Q <sub>gt</sub>	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 10 A		25	40	
Gate-Source Charge	Q <sub>gs</sub>			5.5		
Gate-Drain Charge	Q <sub>gd</sub>			3.7		
Gate Resistance	R <sub>g</sub>	f = 1 MHz	0.5	1.6	2.7	Ω
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 25 V, R <sub>L</sub> = 25 Ω I <sub>D</sub> ≅ 1 A, V <sub>GEN</sub> = 10 V, R <sub>G</sub> = 6 Ω		10	15	ns
Rise Time	t <sub>r</sub>			10	15	
Turn-Off Delay Time	t <sub>d(off)</sub>			40	60	
Fall Time	t <sub>f</sub>			15	25	
Source-Drain Reverse Recovery Time	t <sub>rr</sub>		I <sub>F</sub> = 2.3 A, di/dt = 100 A/μs		35	

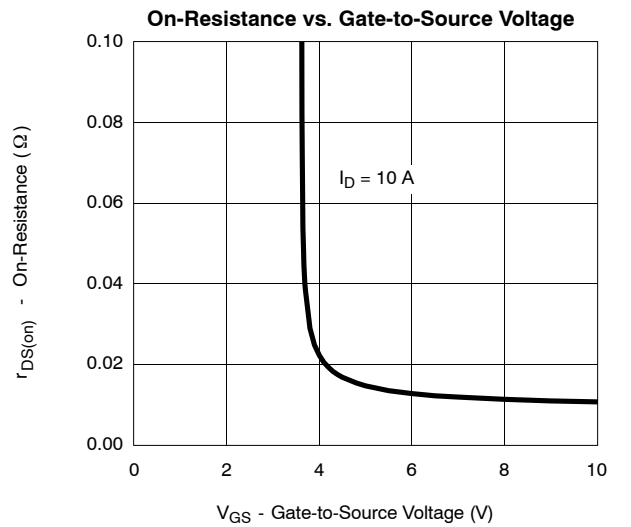
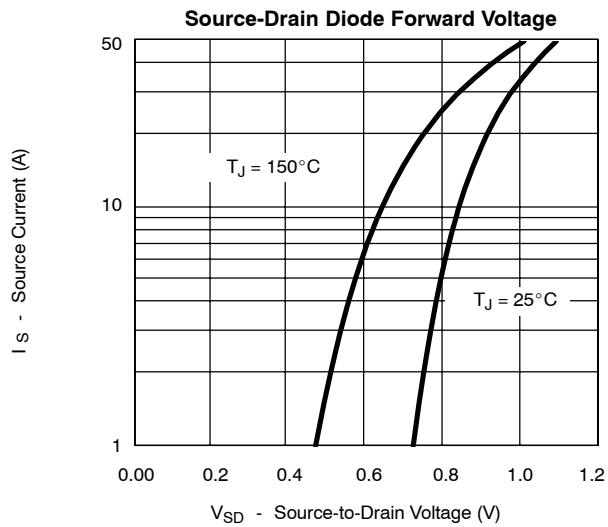
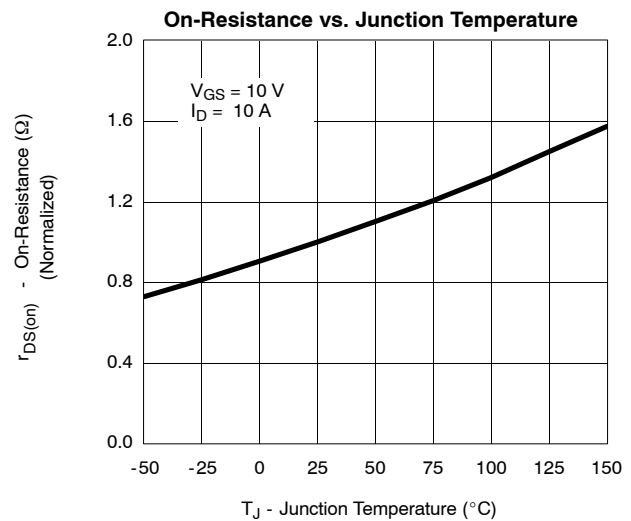
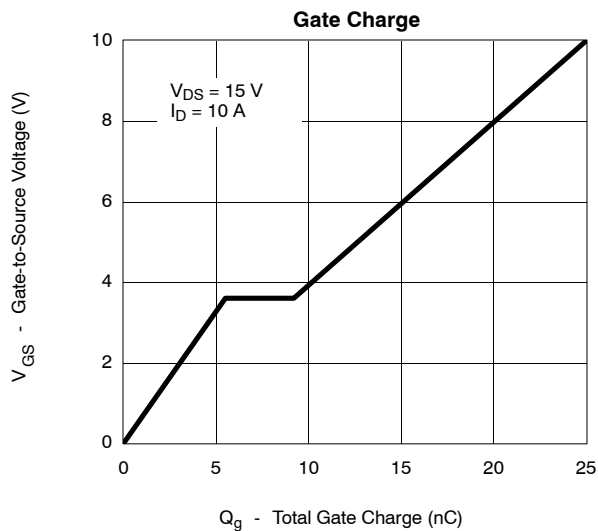
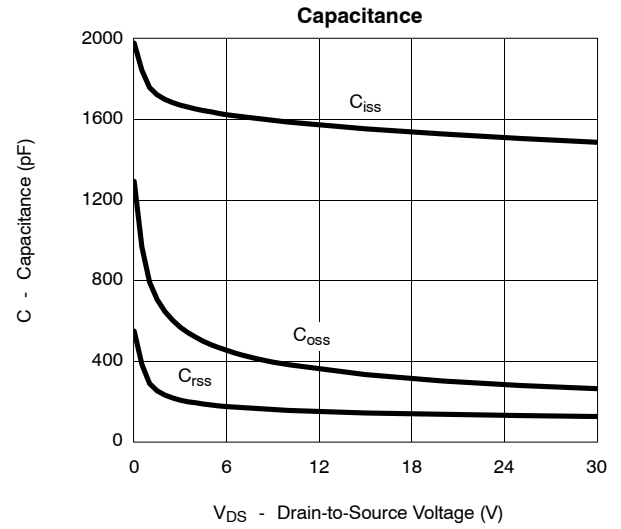
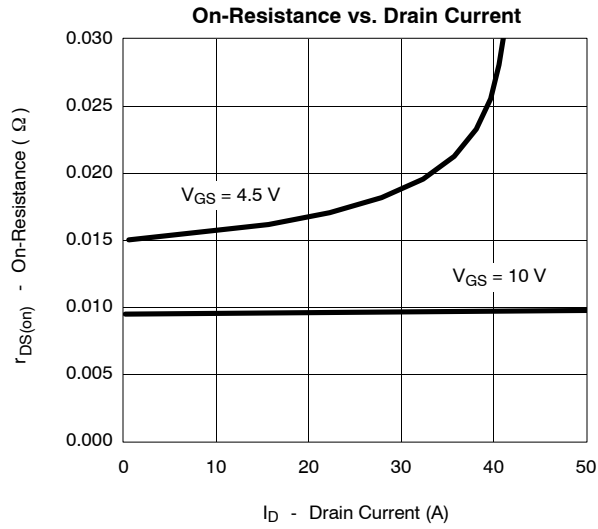
**Notes**

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.

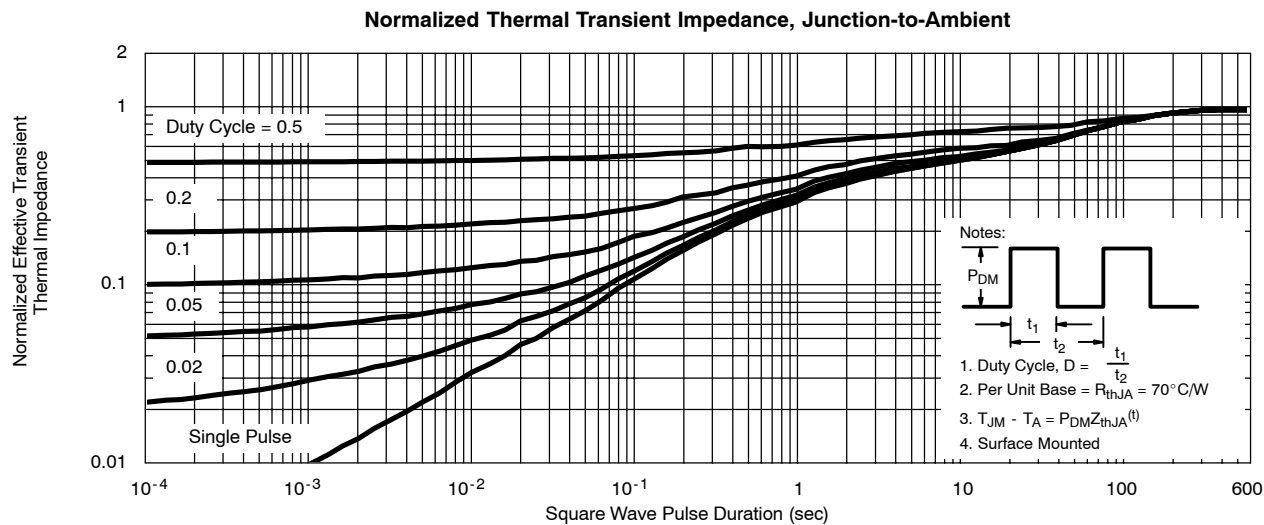
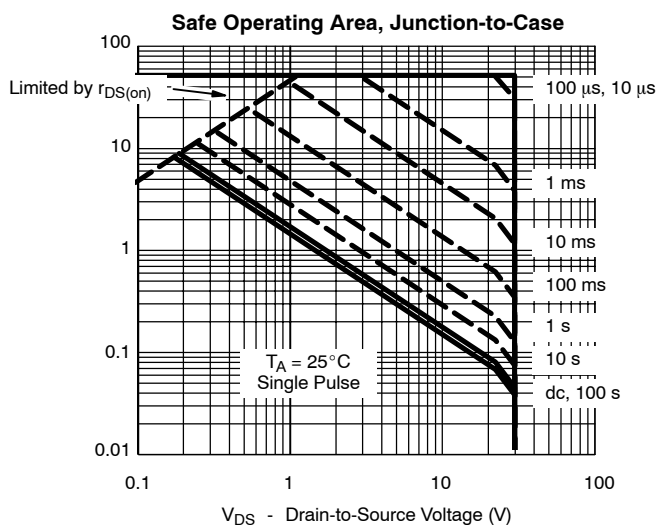
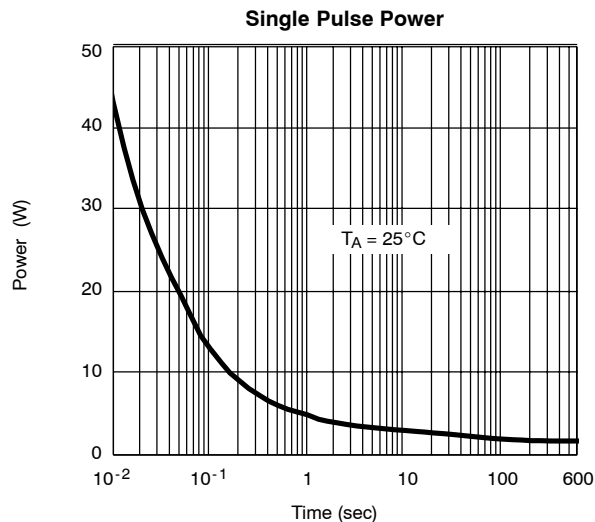
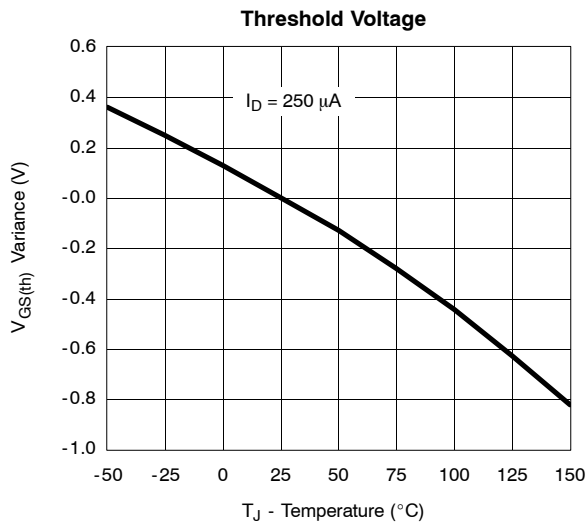
## TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)



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