

## Dual N-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY			
	V <sub>DS</sub> (V)	r <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A)
Channel-1	30	0.019 at V <sub>GS</sub> = 10 V	8.0
		0.026 at V <sub>GS</sub> = 4.5 V	6.9
Channel-2		0.035 at V <sub>GS</sub> = 10 V	6.0
		0.048 at V <sub>GS</sub> = 4.5 V	5.0

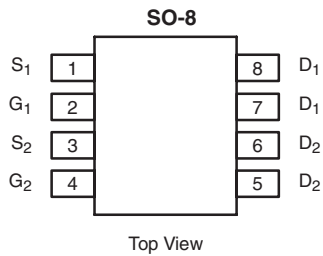
### FEATURES

- TrenchFET<sup>®</sup> Power MOSFET
- 100 % R<sub>g</sub> Tested

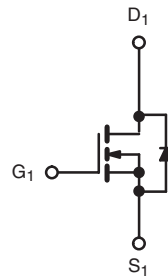


### APPLICATIONS

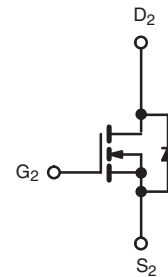
- Logic DC/DC
- Notebook PC



Ordering Information: Si4974DY-T1-E3 (Lead (Pb)-free)



N-Channel 1  
MOSFET



N-Channel 2  
MOSFET

ABSOLUTE MAXIMUM RATINGS T <sub>A</sub> = 25 °C, unless otherwise noted							
Parameter	Symbol	Channel-1		Channel-2		Unit	
		10 sec	Steady State	10 sec	Steady State		
Drain-Source Voltage	V <sub>DS</sub>	30				V	
Gate-Source Voltage	V <sub>GS</sub>	± 20					
Continuous Drain Current (T <sub>J</sub> = 150 °C) <sup>a</sup>	I <sub>D</sub>	T <sub>A</sub> = 25 °C	8.0	6.0	6.0	4.4	A
		T <sub>A</sub> = 70 °C	6.5	4.7	4.8	3.5	
Pulsed Drain Current	I <sub>DM</sub>	40		30			
Continuous Source Current (Diode Conduction) <sup>a</sup>	I <sub>S</sub>	1.8	1.0	1.8	1.0		
Single Pulse Avalanche Current	L = 0.1 mH	I <sub>AS</sub>	15		7		
Avalanche Energy		E <sub>AS</sub>	11		2.45		mJ
Maximum Power Dissipation <sup>a</sup>	T <sub>A</sub> = 25 °C	P <sub>D</sub>	2	1.1	2	1.1	W
			T <sub>A</sub> = 70 °C	1.3	0.7	1.3	
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150				°C	

THERMAL RESISTANCE RATINGS							
Parameter	Symbol	Channel-1		Channel-2		Unit	
		Typ	Max	Typ	Max		
Maximum Junction-to-Ambient <sup>a</sup>	R <sub>thJA</sub>	t ≤ 10 sec	50	62.5	52	62.5	°C/W
		Steady State	90	110	91	110	
Maximum Junction-to-Foot (Drain)	R <sub>thJF</sub>	30	40	32	40		

Notes:

a. Surface Mounted on 1" x 1" FR4 Board.

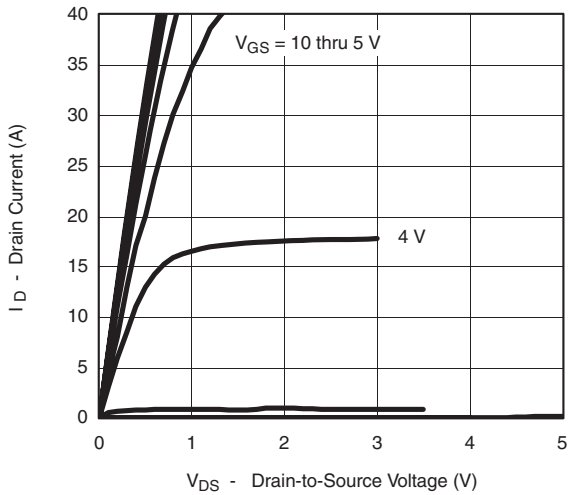
MOSFET SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted							
Parameter	Symbol	Test Conditions	Min	Typ <sup>a</sup>	Max	Unit	
<b>Static</b>							
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	Ch-1	1.0		3.0	V
			Ch-2	1.0		3.0	
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 20\text{ V}$	Ch-1			$\pm 100$	nA
			Ch-2			$\pm 100$	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 30\text{ V}$ , $V_{GS} = 0\text{ V}$	Ch-1			1	$\mu\text{A}$
			Ch-2			1	
		$V_{DS} = 30\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_J = 85\text{ }^\circ\text{C}$	Ch-1			15	
			Ch-2			15	
On-State Drain Current <sup>b</sup>	$I_{D(on)}$	$V_{DS} = 5\text{ V}$ , $V_{GS} = 10\text{ V}$	Ch-1	20			A
			Ch-2	20			
Drain-Source On-State Resistance <sup>b</sup>	$r_{DS(on)}$	$V_{GS} = 10\text{ V}$ , $I_D = 8.0\text{ A}$	Ch-1		0.016	0.019	$\Omega$
			Ch-2		0.029	0.035	
		$V_{GS} = 4.5\text{ V}$ , $I_D = 6.0\text{ A}$	Ch-1		0.0215	0.026	
			Ch-2		0.040	0.048	
Forward Transconductance <sup>b</sup>	$g_{fs}$	$V_{DS} = 15\text{ V}$ , $I_D = 8.0\text{ A}$	Ch-1		19		S
			Ch-2		13		
Diode Forward Voltage <sup>b</sup>	$V_{SD}$	$I_S = 1.8\text{ A}$ , $V_{GS} = 0\text{ V}$	Ch-1		0.8	1.1	V
			Ch-2		0.8	1.1	
<b>Dynamic<sup>a</sup></b>							
Total Gate Charge	$Q_g$	Channel-1 $V_{DS} = 15\text{ V}$ , $V_{GS} = 4.5\text{ V}$ , $I_D = 8.0\text{ A}$	Ch-1		7.0	11	nC
			Ch-2		3.3	5	
Gate-Source Charge	$Q_{gs}$	Channel-2 $V_{DS} = 15\text{ V}$ , $V_{GS} = 4.5\text{ V}$ , $I_D = 6.0\text{ A}$	Ch-1		2.6		
			Ch-2		1.2		
Gate-Drain Charge	$Q_{gd}$	Channel-1 $V_{DS} = 15\text{ V}$ , $V_{GS} = 4.5\text{ V}$ , $I_D = 6.0\text{ A}$	Ch-1		3.0		
			Ch-2		1.5		
Gate Resistance	$R_g$	Channel-2 $V_{DD} = 15\text{ V}$ , $R_L = 15\text{ }\Omega$ $I_D \equiv 1\text{ A}$ , $V_{GEN} = 10\text{ V}$ , $R_G = 6\text{ }\Omega$	Ch-1	0.8	1.5	2.3	$\Omega$
			Ch-2	0.9	1.95	2.9	
Turn-On Delay Time	$t_{d(on)}$	Channel-1 $V_{DD} = 15\text{ V}$ , $R_L = 15\text{ }\Omega$ $I_D \equiv 1\text{ A}$ , $V_{GEN} = 10\text{ V}$ , $R_G = 6\text{ }\Omega$	Ch-1		8	15	ns
			Ch-2		6	10	
Rise Time	$t_r$	Channel-2 $V_{DD} = 15\text{ V}$ , $R_L = 15\text{ }\Omega$ $I_D \equiv 1\text{ A}$ , $V_{GEN} = 10\text{ V}$ , $R_G = 6\text{ }\Omega$	Ch-1		12	20	
			Ch-2		11	18	
Turn-Off Delay Time	$t_{d(off)}$	Channel-1 $V_{DD} = 15\text{ V}$ , $R_L = 15\text{ }\Omega$ $I_D \equiv 1\text{ A}$ , $V_{GEN} = 10\text{ V}$ , $R_G = 6\text{ }\Omega$	Ch-1		22	35	
			Ch-2		15	25	
Fall Time	$t_f$	Channel-2 $V_{DD} = 15\text{ V}$ , $R_L = 15\text{ }\Omega$ $I_D \equiv 1\text{ A}$ , $V_{GEN} = 10\text{ V}$ , $R_G = 6\text{ }\Omega$	Ch-1		6	10	
			Ch-2		6	10	
Source-Drain Reverse Recovery Time	$t_{rr}$	$I_F = 1.8\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$	Ch-1		20	40	
			Ch-2		15	30	

## Notes:

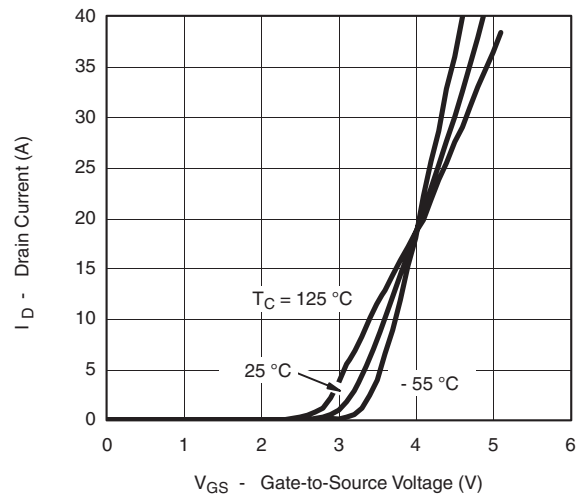
- a. Guaranteed by design, not subject to production testing.  
b. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

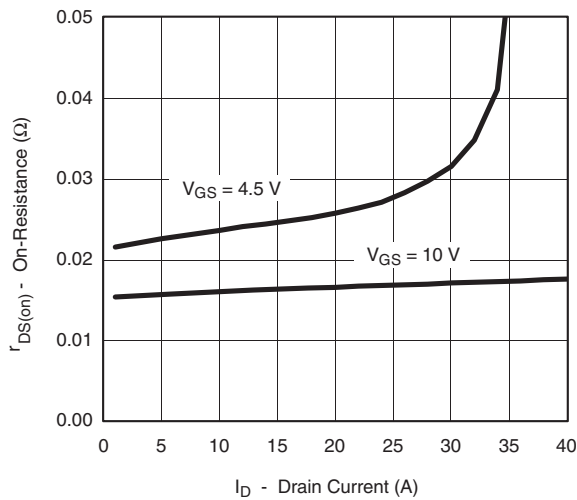
## CHANNEL-1 TYPICAL CHARACTERISTICS 25 °C unless noted



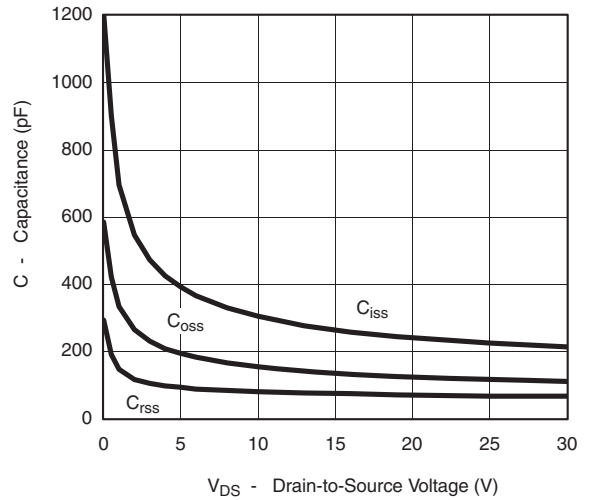
**Output Characteristics**



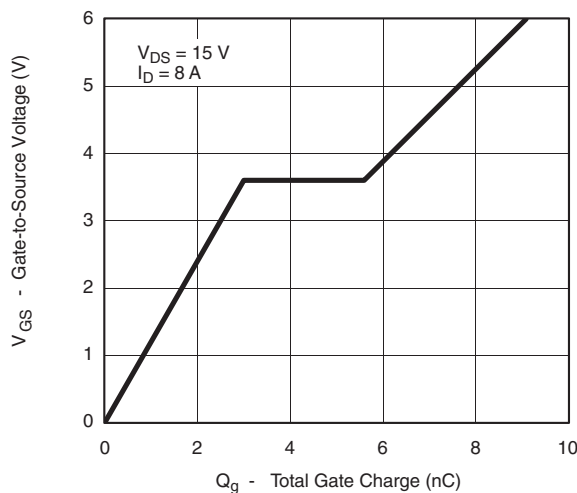
**Transfer Characteristics**



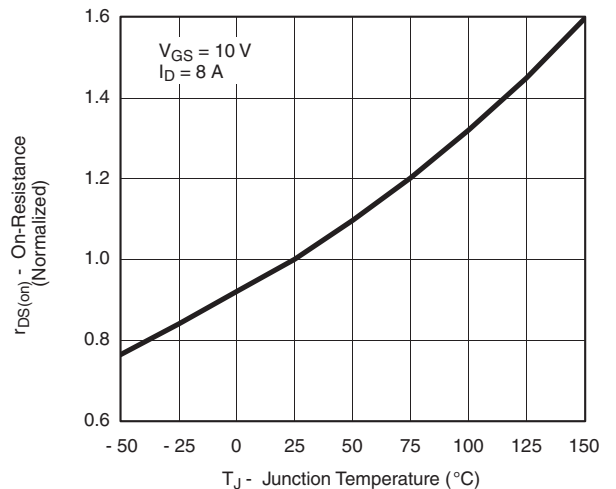
**On-Resistance vs. Drain Current**



**Capacitance**

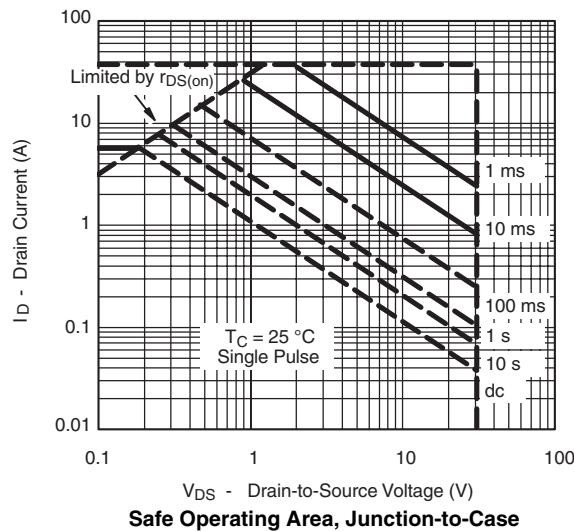
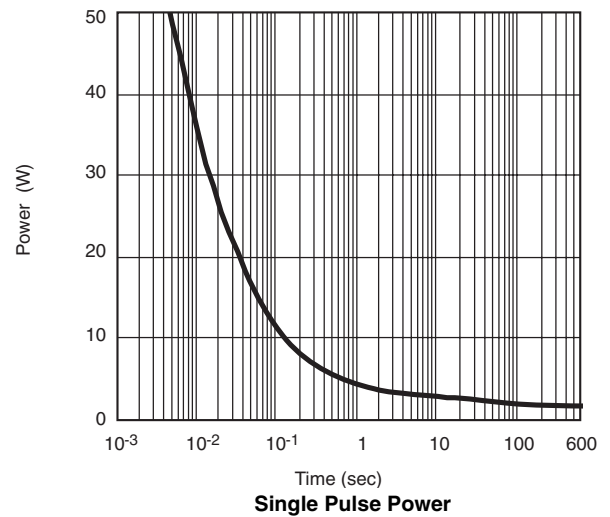
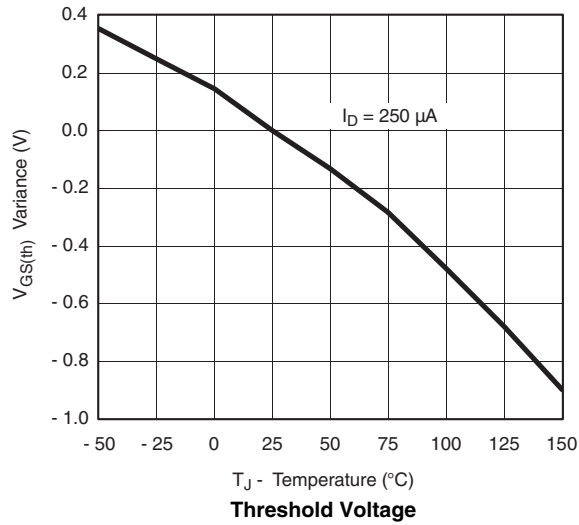
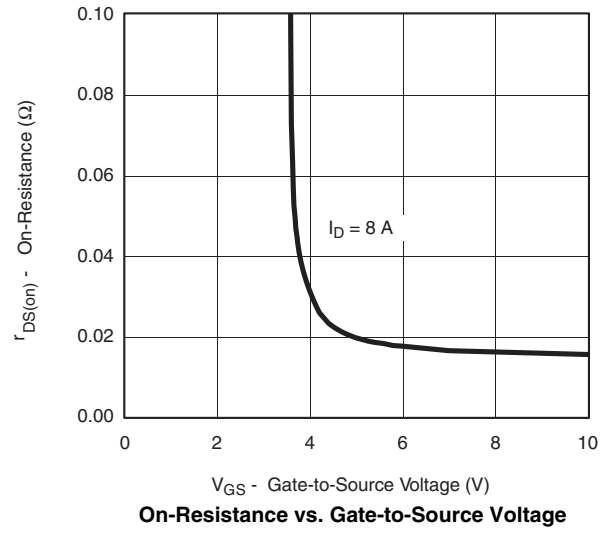
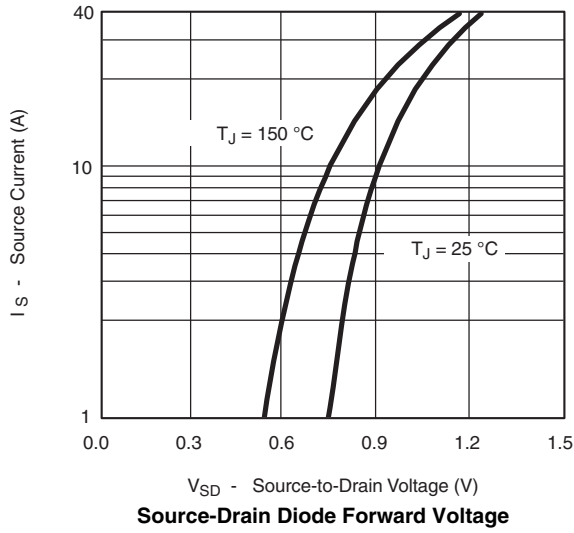


**Gate Charge**

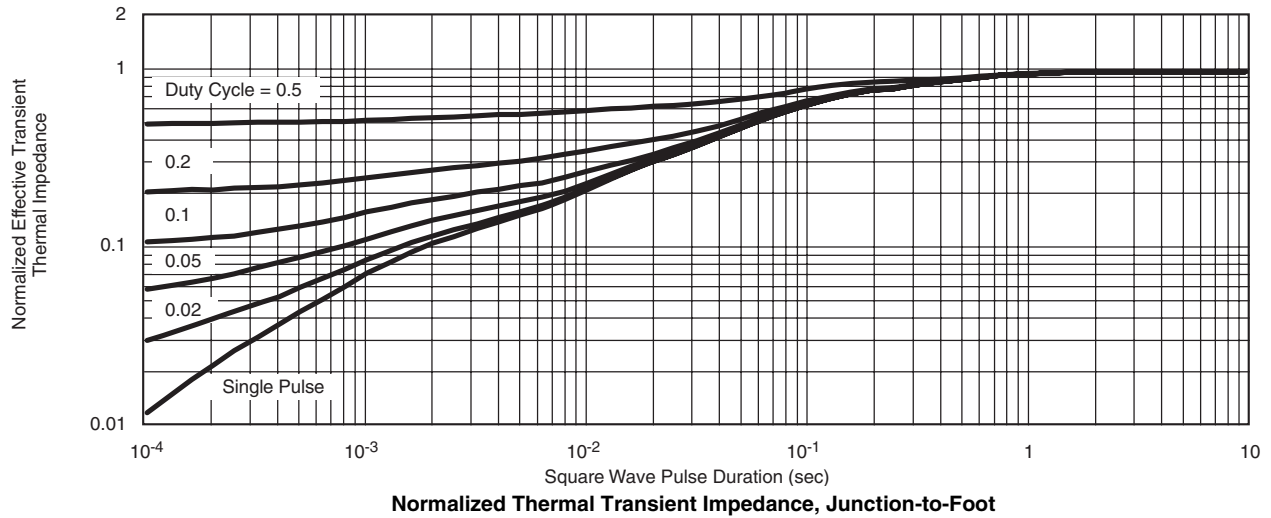
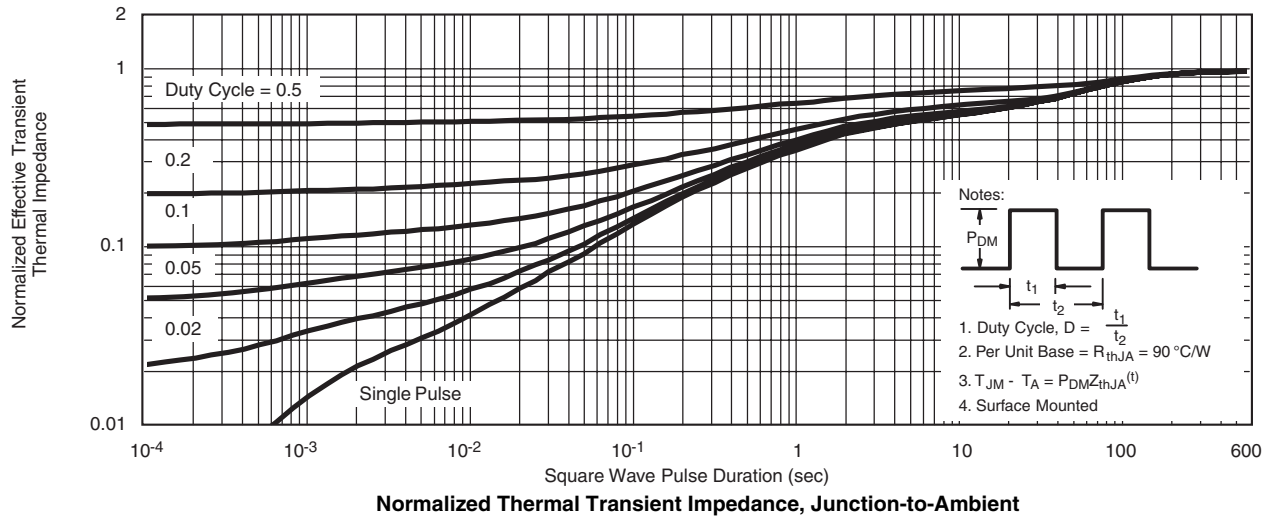


**On-Resistance vs. Junction Temperature**

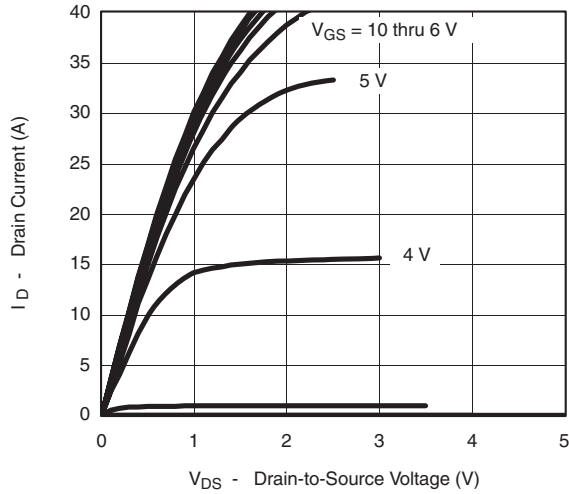
## CHANNEL-1 TYPICAL CHARACTERISTICS 25 °C unless noted



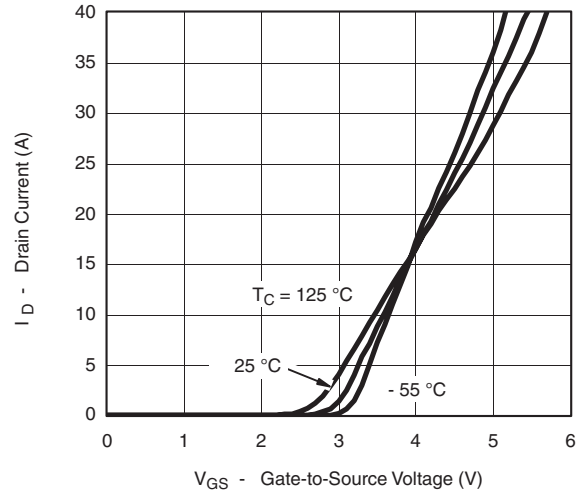
**CHANNEL-1 TYPICAL CHARACTERISTICS** 25 °C unless noted



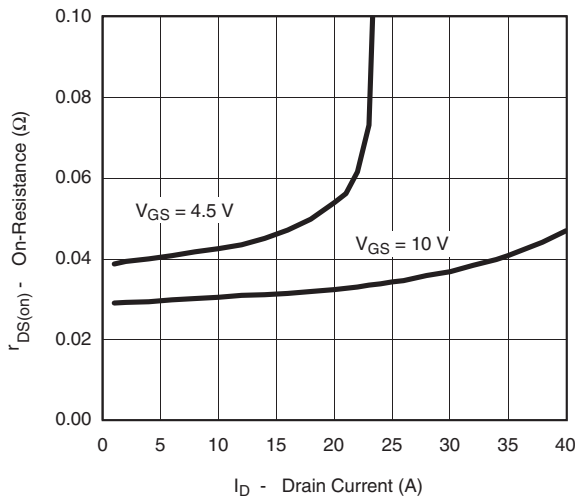
## CHANNEL-2 TYPICAL CHARACTERISTICS 25 °C unless noted



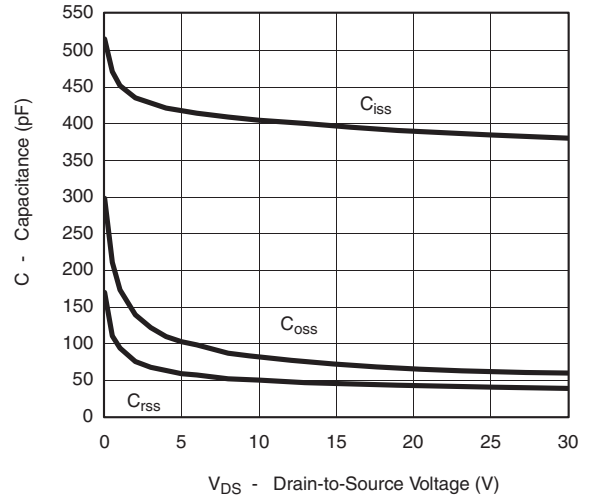
**Output Characteristics**



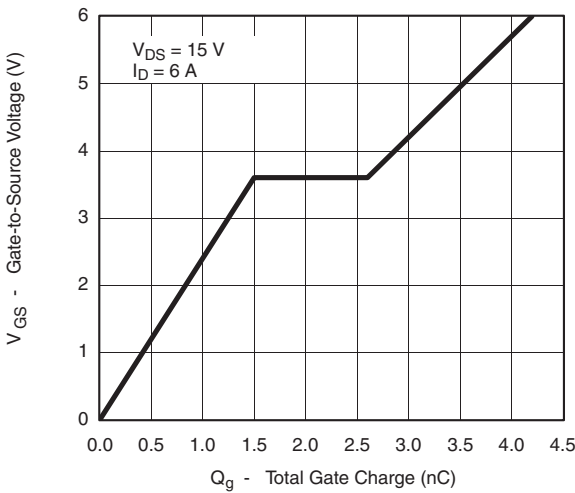
**Transfer Characteristics**



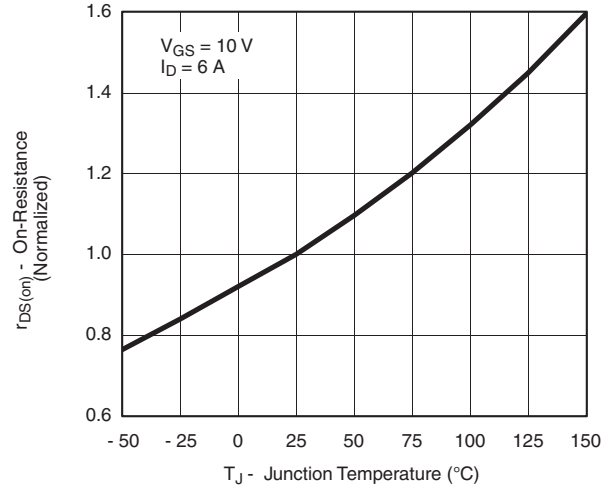
**On-Resistance vs. Drain Current**



**Capacitance**

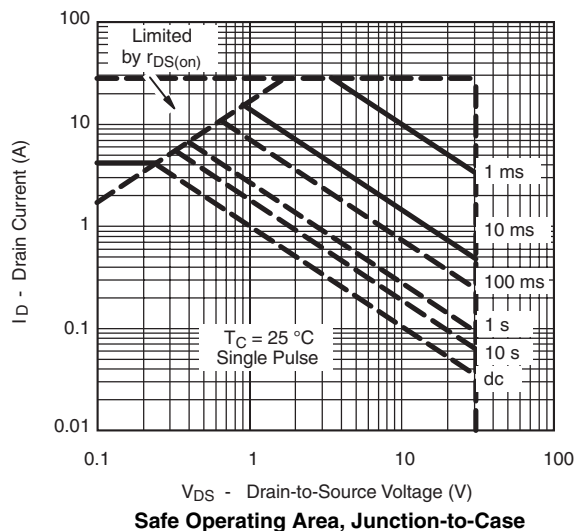
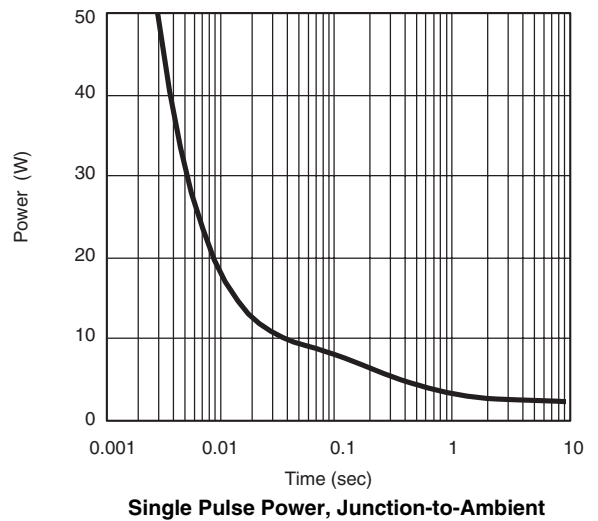
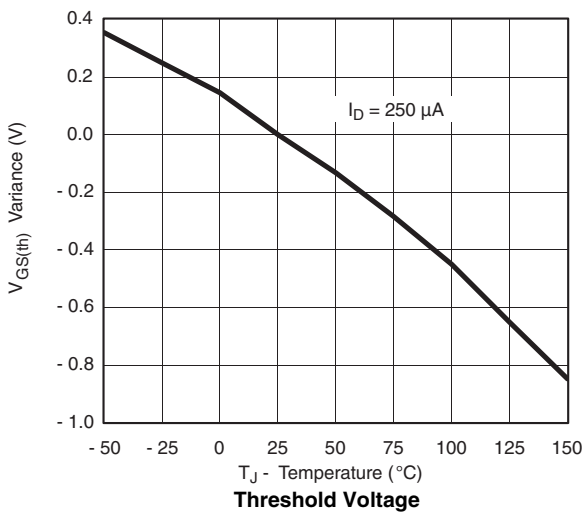
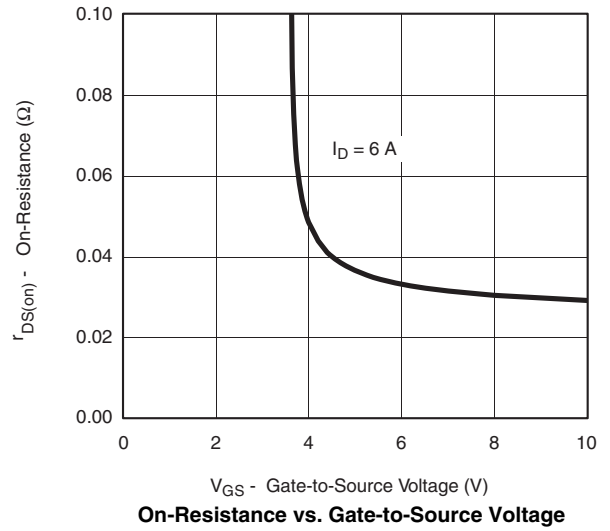
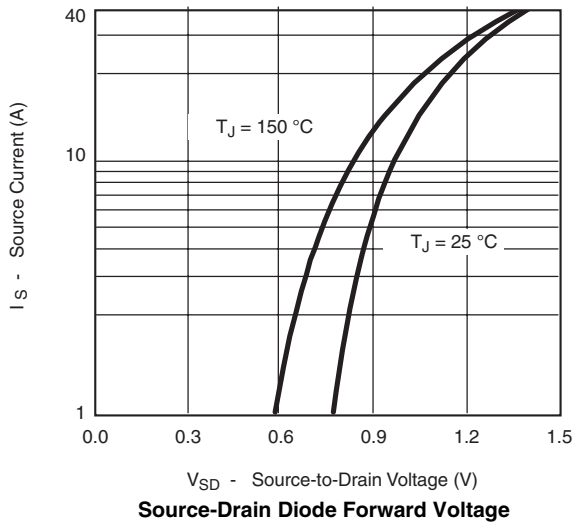


**Gate Charge**

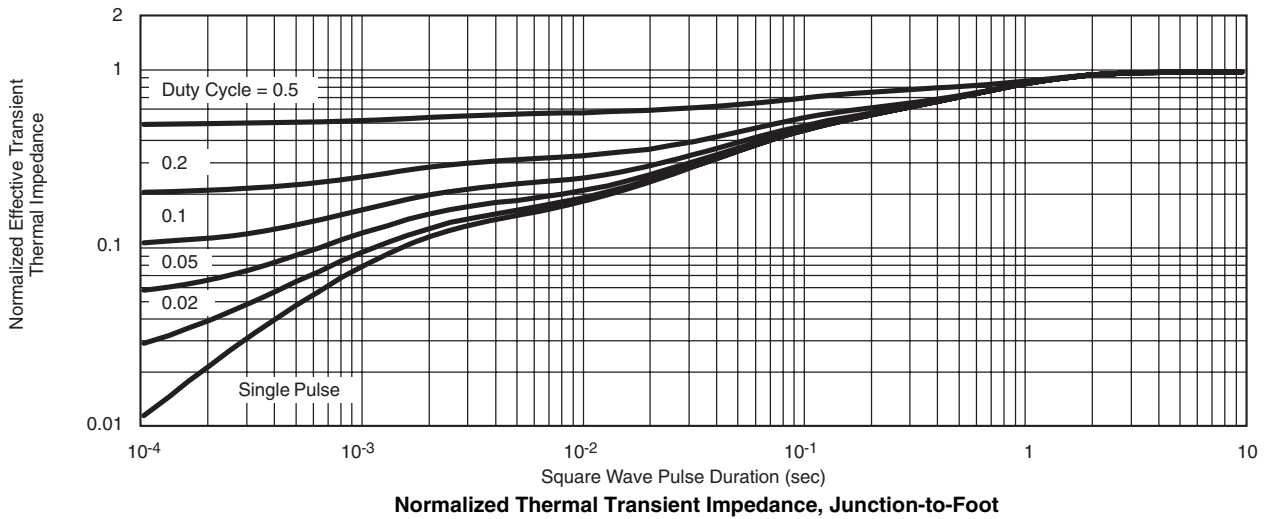
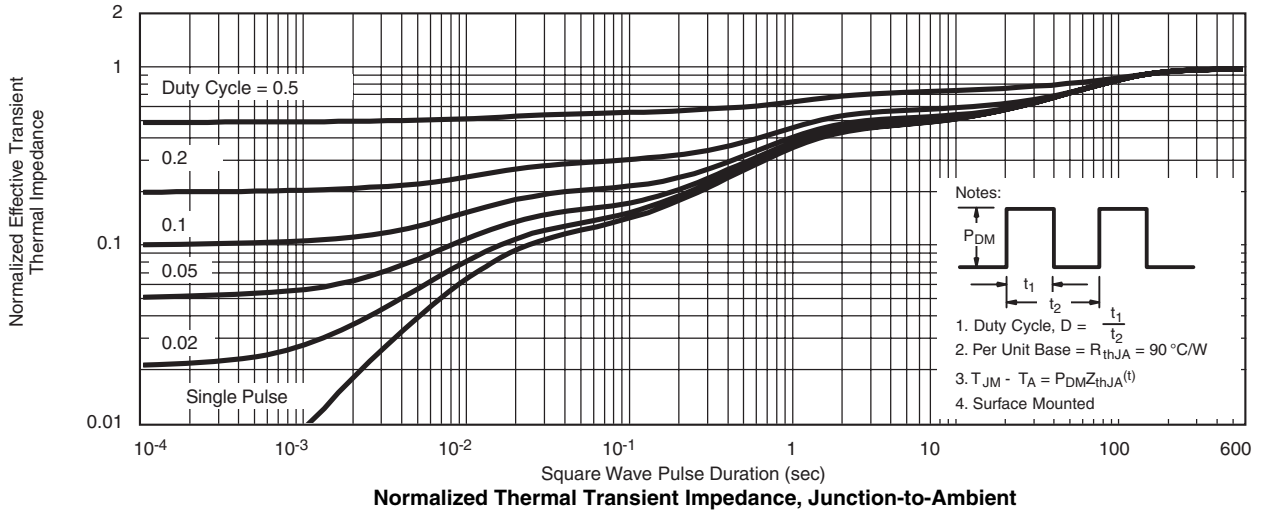


**On-Resistance vs. Junction Temperature**

**CHANNEL-2 TYPICAL CHARACTERISTICS** 25 °C unless noted



**CHANNEL-2 TYPICAL CHARACTERISTICS** 25 °C unless noted



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