

N-Channel 100-V (D-S) MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A) ^d	Q_g (Typ)
100	0.063 at $V_{GS} = 10$ V	6.8	9 nC
	0.084 at $V_{GS} = 6$ V	5.8	

FEATURES

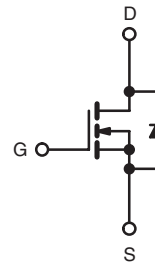
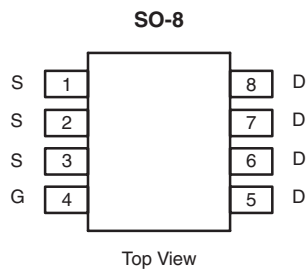
- TrenchFET[®] Power MOSFET
- 100 % UIS Tested



RoHS
COMPLIANT

APPLICATIONS

- High Frequency Boost Converter
- LED Backlight for LCD TV



Ordering Information: Si4100DY-T1-E3 (Lead (Pb)-free)

ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted				
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V_{DS}	100	V	
Gate-Source Voltage	V_{GS}	± 20		
Continuous Drain Current ($T_J = 150$ °C)	I_D	$T_C = 25$ °C	6.8	A
		$T_C = 70$ °C	5.4	
		$T_A = 25$ °C	4.4 ^{a, b}	
		$T_A = 70$ °C	3.5 ^{a, b}	
Pulsed Drain Current	I_{DM}	20		
Continuous Source-Drain Diode Current	I_S	$T_C = 25$ °C	5	
		$T_A = 25$ °C	2.1 ^{a, b}	
Single Avalanche Current	I_{AS}	L = 0.1 mH	19	mJ
Single Avalanche Energy			E_{AS}	
Maximum Power Dissipation	P_D	$T_C = 25$ °C	6	W
		$T_C = 70$ °C	3.8	
		$T_A = 25$ °C	2.5 ^{a, b}	
		$T_A = 70$ °C	1.6 ^{a, b}	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	°C	

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^{b, c}	R_{thJA}	37	50	°C/W	
Maximum Junction-to-Foot (Drain)	R_{thJF}	17	21		

Notes:

- Surface Mounted on 1" x 1" FR4 board.
- $t = 10$ s.
- Maximum under Steady State conditions is 85 °C/W.
- $T_C = 25$ °C.



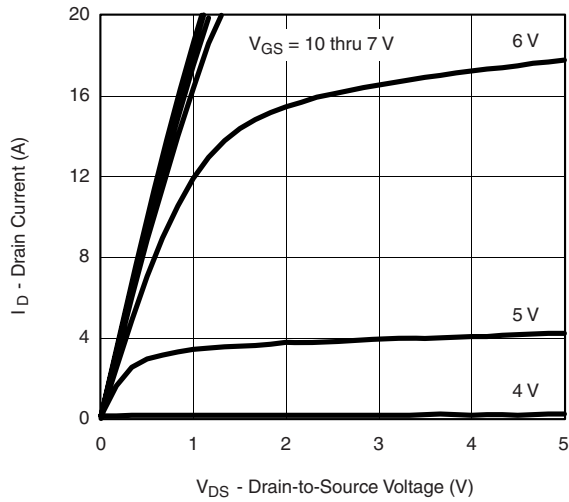
SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	100			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$		120		mV/ $^\circ\text{C}$
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			- 9		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2		4.5	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	20			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 4.4\text{ A}$		0.051	0.063	Ω
		$V_{GS} = 6\text{ V}, I_D = 3.8\text{ A}$		0.069	0.084	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 4.4\text{ A}$		10		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		600		pF
Output Capacitance	C_{oss}			90		
Reverse Transfer Capacitance	C_{rss}			50		
Total Gate Charge	Q_g	$V_{DS} = 50\text{ V}, V_{GS} = 10\text{ V}, I_D = 4.4\text{ A}$		13.5	20	nC
				9	13.5	
Gate-Source Charge	Q_{gs}	$V_{DS} = 50\text{ V}, V_{GS} = 6\text{ V}, I_D = 4.4\text{ A}$		3		
Gate-Drain Charge	Q_{gd}			4.6		
Gate Resistance	R_g	$f = 1\text{ MHz}$		1		Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 50\text{ V}, R_L = 14.3\text{ }\Omega$ $I_D \cong 3.5\text{ A}, V_{GEN} = 6\text{ V}, R_g = 1\text{ }\Omega$		15	25	ns
Rise Time	t_r			12	20	
Turn-Off Delay Time	$t_{d(off)}$			12	20	
Fall Time	t_f			10	15	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 50\text{ V}, R_L = 14.3\text{ }\Omega$ $I_D \cong 3.5\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$		10	15	
Rise Time	t_r			12	20	
Turn-Off Delay Time	$t_{d(off)}$			15	25	
Fall Time	t_f			10	15	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$			5	A
Pulse Diode Forward Current	I_{SM}				20	
Body Diode Voltage	V_{SD}	$I_S = 3.5\text{ A}, V_{GS} = 0\text{ V}$		0.8	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 3.5\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		45	70	ns
Body Diode Reverse Recovery Charge	Q_{rr}			80	120	nC
Reverse Recovery Fall Time	t_a			33		ns
Reverse Recovery Rise Time	t_b			12		

Notes:

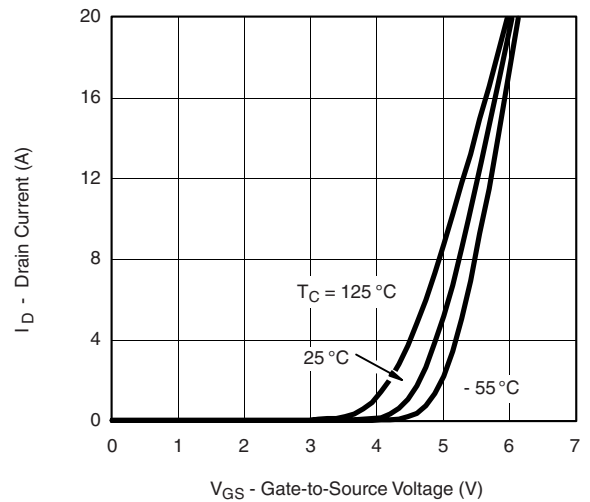
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

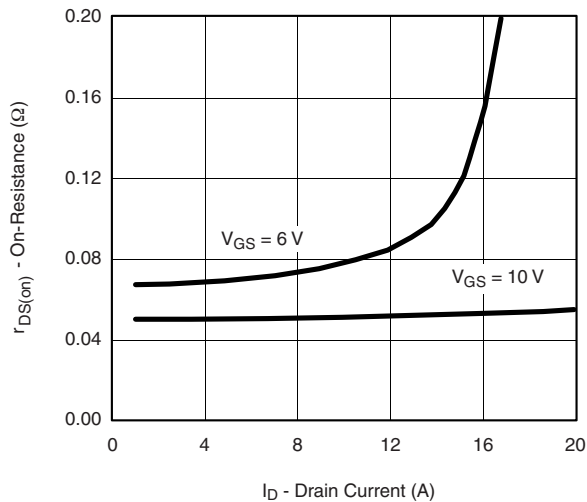
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



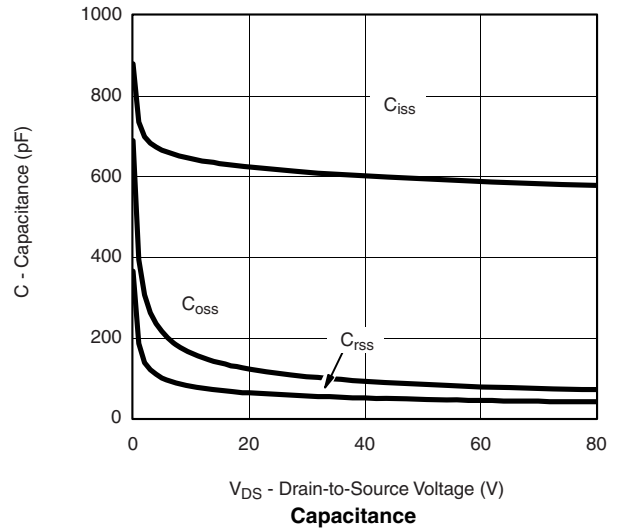
V_{DS} - Drain-to-Source Voltage (V)
Output Characteristics



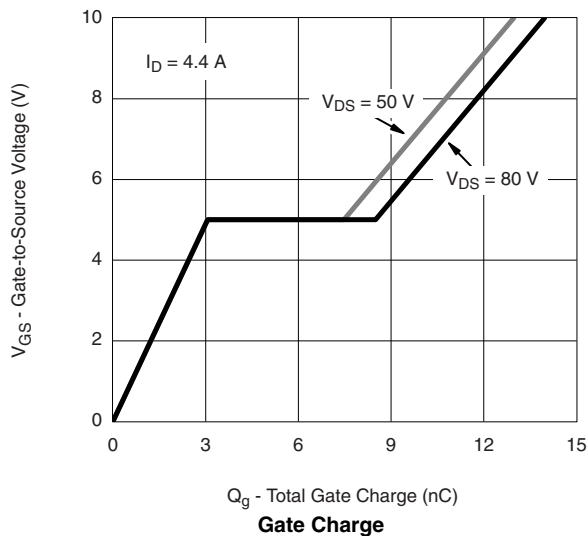
V_{GS} - Gate-to-Source Voltage (V)
Transfer Characteristics



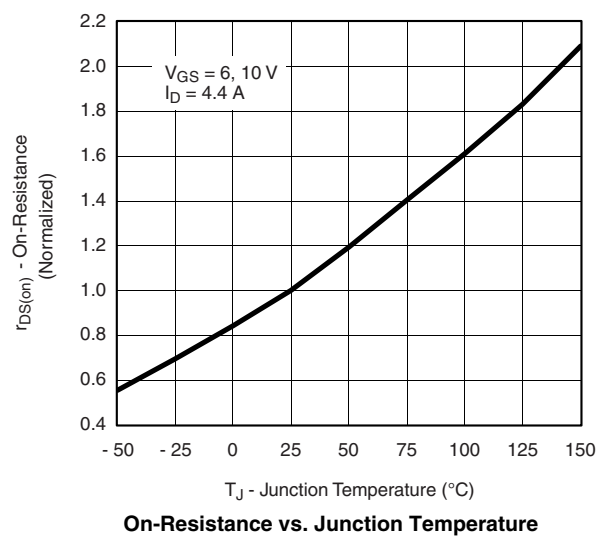
On-Resistance vs. Drain Current



Capacitance



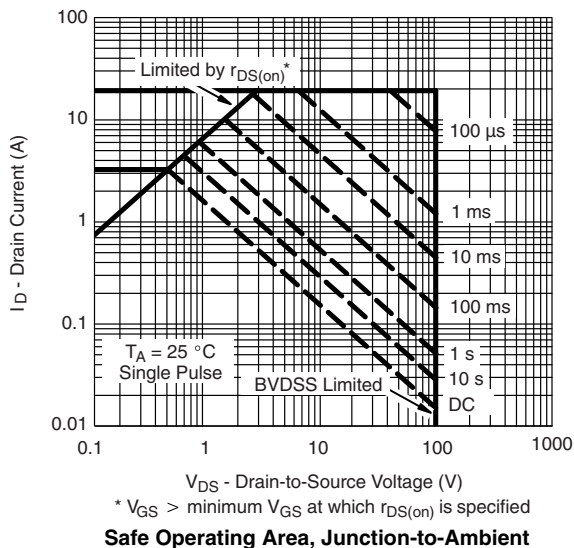
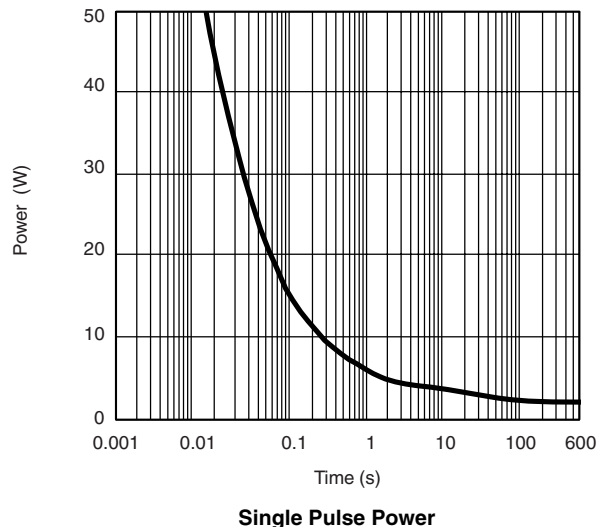
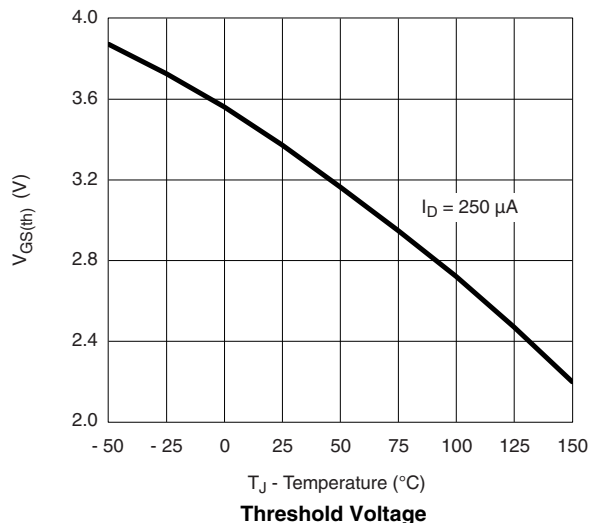
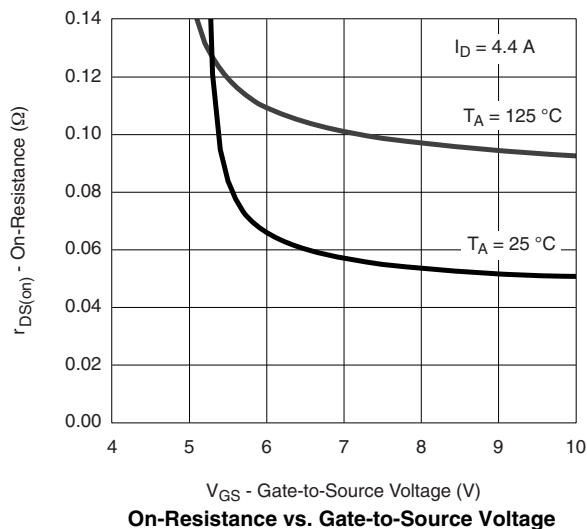
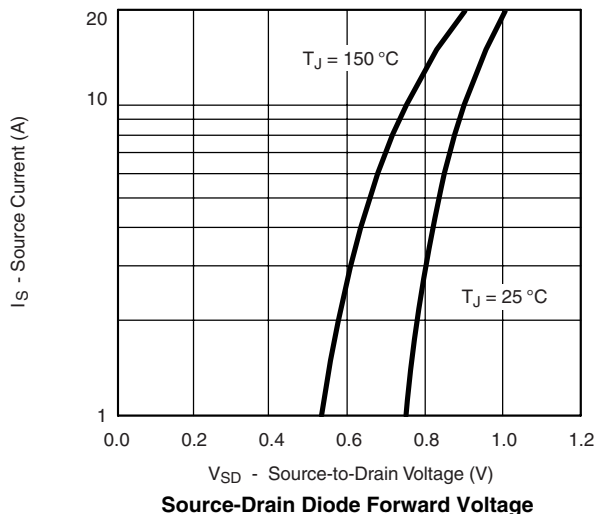
Gate Charge



On-Resistance vs. Junction Temperature

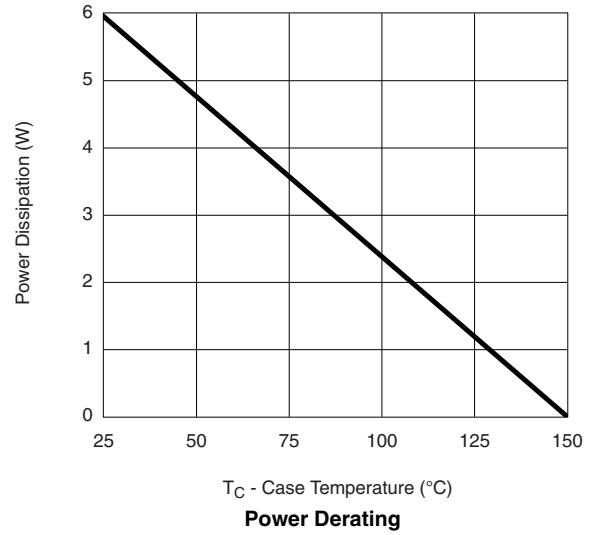
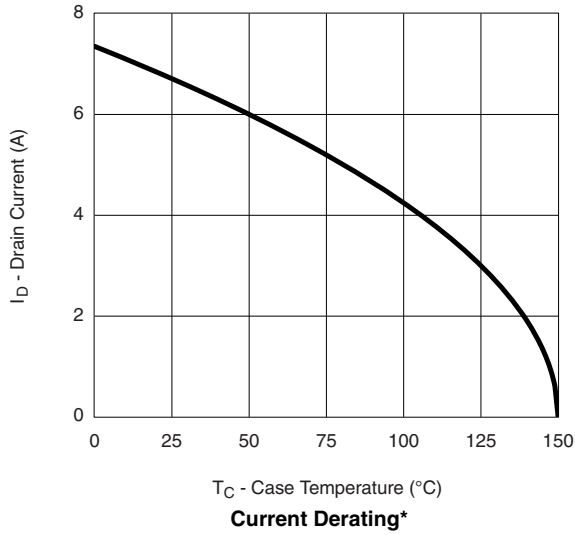


TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted





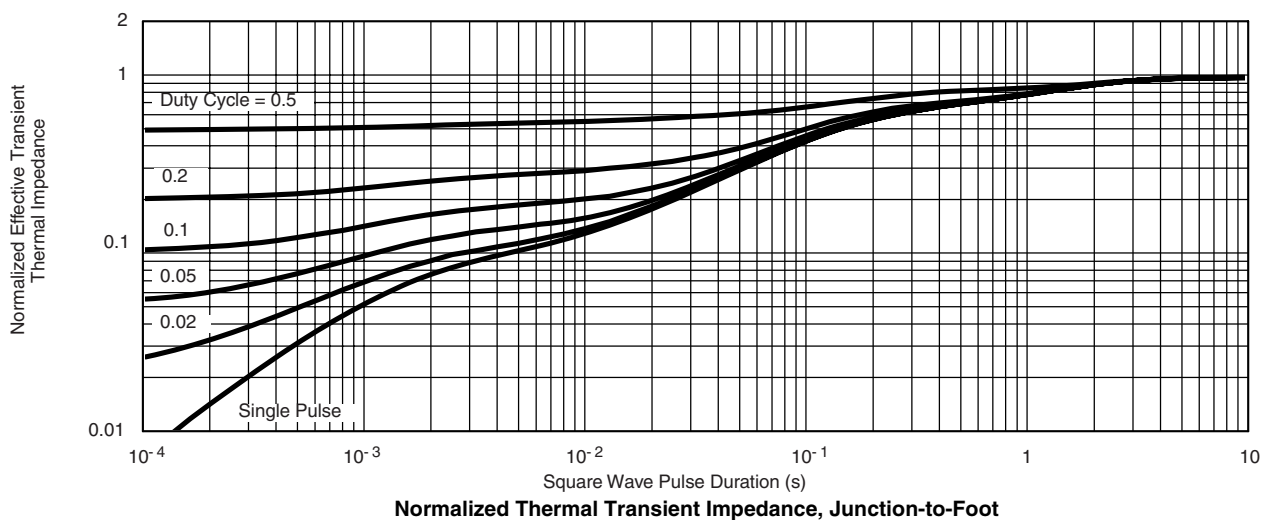
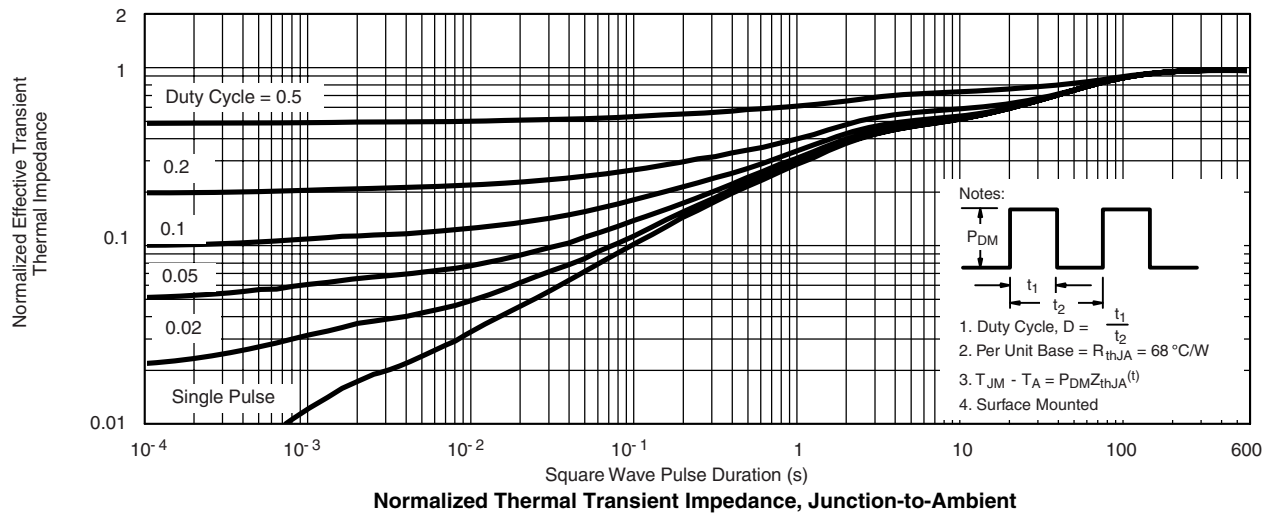
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



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