International
IOR Rectifier

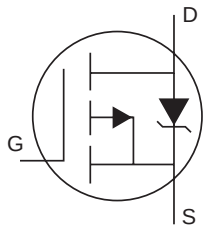
DIGITAL AUDIO MOSFET

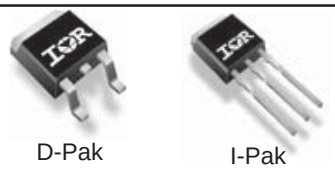
IRLR9343
IRLU9343
IRLU9343-701

Features

- Advanced Process Technology
- Key Parameters Optimized for Class-D Audio Amplifier Applications
- Low R_{DSON} for Improved Efficiency
- Low Q_g and Q_{sw} for Better THD and Improved Efficiency
- Low Q_{rr} for Better THD and Lower EMI
- 175°C Operating Junction Temperature for Ruggedness
- Repetitive Avalanche Capability for Robustness and Reliability
- Multiple Package Options

Key Parameters		
V_{DS}	-55	V
$R_{DS(ON)}$ typ. @ V_{GS} = -10V	93	mΩ
$R_{DS(ON)}$ typ. @ V_{GS} = -4.5V	150	mΩ
Q_g typ.	31	nC
T_J max	175	°C





D-Pak
IRLR9343

I-Pak
IRLU9343

I-Pak Leadform 701
IRLU9343-701
Refer to page 10 for package outline

Description

This Digital Audio HEXFET® is specifically designed for Class-D audio amplifier applications. This MosFET utilizes the latest processing techniques to achieve low on-resistance per silicon area. Furthermore, Gate charge, body-diode reverse recovery and internal Gate resistance are optimized to improve key Class-D audio amplifier performance factors such as efficiency, THD and EMI. Additional features of this MosFET are 175°C operating junction temperature and repetitive avalanche capability. These features combine to make this MosFET a highly efficient, robust and reliable device for Class-D audio amplifier applications.

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{DS}	Drain-to-Source Voltage	-55	V
V_{GS}	Gate-to-Source Voltage	±20	
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ -10V	-20	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	-14	
I_{DM}	Pulsed Drain Current ①	-60	
P_D @T_C = 25°C	Power Dissipation	79	W
P_D @T_C = 100°C	Power Dissipation	39	
	Linear Derating Factor	0.53	W/°C
T_J T_{STG}	Operating Junction and Storage Temperature Range	-40 to + 175	°C
	Clamping Pressure ⑥	——	N

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑤	——	1.9	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mounted) ⑤⑧	——	50	
$R_{\theta JA}$	Junction-to-Ambient (free air) ⑤	——	110	

Notes ① through ⑨ are on page 10

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

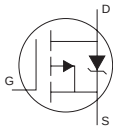
	Parameter	Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	-55	—	—	V	V_{GS} = 0V, I_D = -250µA
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	-52	—	mV/°C	Reference to 25°C, I_D = -1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	93	105	mΩ	V_{GS} = -10V, I_D = -3.4A ③
		—	150	170		V_{GS} = -4.5V, I_D = -2.7A ③
$V_{GS(th)}$	Gate Threshold Voltage	-1.0	—	—	V	V_{DS} = V_{GS}, I_D = -250µA
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	-3.7	—	mV/°C	
I_{DSS}	Drain-to-Source Leakage Current	—	—	-2.0	µA	V_{DS} = -55V, V_{GS} = 0V
		—	—	-25		V_{DS} = -55V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	-100	nA	V_{GS} = -20V
	Gate-to-Source Reverse Leakage	—	—	100		V_{GS} = 20V
g_{fs}	Forward Transconductance	5.3	—	—	S	V_{DS} = -25V, I_D = -14A
Q_g	Total Gate Charge	—	31	47		V_{DS} = -44V
Q_{gs}	Gate-to-Source Charge	—	7.1	—		V_{GS} = -10V
Q_{gd}	Gate-to-Drain Charge	—	8.5	—		I_D = -14A
Q_{godr}	Gate Charge Overdrive	—	15	—		See Fig. 6 and 19
$t_{d(on)}$	Turn-On Delay Time	—	9.5	—		V_{DD} = -28V, V_{GS} = -10V ③
t_r	Rise Time	—	24	—		I_D = -14A
$t_{d(off)}$	Turn-Off Delay Time	—	21	—	ns	R_G = 2.5Ω
t_f	Fall Time	—	9.5	—		
C_{iss}	Input Capacitance	—	660	—		V_{GS} = 0V
C_{oss}	Output Capacitance	—	160	—	pF	V_{DS} = -50V
C_{rss}	Reverse Transfer Capacitance	—	72	—		f = 1.0MHz, See Fig.5
C_{oss}	Effective Output Capacitance	—	280	—		V_{GS} = 0V, V_{DS} = 0V to -44V
L_D	Internal Drain Inductance	—	4.5	—		Between lead,
					nH	6mm (0.25in.)
L_S	Internal Source Inductance	—	7.5	—		from package
						and center of die contact ④

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy②	—	120	mJ
I_{AR}	Avalanche Current ⑦	See Fig. 14, 15, 17a, 17b		A
E_{AR}	Repetitive Avalanche Energy ⑦			mJ

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S @ T_C = 25°C	Continuous Source Current	—	—	-20		MOSFET symbol
	(Body Diode)				A	showing the
I_{SM}	Pulsed Source Current	—	—	-60		integral reverse
	(Body Diode) ①					p-n junction diode.
V_{SD}	Diode Forward Voltage	—	—	-1.2	V	T_J = 25°C, I_S = -14A, V_{GS} = 0V ③
t_{rr}	Reverse Recovery Time	—	57	86	ns	T_J = 25°C, I_F = -14A
Q_{rr}	Reverse Recovery Charge	—	120	180	nC	di/dt = 100A/µs ③



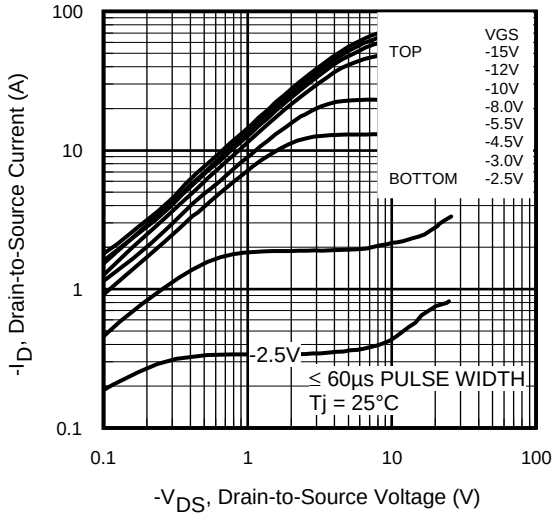


Fig 1. Typical Output Characteristics

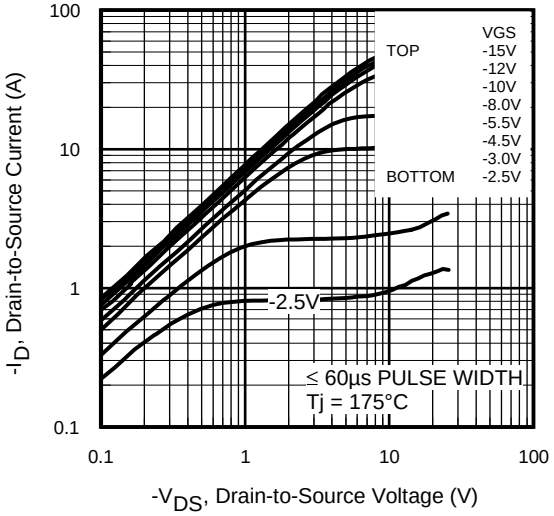


Fig 2. Typical Output Characteristics

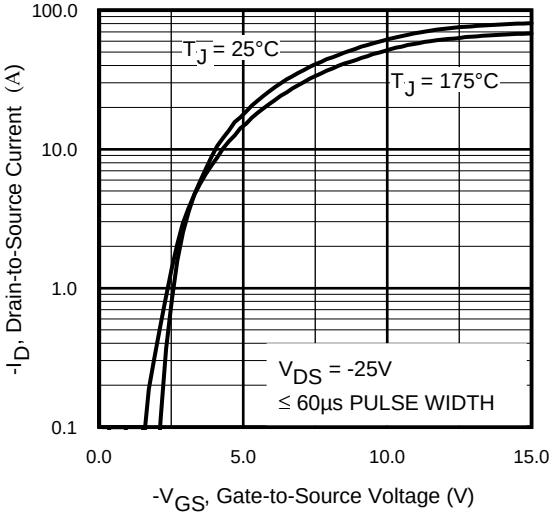


Fig 3. Typical Transfer Characteristics

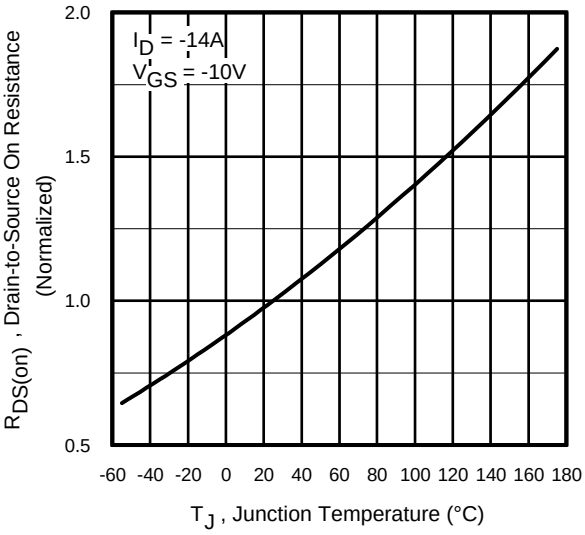


Fig 4. Normalized On-Resistance vs. Temperature

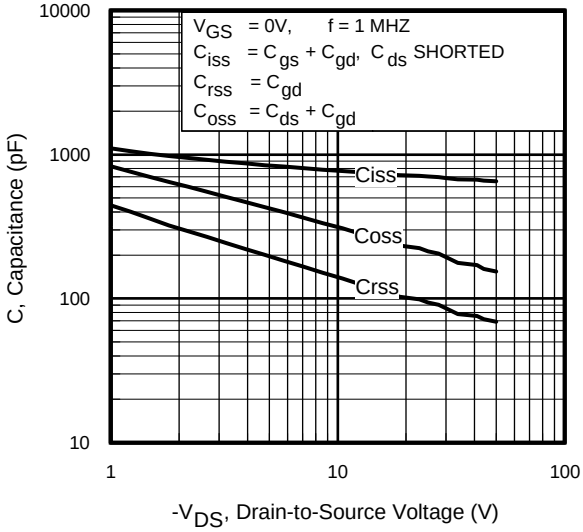


Fig 5. Typical Capacitance vs.Drain-to-Source Voltage

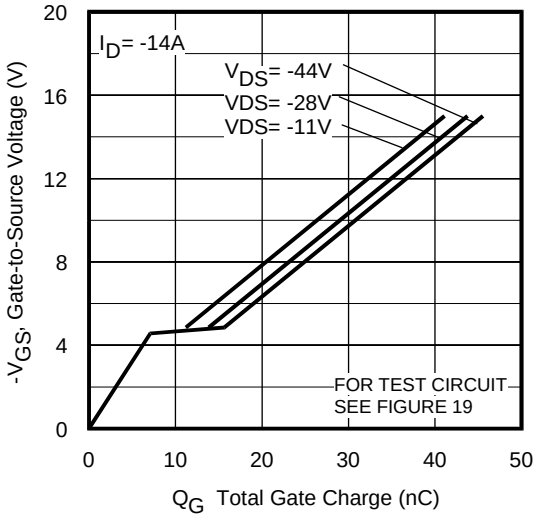


Fig 6. Typical Gate Charge vs.Gate-to-Source Voltage

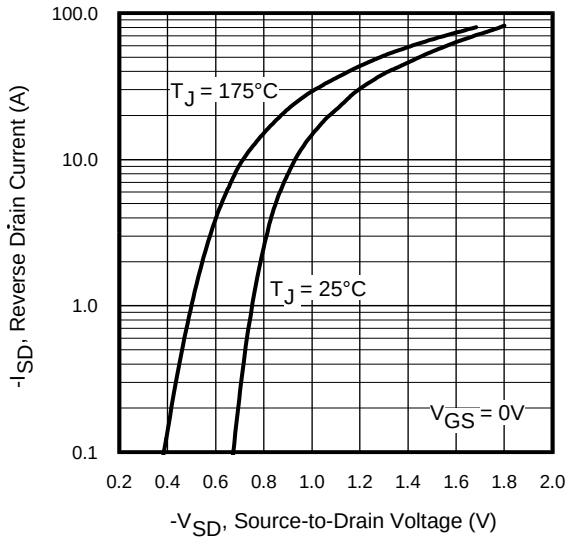


Fig 7. Typical Source-Drain Diode Forward Voltage

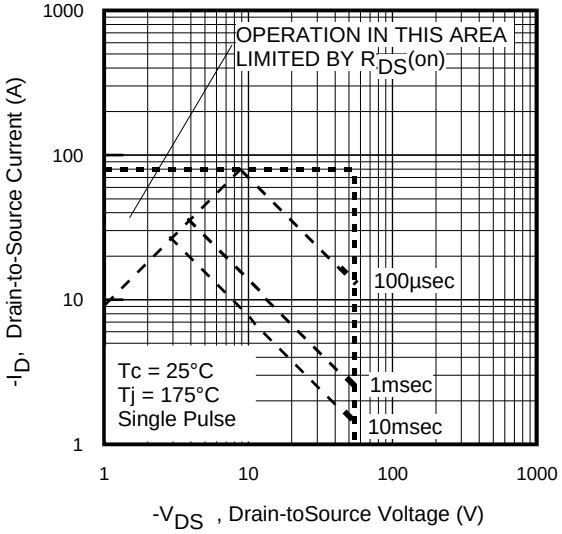


Fig 8. Maximum Safe Operating Area

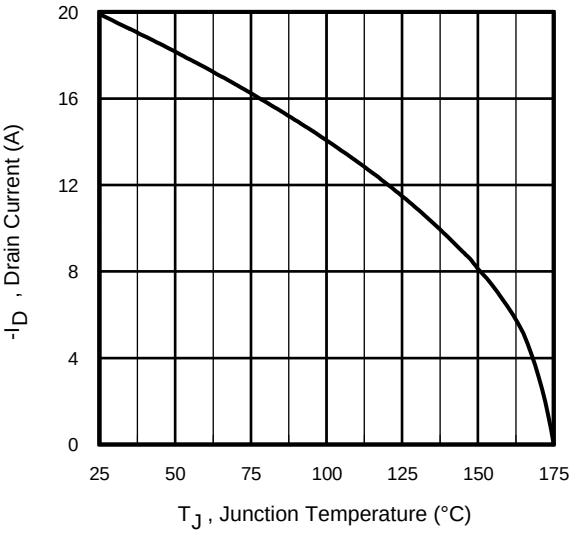


Fig 9. Maximum Drain Current vs. Case Temperature

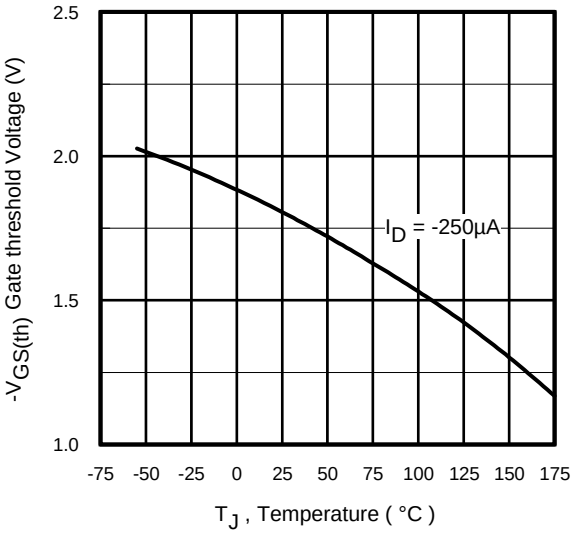


Fig 10. Threshold Voltage vs. Temperature

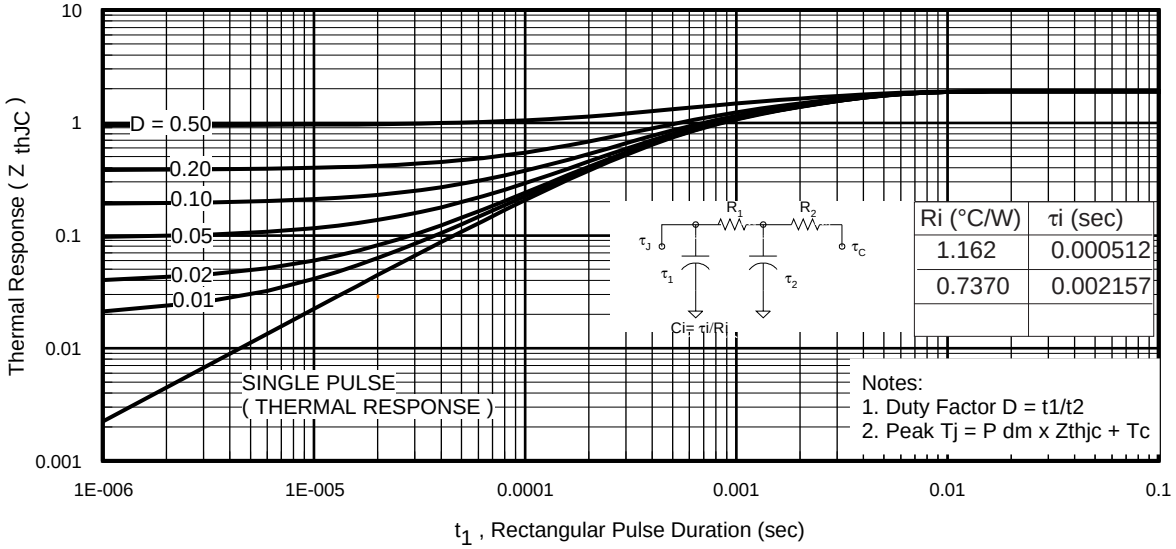


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

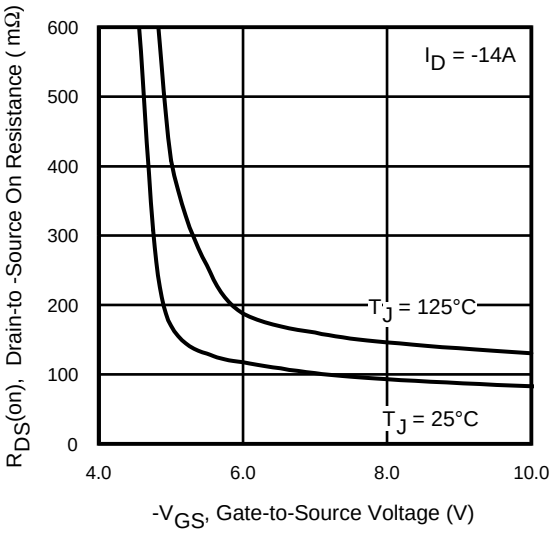


Fig 12. On-Resistance Vs. Gate Voltage

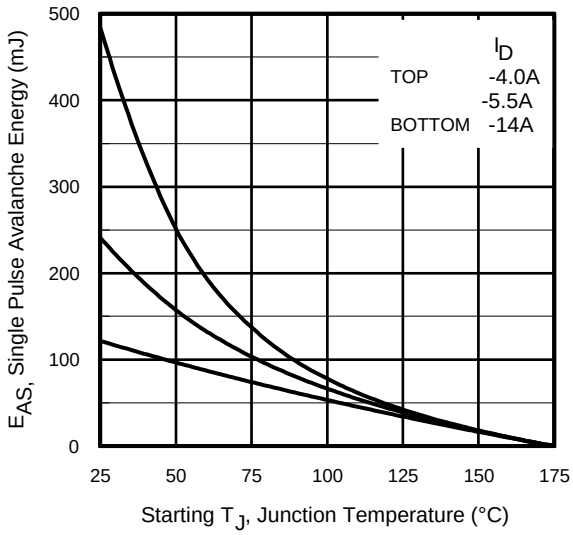


Fig 13. Maximum Avalanche Energy Vs. Drain Current

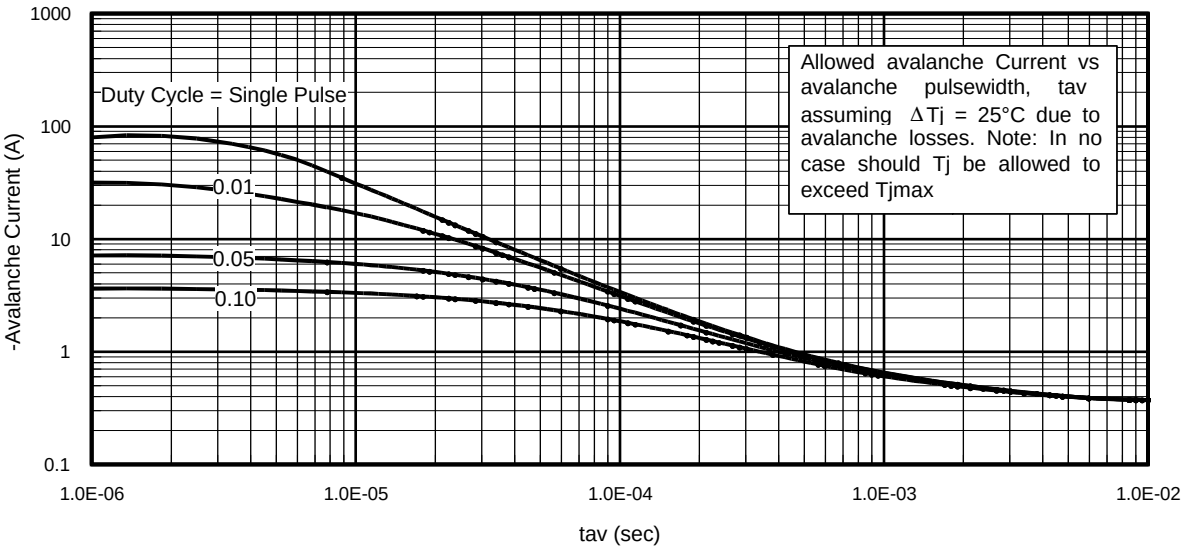


Fig 14. Typical Avalanche Current Vs.Pulsewidth

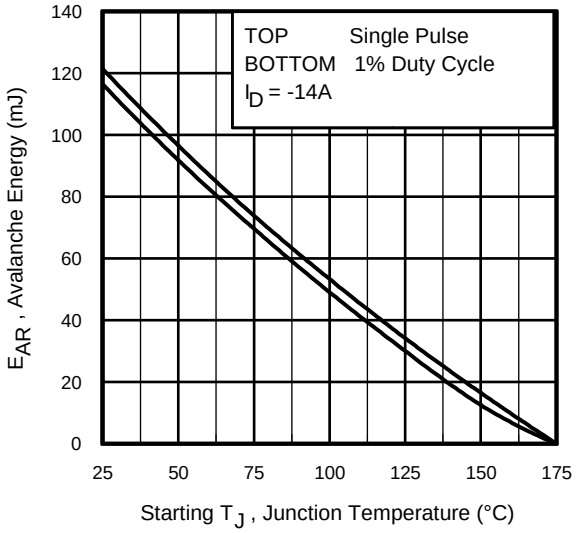


Fig 15. Maximum Avalanche Energy Vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 14, 15:
(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long asT_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 17a, 17b.
4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 14, 15).
   t_{av} = Average time in avalanche.
   D = Duty cycle in avalanche = $t_{av} \cdot f$
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see figure 11)

$$P_{D\ (ave)} = 1/2\ (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS\ (AR)} = P_{D\ (ave)} \cdot t_{av}$$

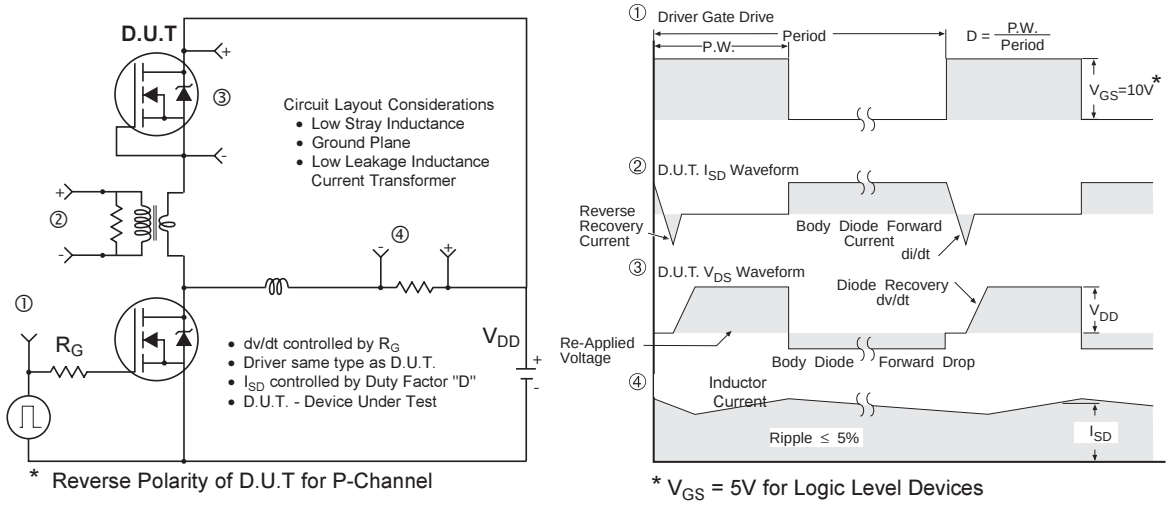


Fig 16. Peak Diode Recovery dv/dt Test Circuit for P-Channel HEXFET® Power MOSFETs

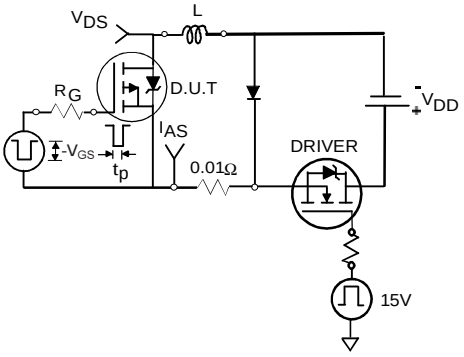


Fig 17a. Unclamped Inductive Test Circuit

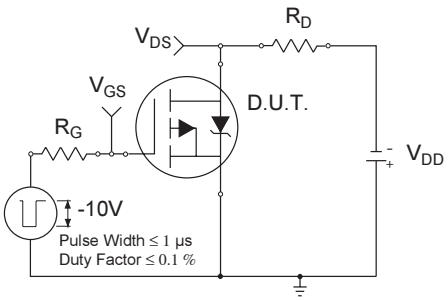


Fig 18a. Switching Time Test Circuit

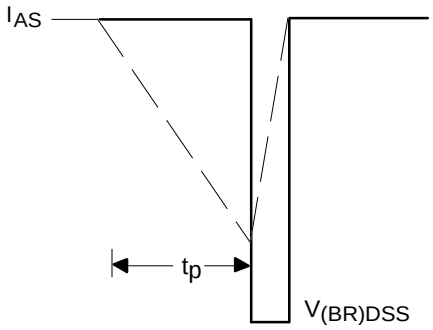


Fig 17b. Unclamped Inductive Waveforms

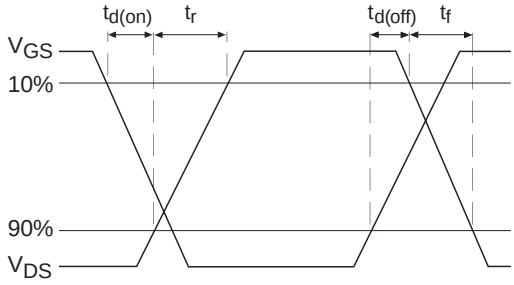


Fig 18b. Switching Time Waveforms

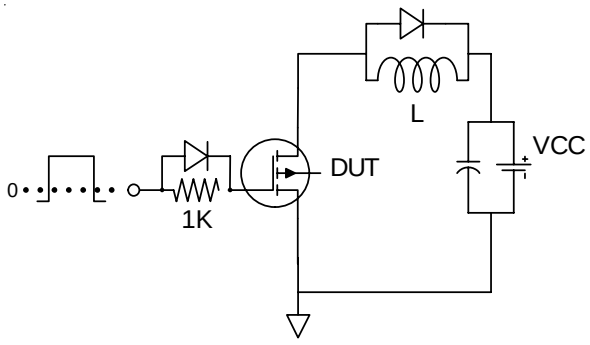


Fig 19a. Gate Charge Test Circuit

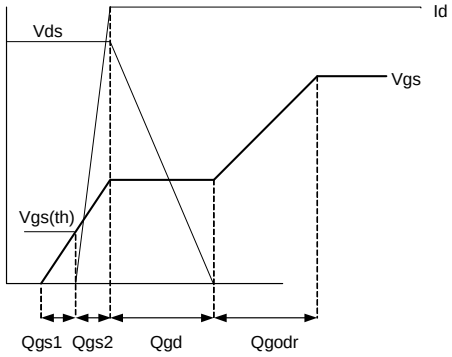
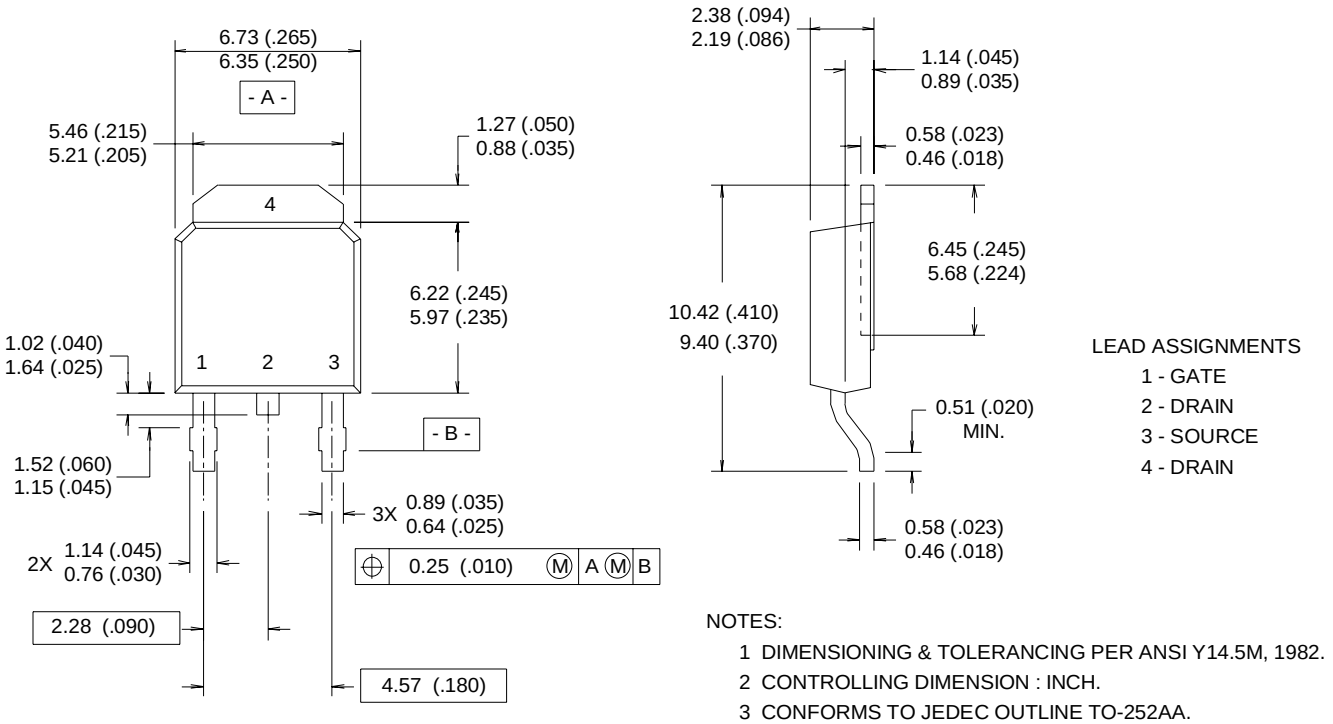


Fig 19b Gate Charge Waveform

D-Pak (TO-252AA) Package Outline

Dimensions are shown in millimeters (inches)



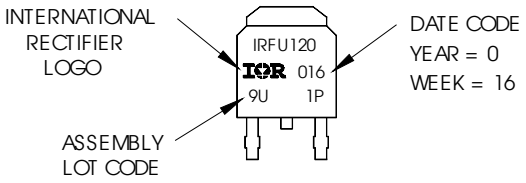
LEAD ASSIGNMENTS
1 - GATE
2 - DRAIN
3 - SOURCE
4 - DRAIN

NOTES:
1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 CONFORMS TO JEDEC OUTLINE TO-252AA.
4 DIMENSIONS SHOWN ARE BEFORE SOLDER DIP, SOLDER DIP MAX. +0.16 (.006).

D-Pak (TO-252AA) Part Marking Information

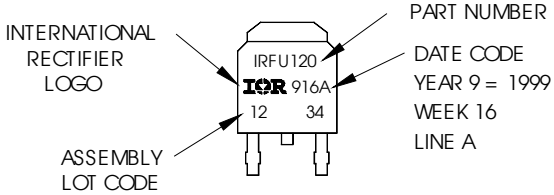
Notes: This part marking information applies to devices produced before 02/26/2001

EXAMPLE: THIS IS AN IRFR120
WITH ASSEMBLY
LOT CODE 9U1P



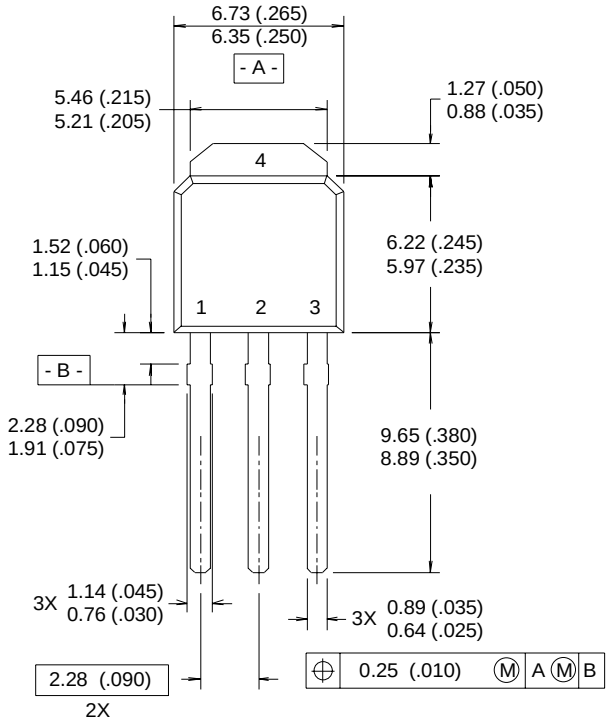
Notes: This part marking information applies to devices produced after 02/26/2001

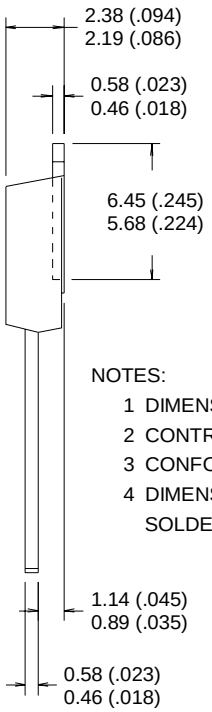
EXAMPLE: THIS IS AN IRFR120
WITH ASSEMBLY
LOT CODE 1234
ASSEMBLED ON WW 16, 1999
IN THE ASSEMBLY LINE "A"



I-Pak (TO-251AA) Package Outline

Dimensions are shown in millimeters (inches)





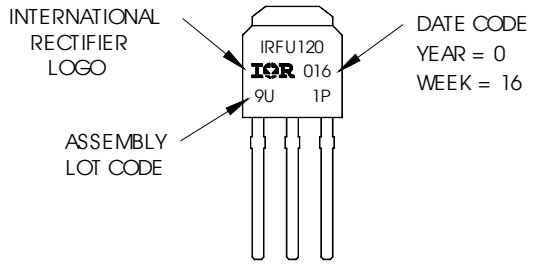
LEAD ASSIGNMENTS
1 - GATE
2 - DRAIN
3 - SOURCE
4 - DRAIN

NOTES:
1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 CONFORMS TO JEDEC OUTLINE TO-252AA.
4 DIMENSIONS SHOWN ARE BEFORE SOLDER DIP, SOLDER DIP MAX. +0.16 (.006).

I-Pak (TO-251AA) Part Marking Information

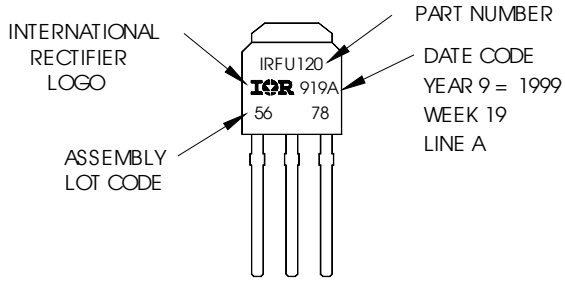
Notes: This part marking information applies to devices produced before 02/26/2001

EXAMPLE: THIS IS AN IRFR120
WITH ASSEMBLY
LOT CODE 9U1P



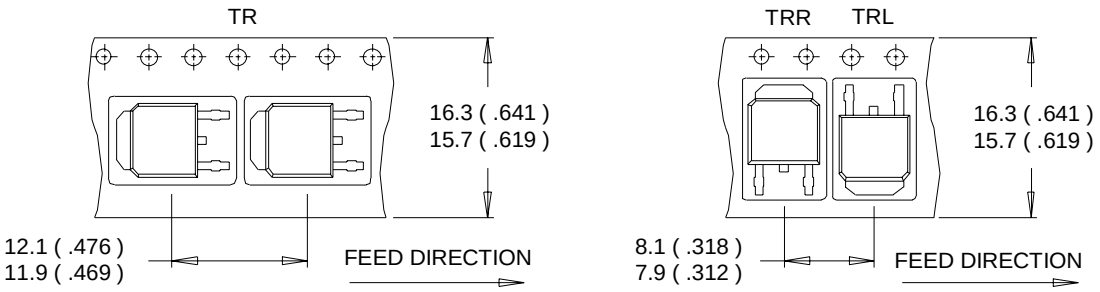
Notes: This part marking information applies to devices produced after 02/26/2001

EXAMPLE: THIS IS AN IRFR120
WITH ASSEMBLY
LOT CODE 5678
ASSEMBLED ON WW 19, 1999
IN THE ASSEMBLY LINE "A"

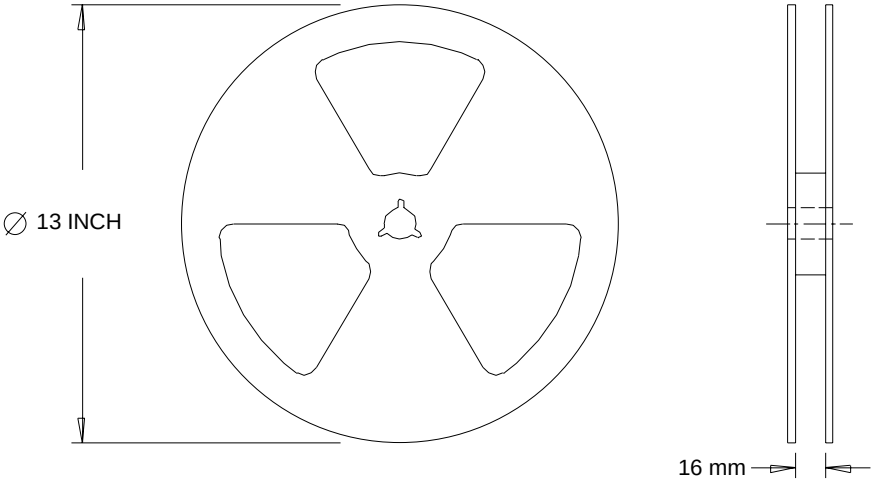


D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.

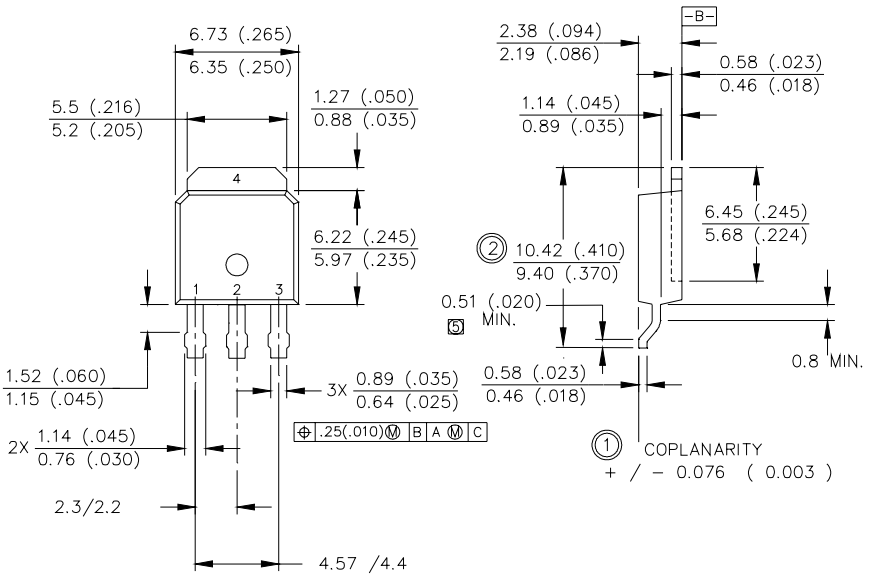


NOTES :
1. OUTLINE CONFORMS TO EIA-481.

International
IOR Rectifier

I-Pak Leadform Option 701 Package Outline ⑨

Dimensions are shown in millimeters (inches)



1-. GATE
2-. DRAIN
3-. SOURCE
4-. DRAIN

NOTES:

1.0 CONTROL DIMENSIONS IN INCHES
2.0 PARALLELISM AND ANGULARITY MAX. 0.076 (0.003)
3.0 LEADFORM CRITICAL DIMENSIONS DOUBLE RINGED

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.
② Starting T_J = 25°C, L = 1.24mH, R_G = 25Ω, I_{AS} = -14A.
③ Pulse width ≤ 400µs; duty cycle ≤ 2%.
④ This only applies for I-Pak, L_S of D-Pak is measured between lead and center of die contact
⑤ R_θ is measured at T_J of approximately 90°C.
⑥ Contact factory for mounting information
⑦ Limited by Tjmax. See Figs. 14, 15, 17a, 17b for repetitive avalanche information
⑧ When D-Pak mounted on 1" square PCB (FR-4 or G-10 Material) . For recommended footprint and soldering techniques refer to application note #AN-994
⑨ Refer to D-Pak package for Part Marking, Tape and Reel information.

Data and specifications subject to change without notice.
This product has been designed for the Industrial market.
Qualification Standards can be found on IR's Web site.

International
IOR Rectifier

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Note: For the most current drawings please refer to the IR website at:
http://www.irf.com/package/