

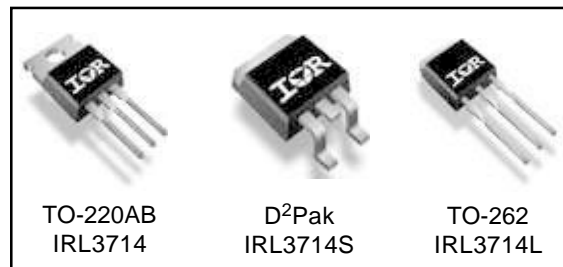
**Applications**

- High Frequency Isolated DC-DC Converters with Synchronous Rectification for Telecom and Industrial Use
- High Frequency Buck Converters for Computer Processor Power

<b>V<sub>DSS</sub></b>	<b>R<sub>DS(on)</sub> max</b>	<b>I<sub>D</sub></b>
<b>20V</b>	<b>20mΩ</b>	<b>36A</b>

**Benefits**

- Ultra-Low Gate Impedance
- Very Low R<sub>DS(on)</sub> at 4.5V V<sub>GS</sub>
- Fully Characterized Avalanche Voltage and Current



**Absolute Maximum Ratings**

Symbol	Parameter	Max.	Units
V <sub>DS</sub>	Drain-Source Voltage	20	V
V <sub>GS</sub>	Gate-to-Source Voltage	± 20	V
I <sub>D</sub> @ T <sub>C</sub> = 25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V	36	A
I <sub>D</sub> @ T <sub>C</sub> = 70°C	Continuous Drain Current, V <sub>GS</sub> @ 10V	31	
I <sub>DM</sub>	Pulsed Drain Current <sup>①</sup>	140	
P <sub>D</sub> @ T <sub>C</sub> = 25°C	Maximum Power Dissipation <sup>③</sup>	47	W
P <sub>D</sub> @ T <sub>C</sub> = 70°C	Maximum Power Dissipation <sup>③</sup>	33	W
	Linear Derating Factor	0.31	W/°C
T <sub>J</sub> , T <sub>STG</sub>	Junction and Storage Temperature Range	-55 to + 175	°C

**Thermal Resistance**

	Parameter	Typ.	Max.	Units
R <sub>θJC</sub>	Junction-to-Case	—	3.2	°C/W
R <sub>θCS</sub>	Case-to-Sink, Flat, Greased Surface <sup>④</sup>	0.50	—	
R <sub>θJA</sub>	Junction-to-Ambient <sup>④</sup>	—	62	
R <sub>θJA</sub>	Junction-to-Ambient (PCB mount) <sup>⑤</sup>	—	40	

Notes ① through ⑥ are on page 11

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# IRL3714/3714S/3714L

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## Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	20	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.022	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	15	20	m $\Omega$	$V_{GS} = 10V, I_D = 18A$ ③
		—	21	28		$V_{GS} = 4.5V, I_D = 14A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	3.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	20	$\mu A$	$V_{DS} = 16V, V_{GS} = 0V$
		—	—	100		$V_{DS} = 16V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	200	nA	$V_{GS} = 16V$
	Gate-to-Source Reverse Leakage	—	—	-200		$V_{GS} = -16V$

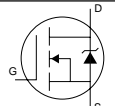
## Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

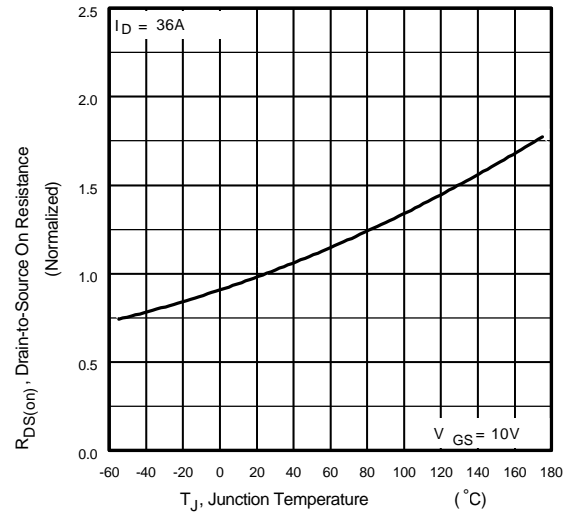
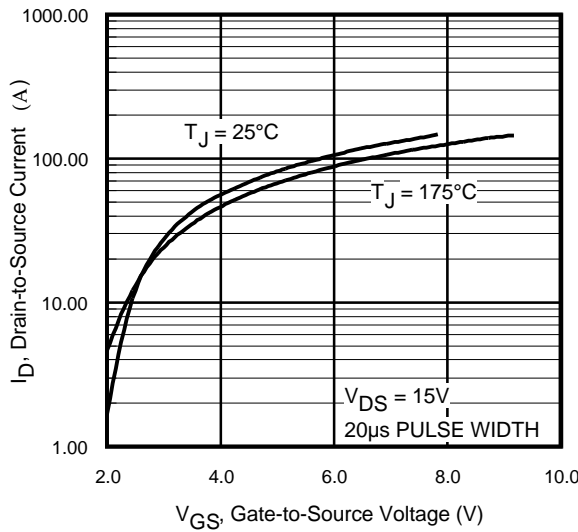
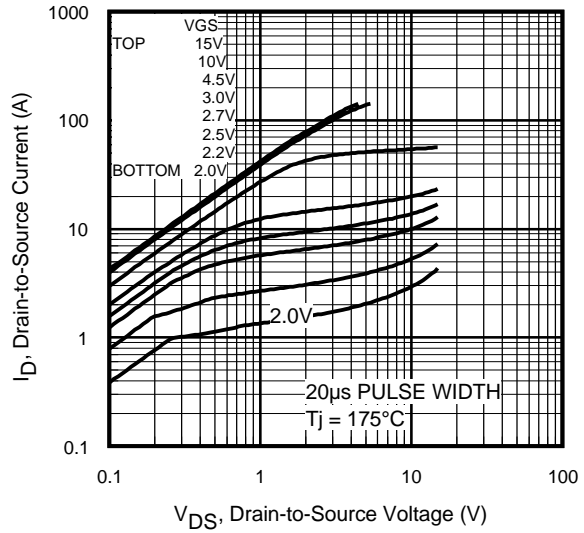
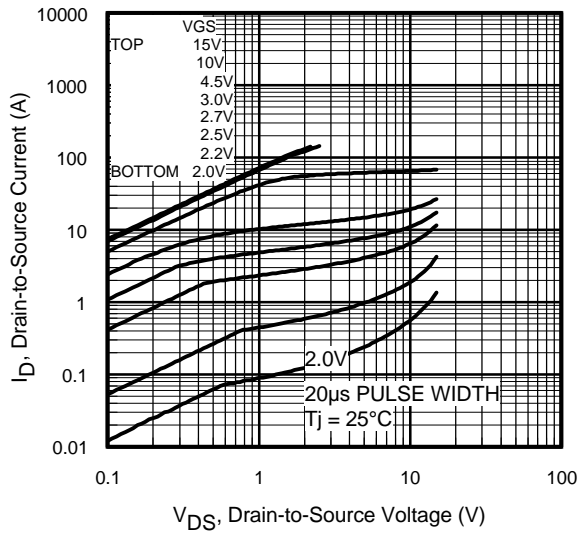
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$g_{fs}$	Forward Transconductance	17	—	—	S	$V_{DS} = 10V, I_D = 14A$
$Q_g$	Total Gate Charge	—	6.5	9.7	nC	$I_D = 14A$
$Q_{gs}$	Gate-to-Source Charge	—	1.8	—		$V_{DS} = 10V$
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	2.9	—		$V_{GS} = 4.5V$
$Q_{oss}$	Output Gate Charge	—	7.1	—		$V_{GS} = 0V, V_{DS} = 10V$
$t_{d(on)}$	Turn-On Delay Time	—	8.7	—	ns	$V_{DD} = 10V$
$t_r$	Rise Time	—	78	—		$I_D = 14A$
$t_{d(off)}$	Turn-Off Delay Time	—	10	—		$R_G = 1.8\Omega$
$t_f$	Fall Time	—	4.5	—		$V_{GS} = 4.5V$ ③
$C_{iss}$	Input Capacitance	—	670	—	pF	$V_{GS} = 0V$
$C_{oss}$	Output Capacitance	—	470	—		$V_{DS} = 10V$
$C_{rss}$	Reverse Transfer Capacitance	—	68	—		$f = 1.0\text{MHz}$

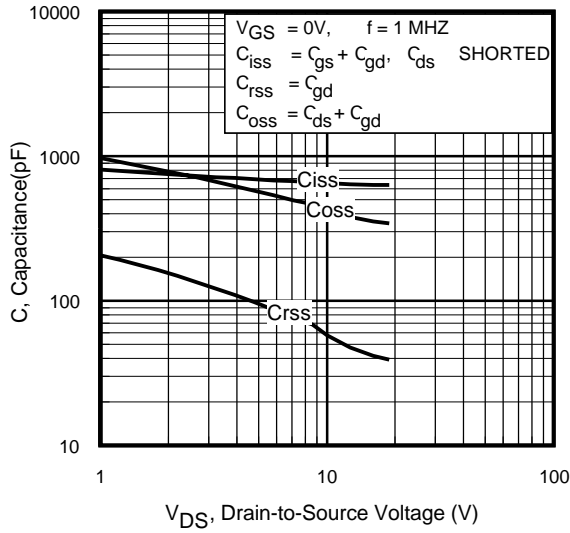
## Avalanche Characteristics

Symbol	Parameter	Typ.	Max.	Units
$E_{AS}$	Single Pulse Avalanche Energy②	—	72	mJ
$I_{AR}$	Avalanche Current①	—	14	A

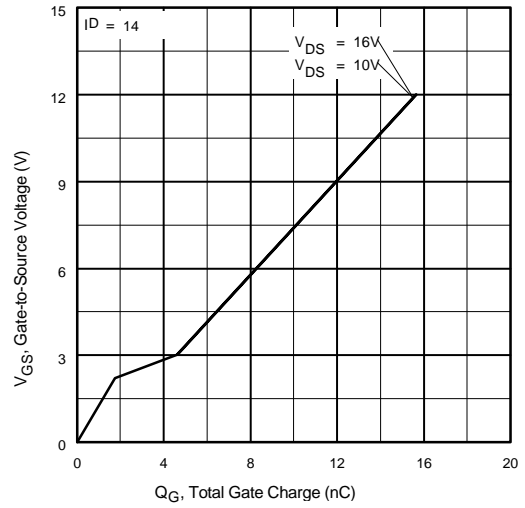
## Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	36	—	A	MOSFET symbol showing the integral reverse p-n junction diode. 
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	140	—		
$V_{SD}$	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 18A, V_{GS} = 0V$ ③
		—	0.88	—		$T_J = 125^\circ\text{C}, I_S = 18A, V_{GS} = 0V$ ③
$t_{rr}$	Reverse Recovery Time	—	35	53	ns	$T_J = 25^\circ\text{C}, I_F = 18A, V_R = 10V$
$Q_{rr}$	Reverse Recovery Charge	—	34	51	nC	$di/dt = 100A/\mu s$ ③
$t_{rr}$	Reverse Recovery Time	—	35	53	ns	$T_J = 125^\circ\text{C}, I_F = 18A, V_R = 10V$
$Q_{rr}$	Reverse Recovery Charge	—	35	53	nC	$di/dt = 100A/\mu s$ ③

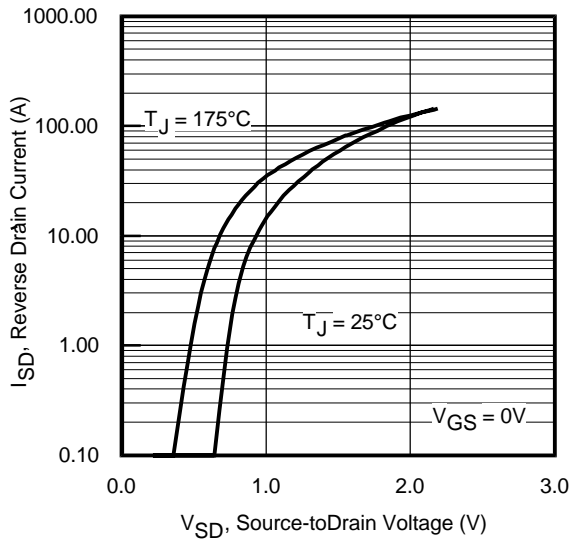




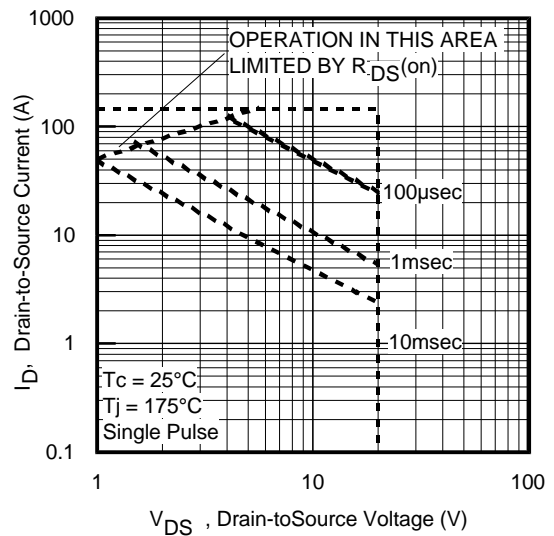
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



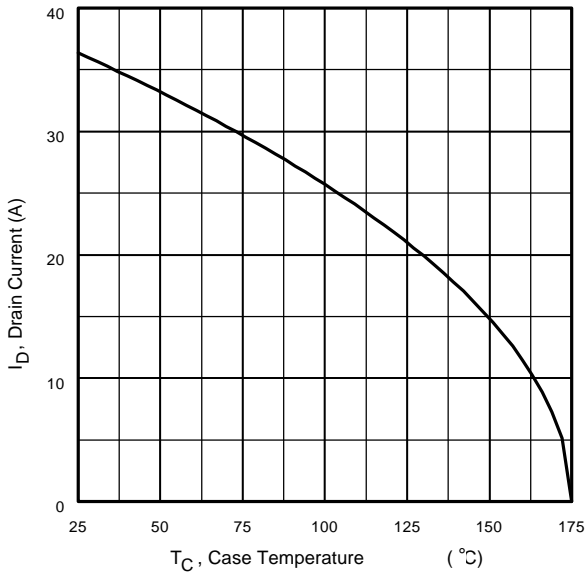
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



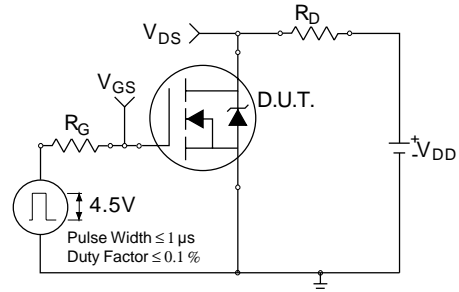
**Fig 7.** Typical Source-Drain Diode Forward Voltage



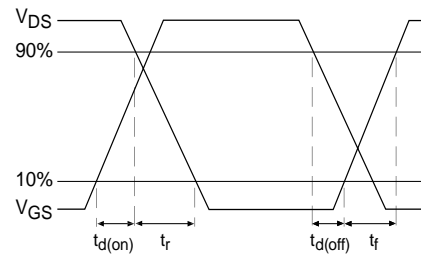
**Fig 8.** Maximum Safe Operating Area



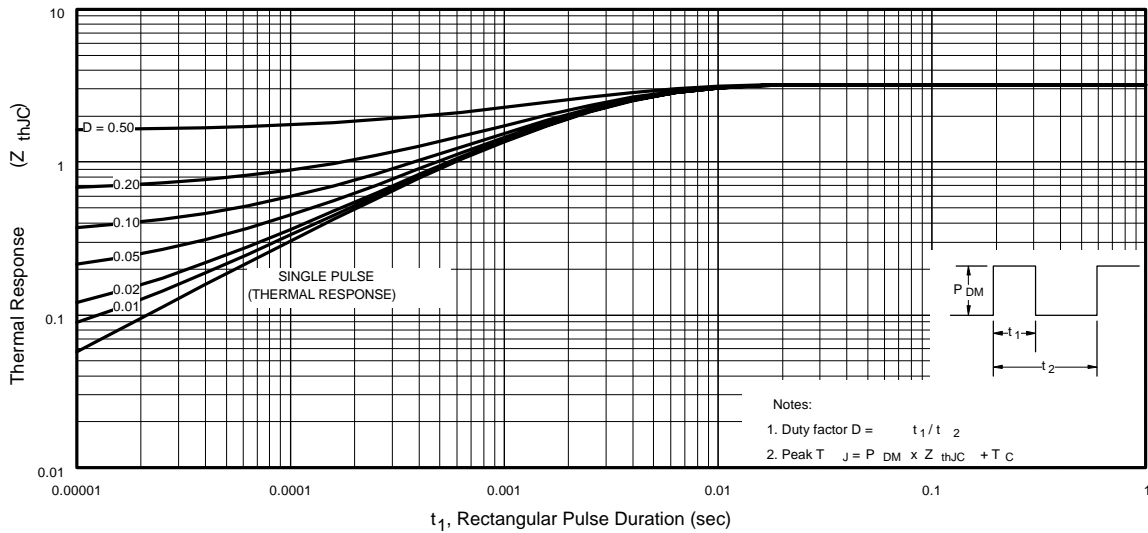
**Fig 9.** Maximum Drain Current Vs. Case Temperature



**Fig 10a.** Switching Time Test Circuit



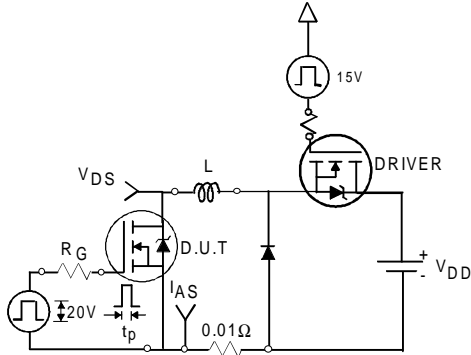
**Fig 10b.** Switching Time Waveforms



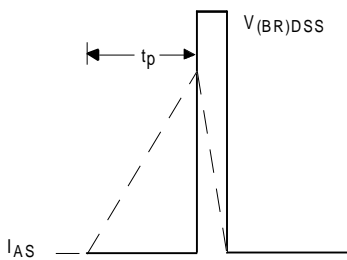
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

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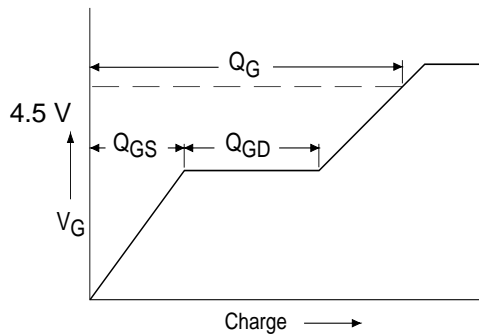
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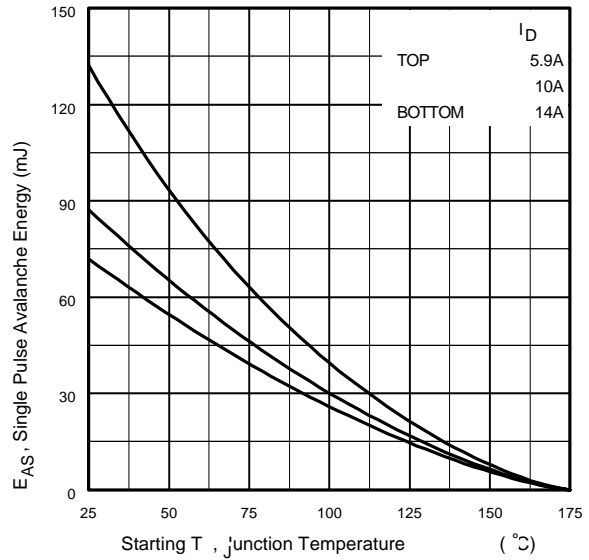
**Fig 12a.** Unclamped Inductive Test Circuit



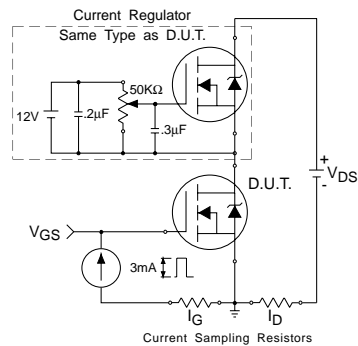
**Fig 12b.** Unclamped Inductive Waveforms



**Fig 13a.** Basic Gate Charge Waveform

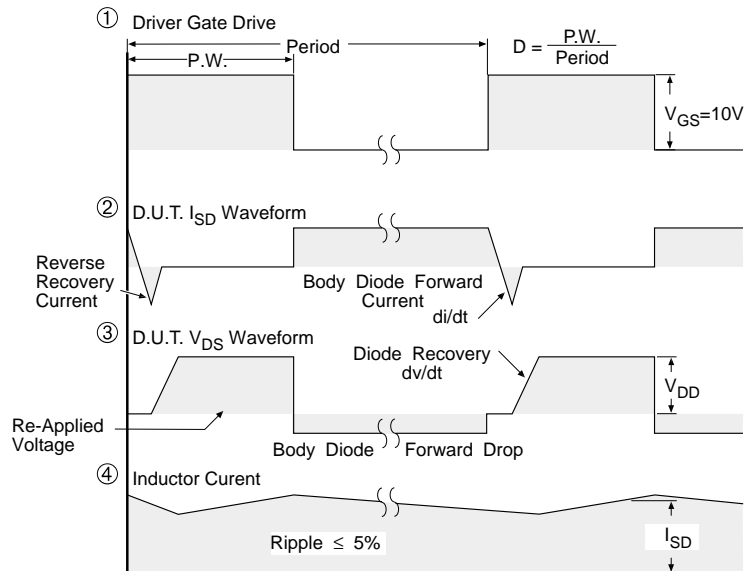
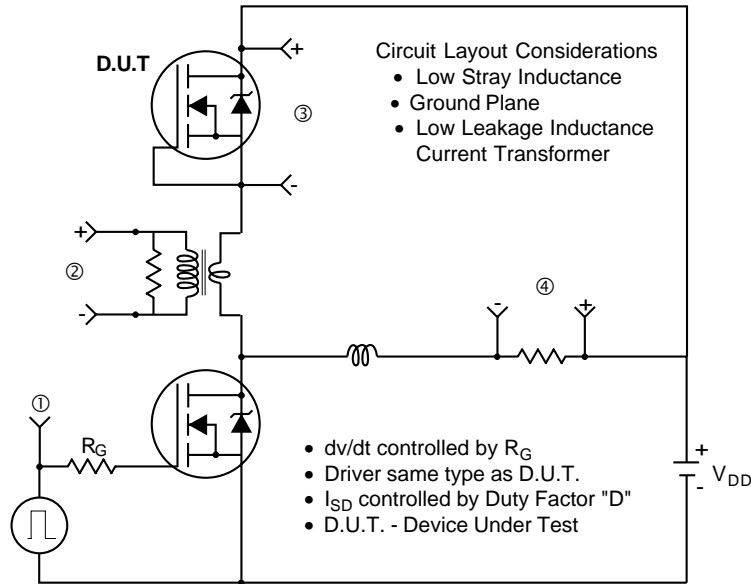


**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current



**Fig 13b.** Gate Charge Test Circuit

## Peak Diode Recovery dv/dt Test Circuit



\*  $V_{GS} = 5V$  for Logic Level Devices

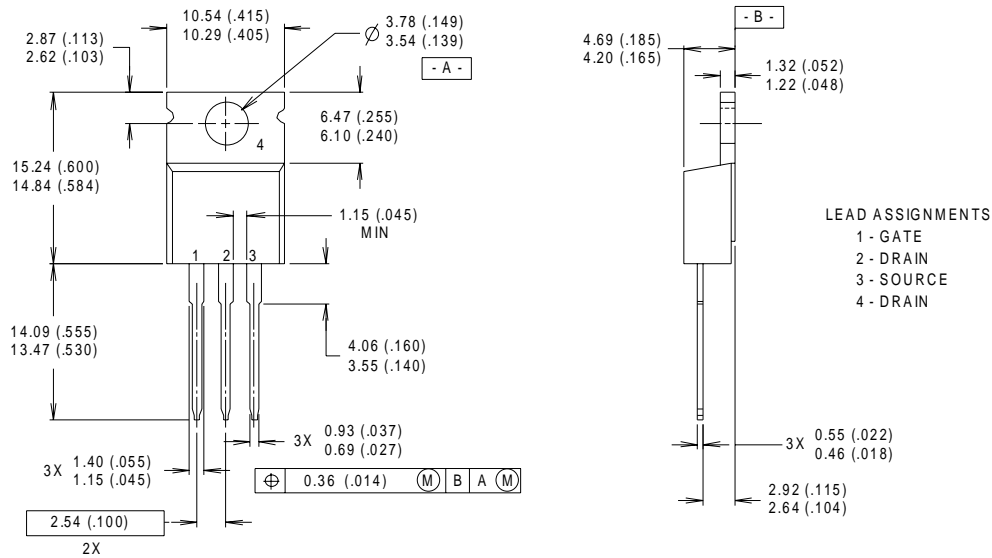
**Fig 14.** For N-Channel HEXFET® Power MOSFETs

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## TO-220AB Package Outline

Dimensions are shown in millimeters (inches)

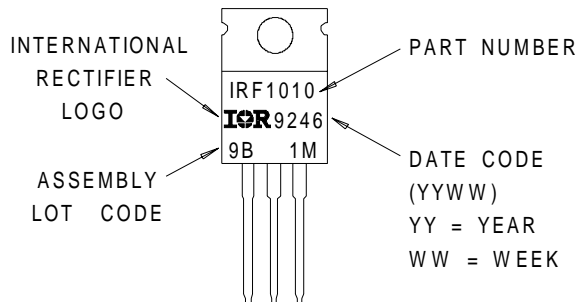


**NOTES:**

- 1 DIMENSIONING & TOLERANCING PER ANS Y14.5M, 1982.
- 2 CONTROLLING DIMENSION : INCH
- 3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
- 4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

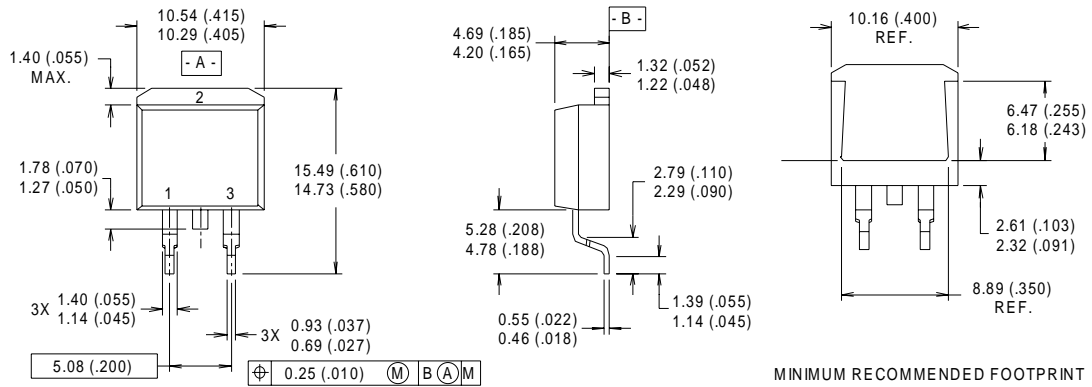
## TO-220AB Part Marking Information

EXAMPLE : THIS IS AN IRF1010  
 WITH ASSEMBLY  
 LOT CODE 9B1M





## D<sup>2</sup>Pak Package Outline



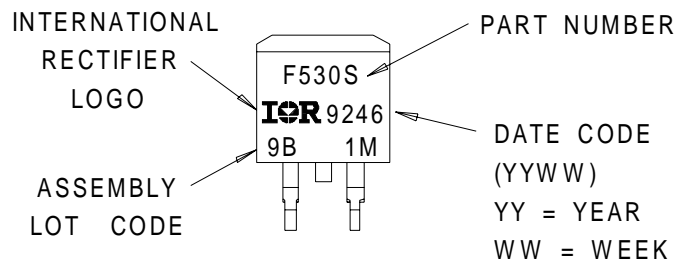
**NOTES:**

- 1 DIMENSIONS AFTER SOLDER DIP.
- 2 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 3 CONTROLLING DIMENSION : INCH.
- 4 HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

**LEAD ASSIGNMENTS**

- 1 - GATE
- 2 - DRAIN
- 3 - SOURCE

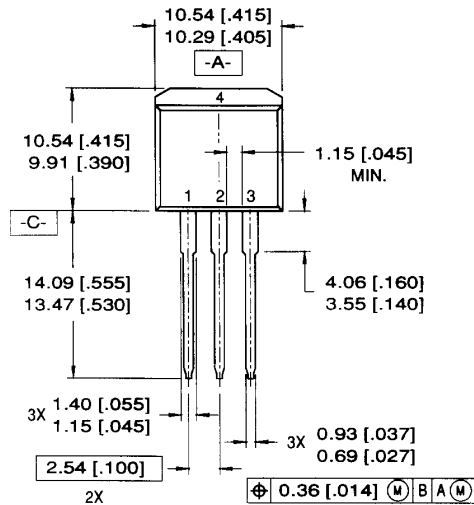
## D<sup>2</sup>Pak Part Marking Information



# IRL3714/3714S/3714L

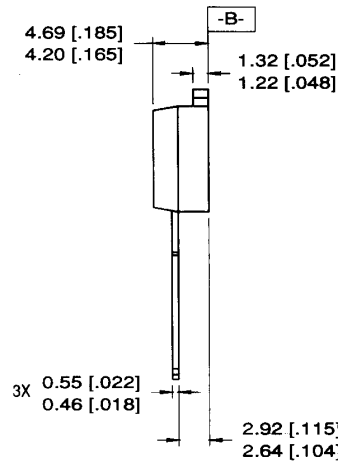
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## TO-262 Package Outline



### LEAD ASSIGNMENTS

1 = GATE      3 = SOURCE  
2 = DRAIN    4 = DRAIN

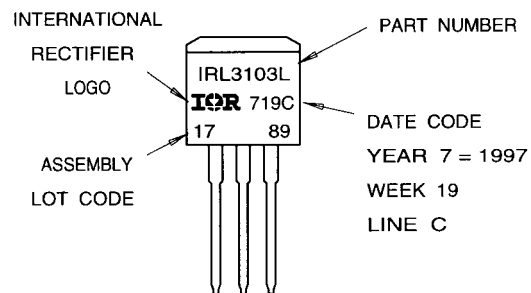


### NOTES:

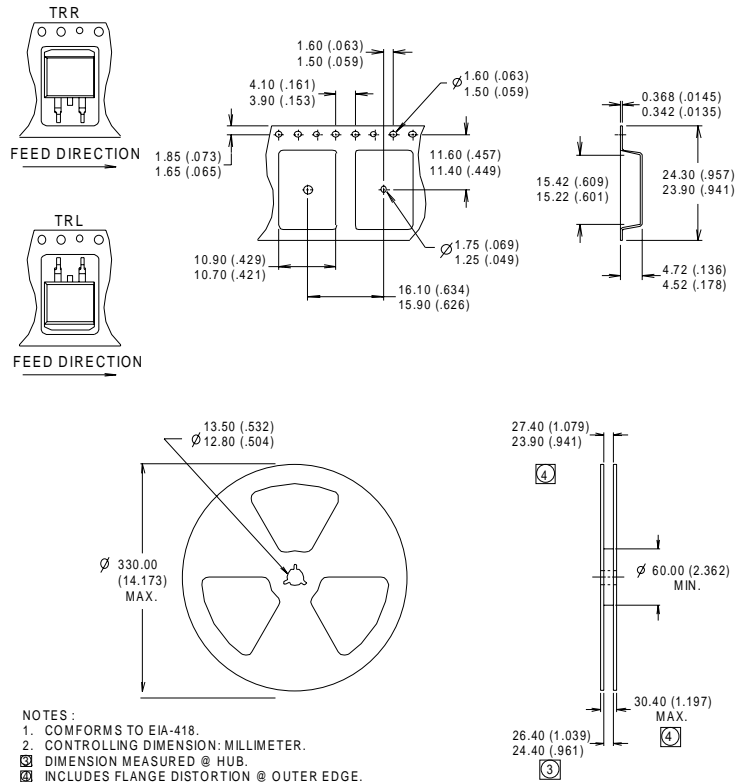
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

## TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L  
LOT CODE 1789  
ASSEMBLED ON WW 19, 1997  
IN THE ASSEMBLY LINE "C"



## D<sup>2</sup>Pak Tape & Reel Information



### Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.69\text{ mH}$   
 $R_G = 25\Omega$ ,  $I_{AS} = 14\text{A}$ .
- ③ Pulse width  $\leq 400\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- ④ This is only applied to TO-220AB package
- ⑤ This is applied to D<sup>2</sup>Pak, when mounted on 1" square PCB ( FR-4 or G-10 Material ).  
For recommended footprint and soldering techniques refer to application note #AN-994.

Data and specifications subject to change without notice.  
These products have been designed and qualified for the Industrial market.  
Qualification Standards can be found on IR's Web site.