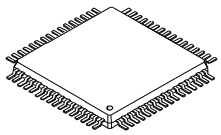
CD DIGITAL SERVO SIGNAL PROCESSOR(SLAVE MODE)

DESCRIPTION

The SC9645 is a digital signal processor LSI for CD players. This LSI incorporates a digital servo and 16bit audio DAC.



LQFP-64-10x10-0.5

FEATURES

* Supports 1X to 2X speed playback
* Servo command and Q-Code by CPU interface
* Controlled With multi-level command structure
* Supports format of CD-A/V, CD-R, CD-R/W and CD-ROM

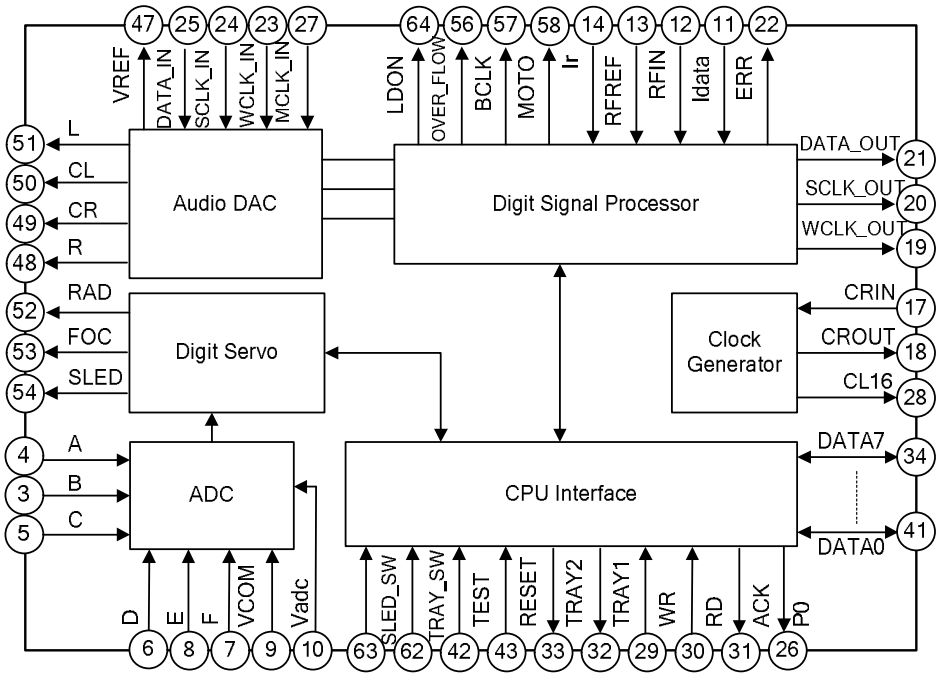
APPLICATIONS

* CD and VCD player
* Auto audio system

ORDERING INFORMATION

Device	Package
SC9645	LQFP-64-10X10-0.5

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Tamb=25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{DD}	-0.5 ~ +5.5	V
Input Voltage On Pins	V_{IN}	-0.5 ~ V_{DD} + 0.5	V
Operating Temperature	Tmax	-20 ~ +75	℃

ELECTRICAL CHARACTERISTICS（V_{DD}=3.4~5.5V;V_{SS}=0V;Tamb=-10~+60°C）

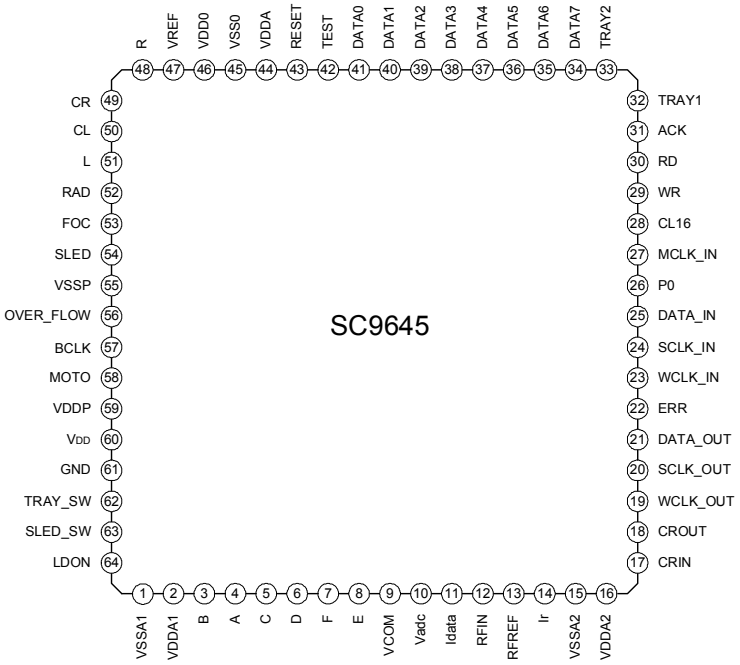
Characteristics	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Supply Voltage	V_{DD}		4.5	5.0	5.5	V
Supply Current	I_{DD}	5V；1X Speed	—	45	—	mA
RFIN Input Signal	V_{RFIN}		—	1.0	—	V
Reference Voltage	I_{Ir}		—	0.5V_{DD}	—	V
Common Mode DC	V_{VCOM}		2.0	2.5	—	V
Output ADC Reference Voltage	V_{Vadc}		V_{VCOM} +0.462	—	V_{VCOM} +2.313	V
Input Current Of Central Diode B	I_B		0	—	10	μA
Input Current Of Central Diode A	I_A		0	—	10	μA
Input Current Of Central diode C	I_C		0	—	10	μA
Input Current Of Central diode D	I_D		0	—	10	μA
Input Current Of Satellite Diode F	I_F		0	—	5	μA
Input Current Of Satellite Diode F	I_E		0	—	5	μA
Data Slicer Feed-back Current Output	I_{Idata}		1.9	—	5.5	μA
LDON Low Level Output Current	I_{LDON}		0	—	2	mA
ERR Output Current	I_{ERR}		0	1	—	mA
DATA_OUT WCLK_OUT SCLK_OUT Output Current	I_{OH1} I_{OL1}		0	1	—	mA
DATA_OUT WCLK_OUT SCLK_OUT Low Level Output Voltage	V_{OL1}	I_{OL1}=1mA	0	—	0.4	V
DATA_OUT WCLK_OUT SCLK_OUT High Level Output Voltage	V_{OH1}	I_{OH1}=-1mA	V_{DD}-0.4	—	V_{DD}	V
RAD Output Current	I_{RAD}		0	1	—	mA
FOC Output Current	I_{FOC}		0	1	—	mA

(To be continued)

(Continued)

Characteristics	Symbol	Test Condition	Min.	Typ.	Max.	Unit
SLED Output Current	I_{SLED}		0	1	—	mA
MOTO Output Current	I_{MOTO}		0	10	—	mA
RAD, FOC, SLED Low Level Output Voltage	V_{OL}	I_{OL}=1mA	0	—	0.4	V
RAD, FOC, SLED High Level Output Voltage	V_{OH}	I_{OH}=-1mA	V_{DD}-0.4	—	V_{DD}	V
Moto Low Level Output Voltage	V_{OLmoto}	I_{OLmoto}=10mA	0	—	1.0	V
Moto high Level Output Voltage	V_{OHmoto}	I_{OHmoto}=-10mA	V_{DD}-1	—	V_{DD}	V
RAD, FOC, SLED, MOTO Output 3-state Leakage Current	I_{ZO}		-10	0	+10	μA
ACK, WR, RD, DATA0～7, High Level Input Voltage	V_{iLH}		2.8	3.0	-	V
ACK, WR, RD, DATA0～7, Low Level Input Voltage	V_{iHL}		0.6	—	0.7	V
DATA_IN, WCLK_IN, SCLK_IN, High Level Input Voltage	V_{OHda}		0.7V_{DD}	—	V_{DD}+0.5	V
DATA_IN, WCLK_IN, SCLK_IN, Low Level Input Voltage	V_{OLda}		-0.5	—	0.3V_{DD}	V
DAC Total Harmonic Distortion Plus Noise	(THD+N)/S		60	65	70	dB
DA Filter Attenuation	Filter_DA	0~19 kHz	-	-	0.001	dB
		19~20 kHz	-	-	0.03	dB
		24KHz	25	-	-	dB
		25 ~ 35 KHz	40	-	-	dB
		35 ~ 64 KHz	50	-	-	dB
		64 ~68 KHz	31	-	-	dB
		68KHz	35	-	-	dB
		69~ 88KHz	40	-	-	dB
Crystal Frequency	f_{system}		—	16.9344	—	MHz
SCLK Frequency	f_{SCLK_IN}		—	2.8224	—	MHz
WCLK Frequency	f_{WCLK_IN}		—	44.1	—	KHz

PIN CONFIGURATION



PIN DESCRIPTION

Pin No	Symbol	Description
1	VSSA1	Analog Ground 1
2	VDDA1	Analog Supply 1
3	B	Central diode current signal input
4	A	Central diode current signal input
5	C	Central diode current signal input
6	D	Central diode current signal input
7	F	Satellite diode current signal input
8	E	Satellite diode current signal input
9	VCOM	DC voltage input
10	Vadc	ADC reference voltage output
11	Idata	Data Slicer feed-back current output
12	RFIN	EFM signal input
13	RFREF	Comparator common mode input
14	Ir	Reference current output
15	VSSA2	Analog Ground 2
16	VDDA2	Analog Supply 2
17	CRIN	Crystal oscillation circuit input. When the master clock is input externally, input it from this pin.
18	CROUT	Crystal oscillation circuit output.
19	WCLK_OUT	D/A interface. LR clock output. f = Fs
20	SCLK_OUT	D/A interface. Bit clock output.

(To be continued)

(Continued)

Pin NO.	Symbol	Description
21	DATA_OUT	D/A interface. Serial data output (two's complement, MSB first).
22	ERR	C2 error flag
23	WCLK_IN	D/A interface. LR clock input.
24	SCLK_IN	D/A interface. Bit clock input.
25	DATA_IN	D/A interface. Serial data input
26	P0	NC
27	MCLK_IN	DAC system clock input (16.9344MHZ)
28	CL16	16.9344MHZ clock output
29	WR	Write control signal I/O
30	RD	Read control signal I/O
31	ACK	Acknowledge Signal
32	TRAY1	Loading control output (+)
33	TRAY2	Loading control output (-)
34	DATA7	Microcontroller interface data 7 I/O pins.
35	DATA6	Microcontroller interface data 6 I/O pins.
36	DATA5	Microcontroller interface data 5 I/O pins.
37	DATA4	Microcontroller interface data 4 I/O pins.
38	DATA3	Microcontroller interface data 3 I/O pins.
39	DATA2	Microcontroller interface data 2 I/O pins.
40	DATA1	Microcontroller interface data 1 I/O pins.
41	DATA0	Microcontroller interface data 0 I/O pins.
42	TEST	Test enable
43	RESET	Reset signal input pin. At reset, “L”.
44	VDDA	Analog Supply
45	VSSO	Analog Ground
46	VDD0	Analog Supply
47	VREF	Internal reference voltage for output channels
48	R	Right channel output
49	CR	Capacitor for right channel 1st order filter function
50	CL	Capacitor for left channel 1st order filter function
51	L	Left channel output
52	RAD	Tracking drive output
53	FOC	Focus drive output
54	SLED	Sled drive output
55	VSSP	Ground
56	OVER_FLOW	Shock dectect signal output
57	BCLK	Subcode block clock
58	MOTO	Spindle drive output
59	VDDP	Digital Supply
60	VDD	Digital Supply
61	GND	Digital Ground
62	TRAY_SW	Loading position monitor signal input
63	SLED_SW	Sledge motor position monitor signal input
64	LDON	Laser control signal output

FUNCTION DESCRIPTION

The system controller set the mode and read back status of signal processor and digital servo by the standard CPU interface. The detail of command and interface timing is explained in following tables.

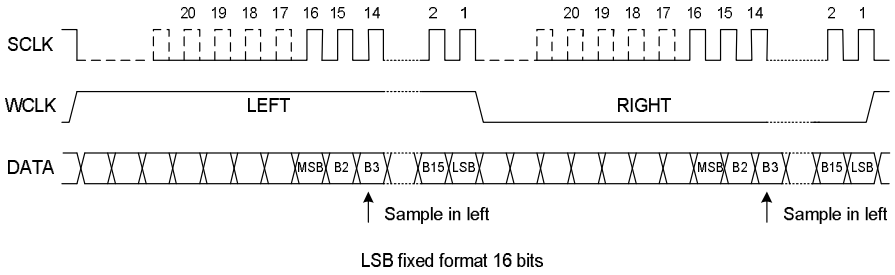
1. SYSTEM WRITE COMMAND TABLE:

Command (HEX)	Parameter(BIN)	FUNCTION DESCRIPTION
10	00000001	reset servo(SC9645 has power on reset)
	00000010	Stop all servo
	00000011	Start play
	00000100	Play pause
11	XXXXXXX0	set 1x speed play
	XXXXXXX1	set 2X speed play
	XXXXXX0X	close DAC interface output(CD format only)
	XXXXXX1X	open DAC interface output(CD format only)
	0000XXXX	set output format I2S; CD-ROM mode
11	0001XXXX	set output format EIAJ; CD-ROM mode
	0010XXXX	set output format I^2S; 18 Bits; $4F_S$ mode
	0011XXXX	set output format I^2S; 18 Bits; $2F_S$ mode
	0100XXXX	set output format I^2S; 16 Bits; F_S mode
	0101XXXX	set output format EIAJ; 16 Bits; $4F_S$ mode
	0110XXXX	set output format EIAJ; 16 Bits; $2F_S$ mode
	0111XXXX	set output format EIAJ; 16 Bits; F_S mode
	1000XXXX	set output format EIAJ; 18 Bits; $4F_S$ mode
	1001XXXX	set output format EIAJ; 18 Bits; $2F_S$ mode
	1010XXXX	set output format EIAJ; 18 Bits; F_S mode
20	00000100	Jump forward; Target jump track
	00000101	Jump back; Target jump track
	00000110	jump to target MSF (minute-second-frame) and play
2F	XXXXXXXX	Frame control
31	XXXXXXXX	Target minute
32	XXXXXXXX	Target second
33	XXXXXXXX	Target frame
34	XXXXXXXX	Target frame range
35	XXXXXXXX	Target jump trackH (HIGH 8 BIT)
36	XXXXXXXX	Target jump trackL (LOW 8 BIT)
40	00000001	Open Loading
	00010000	Close Loading
41	1001XXXX	Focus gain parameter I : FOC KP 90H~9FH
42	XXXXXXXX	Focus integration parameter: FOC INT 00H~FFH
47	XXXXXXXX	Focus gain parameter II : FOC GAIN 00H~FFH
4C	XXXXXXXX	Focus differential parameter: FOC KD: 80H~92H
4F	XXXXXXXX	Tracking gain parameter I : RAD KP 00H~0FH
50	XXXXXXXX	Tracking integration parameter : RAD INT 00H~FFH
53	XXXXXXXX	Tracking gain parameter I : RAD GAIN 00H~FFH
59	00000001	Default servo parameter initialization include command of 41H; 42H; 47H; 4CH; 4FH; 50H; 53H .

2. STATUS OUTPUT:

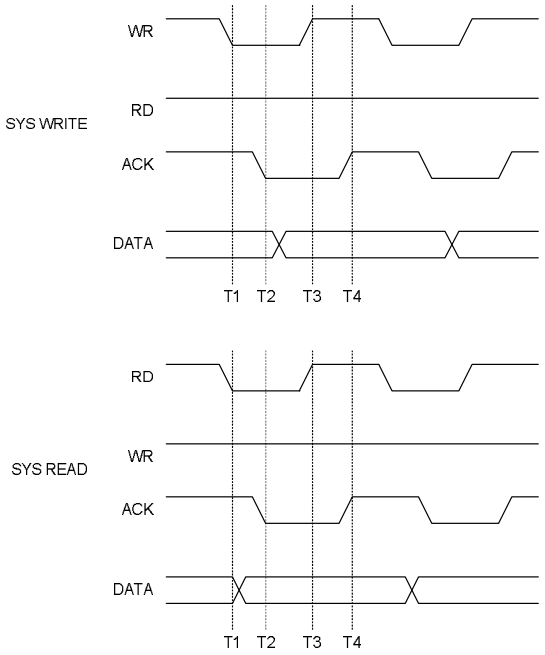
COMMAND (HEX)	STATUS PARAMETER	FUNCTION DESCRIPTION
80	QCODE0	CTRLADR(BCD)
81	QCODE1	TNO (BCD)
82	QCODE2	IX (BCD)
83	QCODE3	RMIN (BCD)
84	QCODE4	RSEC (BCD)
85	QCODE5	RFRAME (BCD)
86	QCODE6	ZERO (BCD)
87	QCODE7	AMIN (BCD)
88	QCODE8	ASEC (BCD)
89	QCODE9	AFRAME (BCD)
8A	QCODE0~9	10 byte Q-code
92	XXXXXXX1	QCODE OK=1, Q-CODE READY
	XXXXXXX0	QCODE OK=0, Q-CODE NOT READY
	XXXXXX1X	FOCUS LOST=1, Focus not ok
	XXXXXX0X	FOCUS LOST=0, Focus ok
	XXXXX1XX	GFS OK=1, Spindle motor CLV lock
	XXXXX0XX	GFS OK=0, Spindle motor CLV not lock
	XXXX1XXX	SEEK OK=1, get to target frame range
	XXXX0XXX	SEEK OK=0, not get to target frame range
	XXX1XXXX	NO DISC=1, no disc detected
	XXX0XXXX	NO DISC=0, disc detected
	X1XXXXXX	SEEK ERROR=1, can't get to starget point
	X0XXXXXX	SEEK ERROR=0, can get to target point
93	XXXXXXX1	SERVO RESET OK=1, servo reset OK
	XXXXXXX0	SERVO RESET OK=0, servo reset not complete
	XXXXXX1X	SERVO STOPED=1, servo stop
	XXXXXX0X	SERVO STOPED=0, servo not stop
	XXXXX1XX	SERVO PLAY=1, servo in play status
	XXXXX0XX	SERVO PLAY=0, servo not in play status
	XXXX1XXX	SERVO PAUSE=1, servo in pause status
	XXXX0XXX	SERVO PAUSE=0, servo not in pause status
	X1XXXXXX	TRAY OPENED=1, loading open
	X0XXXXXX	TRAY OPENED=0, loading not open
	1XXXXXXX	TRAY CLOSED=1, loading close
	0XXXXXXX	TRAY CLOSED=0, loading not close

3. DAC INTERFACE INPUT FORMAT：



LSB fixed format 16 bits

CPU INTERFACE TIMING



WR, RD are output from system CPU and ACK is output from SC9645 ,the default signal level is high and DATA bus can be used by system CPU and SC9645.

1) System CPU writes: in condition ACK is high.
   a. CPU sets WR low level at T1 to start writing.
   b. SC9645 sets acknowledge signal: ACK low level at T2.
   c. DATA bus is ready when WR is set from low to high at T3.
   d. SC9645 has finished reading data bus when signal ACK is set from low to high.
   e. One byte write is finished.
2) System CPU read: in condition ACK is high.
   a. CPU sets Rd from high to low at T1 to start reading.
   b. ACK is set from high to low at T2 when SC9645 is ready.
   c. DATA bus is ready when RD is set from low to high at T3.
   d. ACK is set from low to high at T4 by SC9645.
   e. One byte read is finished.

3) Timing :

a. system read：

T2-T1: >=7us

T3-T2: Typical 5us which is decided by system CPU.

T4-T3: >=6us

b. system write :

T2-T1: >=6us

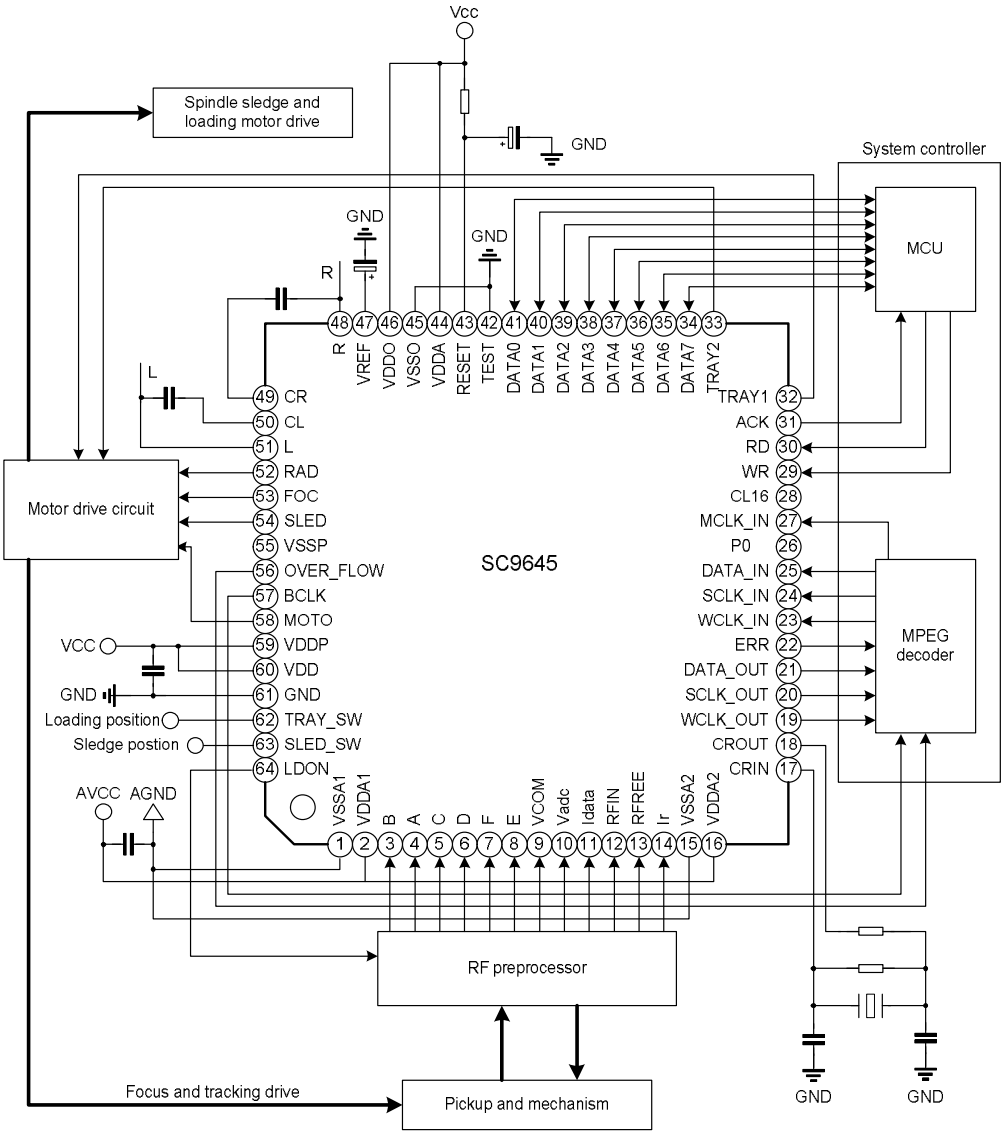
T3-T2: Typical 5us which is decided by system CPU.

T4-T3: >=4us

4) Timing limited

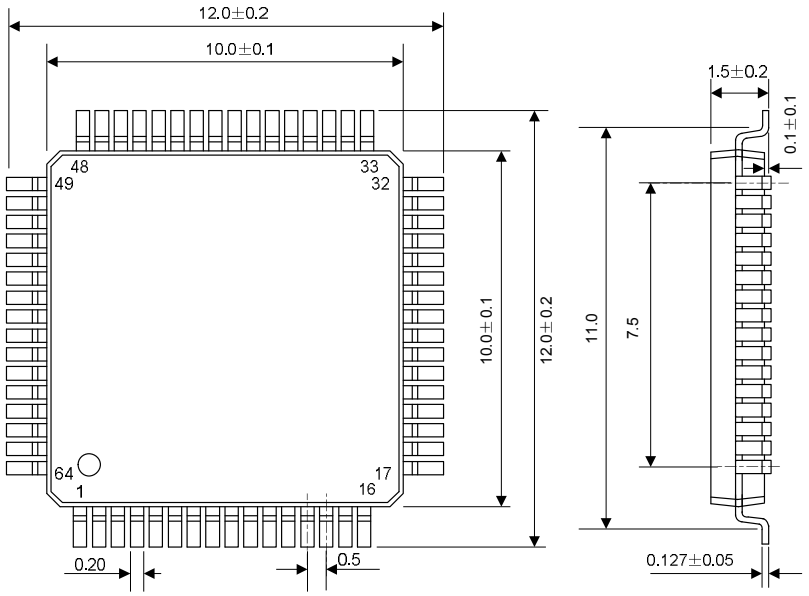
The maximum time between T3-T2 is 130us.

TYPICAL APPLICATION CIRCUIT



PACKAGE OUTLINE

LQFP-64-10x10-0.5 UNIT: mm



HANDLING MOS DEVICES:

Electrostatic charges can exist in many things. All of our MOS devices are internally protected against electrostatic discharge but they can be damaged if the following precautions are not taken:

- Persons at a work bench should be earthed via a wrist strap.
- Equipment cases should be earthed.
- All tools used during assembly, including soldering tools and solder baths, must be earthed.
- MOS devices should be packed for dispatch in antistatic/conductive containers.

Note: Silan reserves the right to make changes without notice in this specification for the improvement of the design and performance. Silan will supply the best possible product for customers.