

Bi-Directional P-Channel MOSFET/Power Switch

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
± 7	0.170 @ $V_{GS} = -4.5$ V	± 2.4
	0.240 @ $V_{GS} = -2.5$ V	± 2.0

FEATURES

- Low $r_{DS(on)}$ Symmetrical P-Channel MOSFET
- Integrated Body Bias For Bi-Directional Blocking
- 2.5- to 5.5-V Operation
- Exceeds ± 2 kV ESD Protected
- Solution for High-Side Battery Disconnect Switching (BDS)
- Supports Battery Switching in Multiple Battery Cell Phones, PDAs and PCS Products
- Low Profile, Small Footprint TSOP-6 Package

DESCRIPTION

The Si3831DV is a low on-resistance p-channel power MOSFET providing bi-directional blocking and conduction. Bi-directional blocking is facilitated by combining a 4-terminal symmetric p-channel MOSFET with a body bias selector circuit*. Circuit operation automatically biases the p-channel body to the most positive source/drain potential thereby maintaining a reverse bias across the diode present between the source/drain terminals. Off-state device blocking

characteristics are symmetric, facilitating bi-directional blocking for high-side battery switching in portable products. Gate drive is facilitated by negatively biasing the gate relative to the body potential. The off-state is achieved by biasing the gate to the most positive supply voltage or to the body potential. The Si3831DV is available in a 6-pin TSOP-6 package rated for the -25 to 85°C commercial temperature range.

APPLICATION CIRCUITS

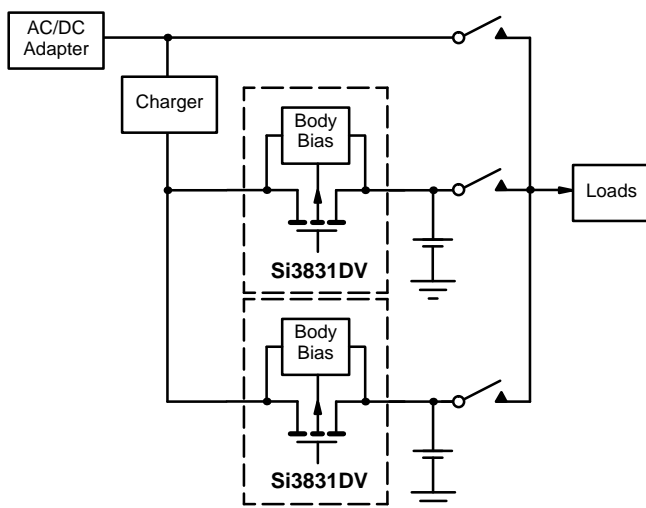


FIGURE 1. Charger Demultiplexing

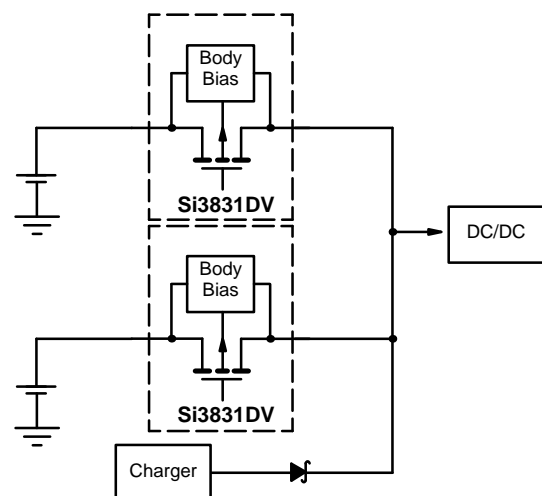


FIGURE 2. Battery Multiplexing (High-Side Switch)

*Patents pending.

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

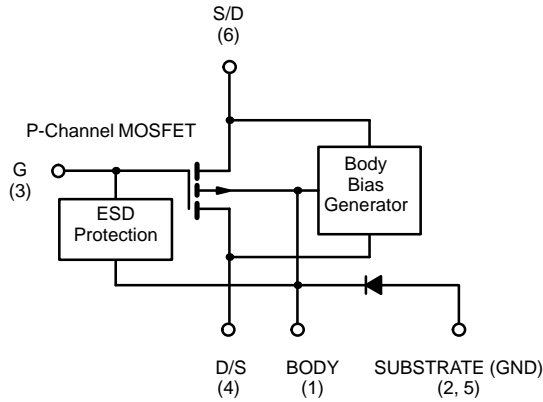


FIGURE 3.

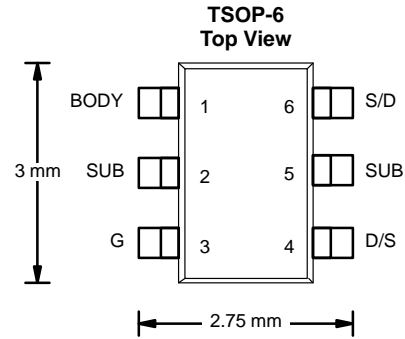


FIGURE 4.

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

Parameter	Symbol	Limit	Unit	
Drain-Source Voltage, Source-Drain Voltage ^a	V_{DS}	-7.0 to +7.0	V	
Source-Body/Drain-Body/Gate-Body Voltage	V_{SB}, V_{DB}, V_{GB}	0.3 to -7.0		
Body-Substrate Voltage	V_{BSUB}	+7.0 to -0.3		
Continuous Drain-to-Source Current ($T_J = 150^\circ\text{C}$) ^{a, b}	I_D	$T_A = 25^\circ\text{C}$	± 2.4	A
		$T_A = 70^\circ\text{C}$	± 2.0	
Pulsed Drain-to-Source Current ^a	I_{DM}	± 8		
Maximum Power Dissipation ^b	P_D	$T_A = 25^\circ\text{C}$	1.5	W
		$T_A = 70^\circ\text{C}$	1.0	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$	

RECOMMENDED OPERATING RANGE

Parameter	Symbol	Range	Unit
Drain-Source Voltage ^a	V_{DS}, V_{DS}	-5.5 to 5.5	V
Gate-Drain,/Gate-Source Voltage	V_{GD}, V_{GS}	0 to -5.5	
Source-Body/Drain-Body/Gate-Body Voltage	V_{SB}, V_{DB}, V_{GB}	0 to -5.5	
Drain-to-Source Current ^{a, b}	I_{DS}	± 2.4	A
Body-Source Current	I_{BS}	0 to 10	μA

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^b	R_{thJA}	80	$^\circ\text{C/W}$
		125	

Notes

- a. Bi-directional.
- b. Surface Mounted on FR4 Board, $t \leq 5$ sec.
- c. Surface Mounted on FR4 Board, Steady-State.

SPECIFICATIONS ($V_{BS} = 0\text{ V}$, $T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -250\ \mu\text{A}$	-0.4			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}$, $V_{GS} = -5.5\text{ V to }+0.3\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -5.5\text{ V}$, $V_{GS} = 0\text{ V}$, $V_{SB} = 0\text{ V}$			-1	μA
		$V_{DS} = -5.5\text{ V}$, $V_{GS} = 0\text{ V}$, $V_{SB} = 0\text{ V}$, $T_J = 70^\circ\text{C}$			-5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} = -3\text{ V}$, $V_{GS} = -4.5\text{ V}$	-8			A
		$V_{DS} = -3\text{ V}$, $V_{GS} = -2.5\text{ V}$	-3			
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = -4.5\text{ V}$, $I_D = -2.4\text{ A}$		0.130	0.170	Ω
		$V_{GS} = -2.5\text{ V}$, $I_D = -2.0\text{ A}$		0.180	0.240	
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = -5\text{ V}$, $V_{GS} = -4.5\text{ V}$, $I_D = -2.4\text{ A}$		2.0	4.0	nC
Gate-Source Charge	Q_{gs}			0.23		
Gate-Drain Charge	Q_{gd}			0.14		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -3\text{ V}$, $R_L = 3\ \Omega$ $I_D \approx -1.0\text{ A}$, $V_{GEN} = -4.5\text{ V}$, $R_G = 6\ \Omega$		12	25	ns
Rise Time	t_r			55	110	
Turn-Off Delay Time	$t_{d(off)}$			90	180	
Fall Time	t_f			85	170	

Notes

- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
- b. Guaranteed by design, not subject to production testing.

GATE BUFFER REFERENCE

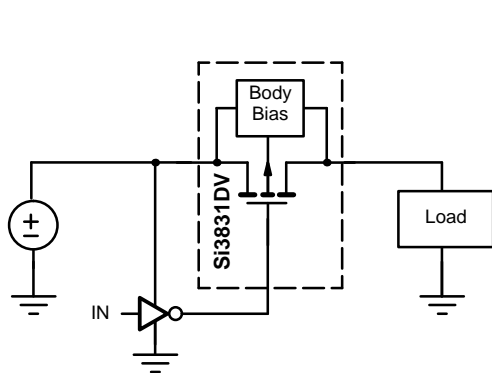


FIGURE 5. Gate Buffer Referenced to Most Positive Supply

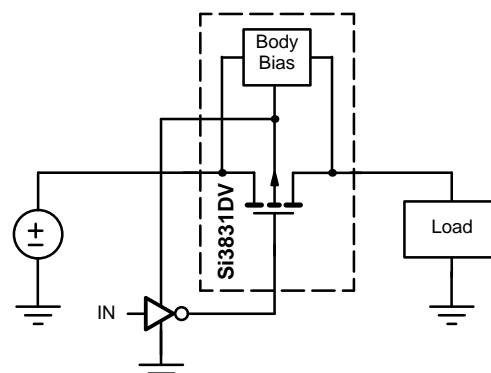
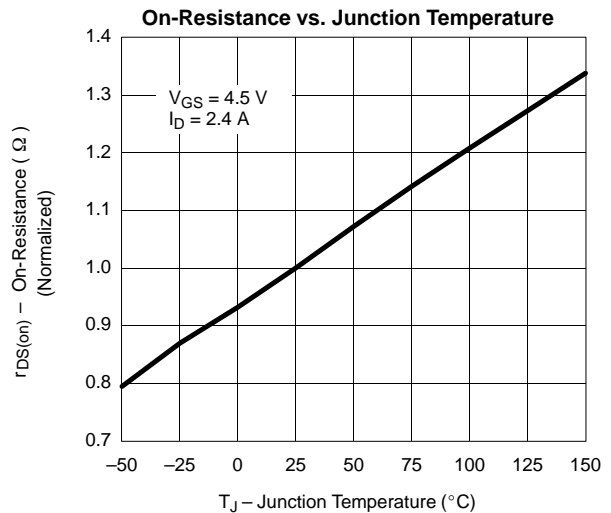
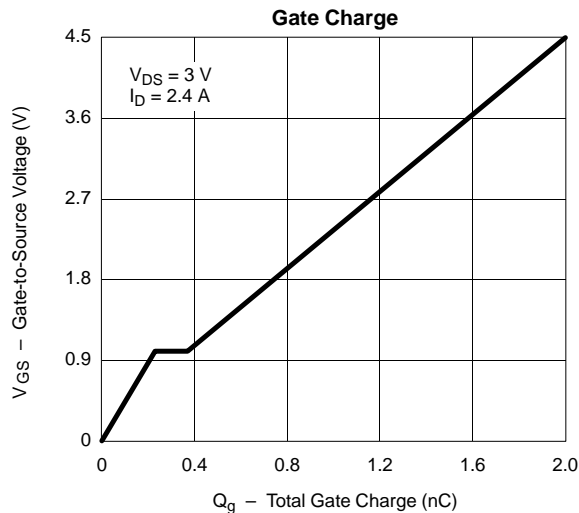
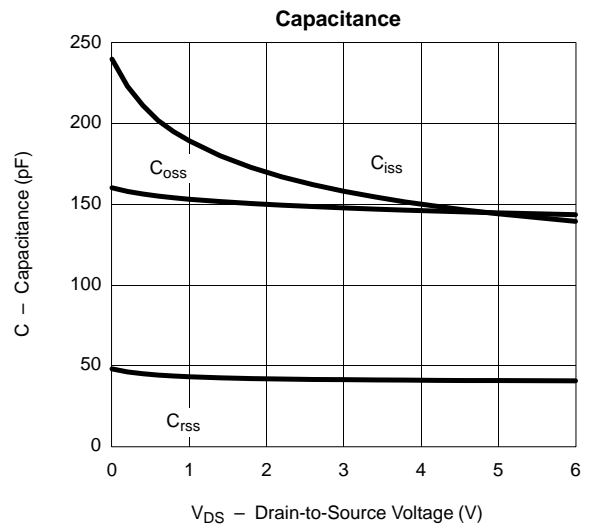
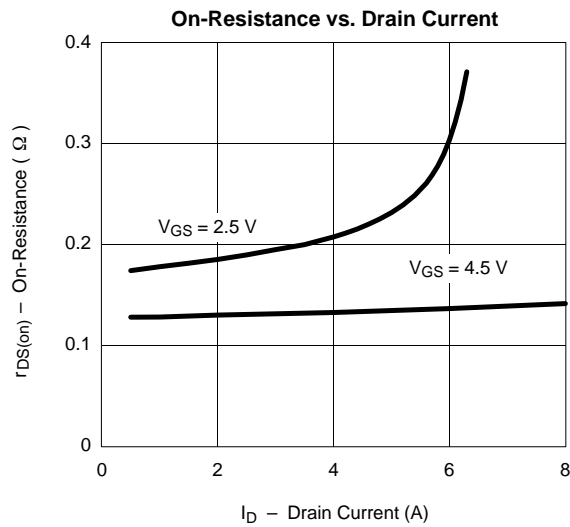
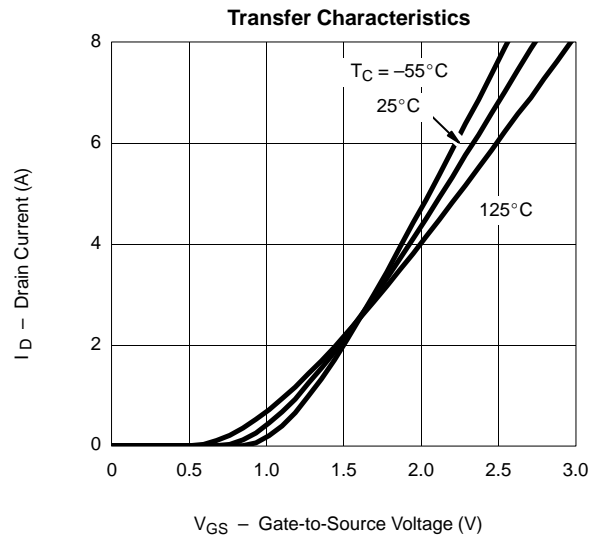
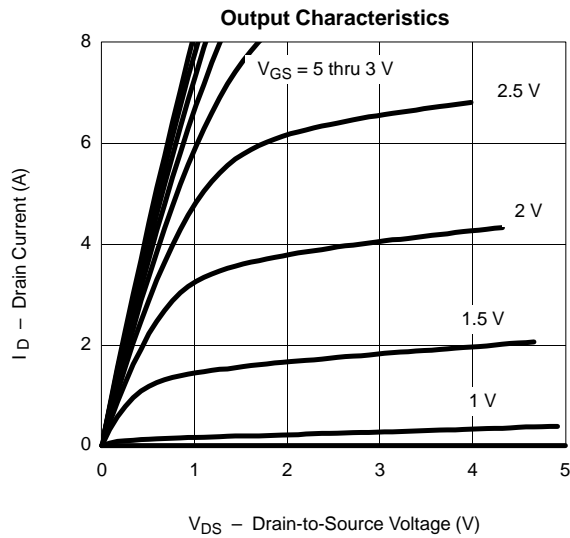
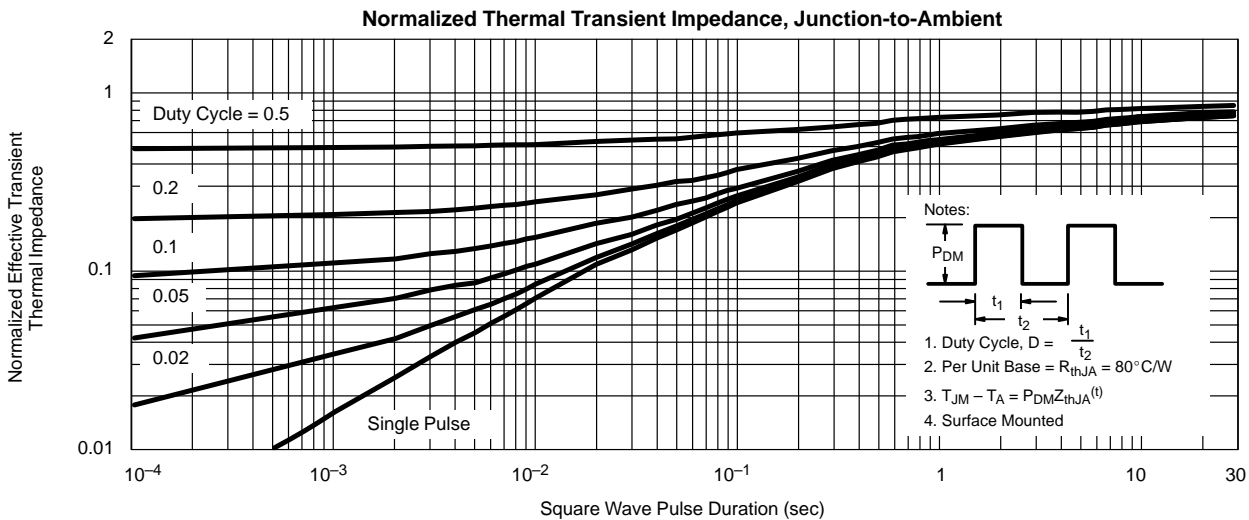
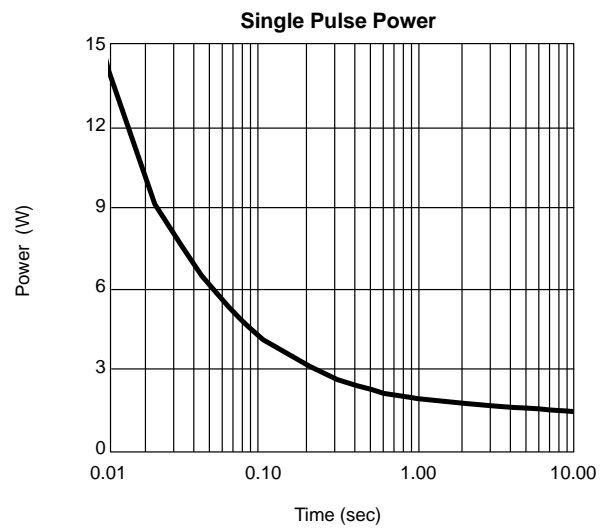
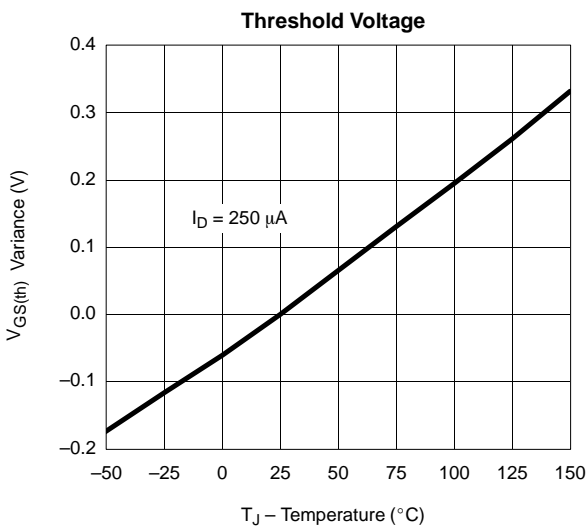
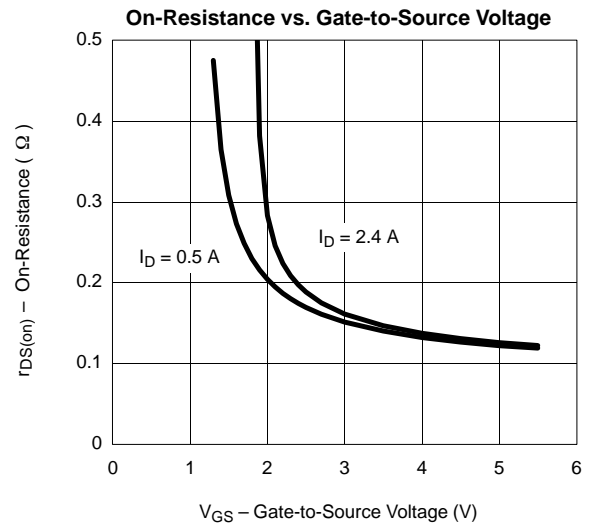
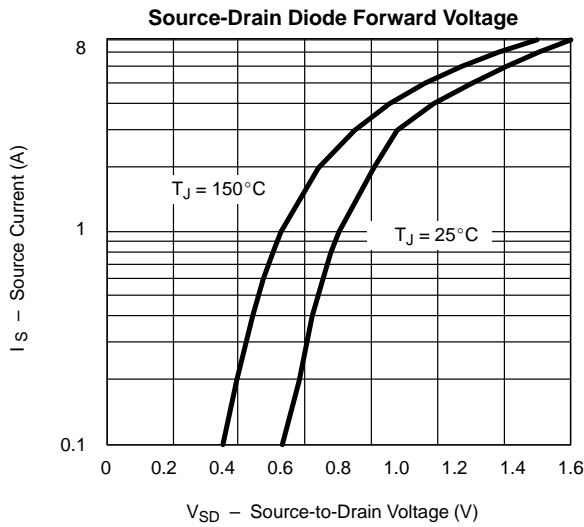


FIGURE 6. Gate Buffer Referenced to Body Bias Pin

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



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