MAS6270

IC FOR 6.50 – 40.00 MHz VCTCXO

This is preliminary information on a new product under development. Micro Analog Systems Oy reserves the right to make any changes without notice.

Preliminary

- **Min. Supply Voltage 2.6 V**
- **Max. Frequency 40 MHz**
- **True Sine Wave Output**
- **CMOS Output**
- **Frequency Stability ±2.0 ppm**
- **Suitable for Ultra Small VCTCXO**
- **Very Low Phase Noise**

DESCRIPTION

The MAS6270 is an integrated circuit well suited to build VCTCXO for mobile communication. Temperature calibration is achieved in three calibration temperatures only. The trimming is done through a serial bus and the calibration information is stored in an internal PROM.

To build a VCTCXO only a crystal is required in addition to MAS6270. The compensation method is fully analog, working continuously without generating any steps or other interference.
Output is either CMOS or a true sine wave resulting in lower harmonics than with clipped sine wave output.

FEATURES

- Very small size
- Minimum Vdd 2.6V
- No voltage reference capacitor needed
- Programmable VC-sensitivity
- Divider option selectable by a PROM bit
- Output waveform options: sine wave or CMOS
- Output peak voltage (amplitude) option selectable by a PROM bit in sine wave version

APPLICATIONS

- VCTCXO modules for mobile phones
- VCTCXO modules for other applications

BLOCK DIAGRAM

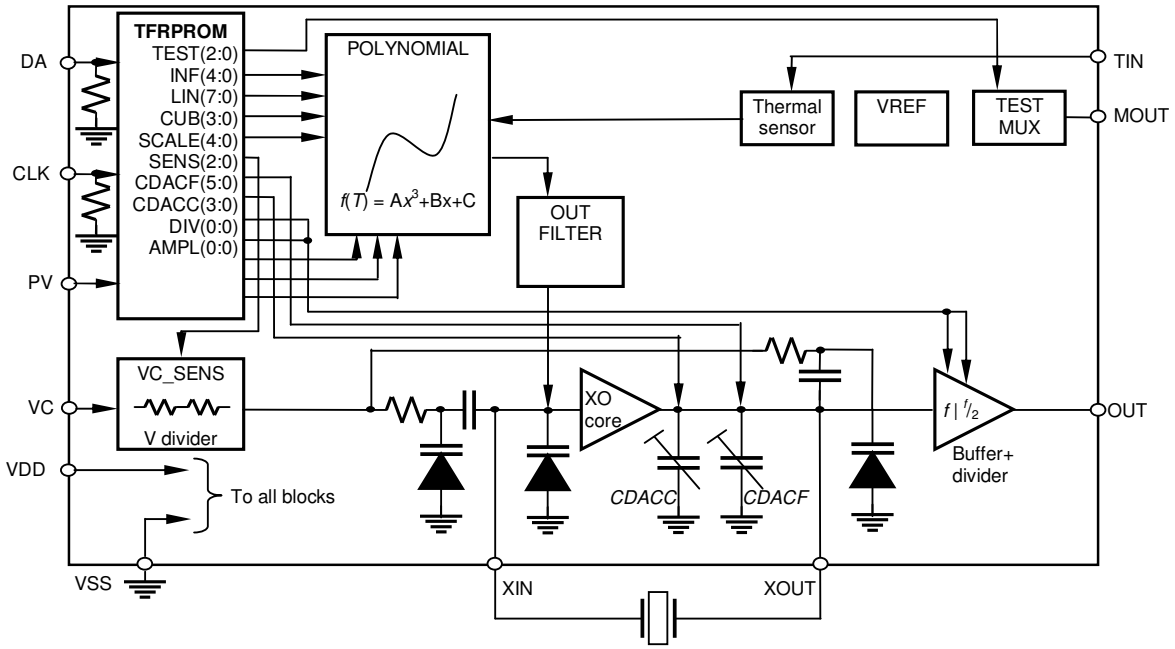


Figure 1. Block diagram of MAS6270.

PIN DESCRIPTION

Pin Description MAS6270A	Symbol	x-coordinate	y-coordinate
Test Multiplexer Output	MOUT	140	142
Temperature Input / Output	TIN	624	142
Serial Bus Data Input	DA	771	142
Serial Bus Clock Input	CLK	1083	142
Programming Input	PV	1256	140
Power Supply Voltage	VDD	1718	142
Voltage Control Input	VC	1687	1219
XO Output (crystal connection)	XOUT	1210	1219
XO Input (crystal connection)	XIN	848	1219
Power Supply Ground	VSS	495	1219
Buffered Output	OUT	134	1219

Note: Because the substrate of the die is internally connected to VSS, the die has to be connected to VSS or left floating. Please make sure that VSS is the first pad to be bonded. Pick-and-place and all component assembly are recommended to be performed in ESD protected area.
Note: Pad coordinates are measured from the left bottom corner of the chip to the center of the pads. The coordinates may vary depending on sawing width and location, however, distances between pads are accurate.
Note: Test Multiplexer Output is for testing only and must not be connected in an end user application.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit	Note
Supply Voltage	$V_{DD} - V_{SS}$	–0.3	6.0	V	
Input Voltage	V_{IN}	V_{SS} -0.3	V_{DD} + 0.3	V	1)
Power Dissipation	P_{MAX}		40	mW	2)
Storage Temperature	T_{ST}	–55	150	°C	
Latchup Current Limit	I_{LUT}	±100		mA	

Note: Stresses beyond the values listed may cause a permanent damage to the device. The device may not operate under these conditions, but it will not be destroyed.

Note: This is a CMOS device and therefore it should be handled carefully to avoid any damage by static voltages (ESD).

Note 1: Not valid for programming pin PV
Note 2: Value depends on a thermal resistance of the used package.

RECOMMENDED OPERATION CONDITIONS

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}		2.6	2.8	5.3	V	
Operating temperature	T_{OP}		–40		+85	°C	
Crystal load capacitance	C_L			8		pF	1)
Crystal pulling sensitivity	S		18		30	ppm/pF	
Crystal Rs	R_S			20	50	Ω	

Note 1: CDACF = 32 and CDACC = 8

ELECTRICAL CHARACTERISTICS

Parameter		Symbol	Min	Typ	Max	Unit	Note
Crystal frequency range		f_c	13.00		40.00	MHz	1)
Output frequency range		f_o	6.50		40.00	MHz	1)
Voltage control range		V_C	0	1.3	V_{DD}	V	
Voltage control sensitivity (SENS=7)		V_{CSENS}		10		ppm/V	2)
Frequency vs. supply voltage		df_o			±0.2	ppm	3) 8)
Frequency vs. load change		df_o			±0.2	ppm	4) 8)
Frequency vs. supply voltage		df_o			±0.2	ppm	3) 9)
Frequency vs. load change		df_o			±0.2	ppm	4) 9)
Output voltage (10 kΩ || 10 pF)		V_{out}	0.6	0.8/1.0		Vpp	5) 8)
Output voltage (10 kΩ || 10 pF)		V_{out}			V_{DD}	Vpp	9)
Rise and Fall Time (10 – 15 pF)				3		ns	9)
Duty Cycle			45		55	%	9)
Power Consumption		P			15	mW	7)
Harmonic Distortion				-25		dBc	8)
Supply current (Vdd = 2.8 V, f_c =26 MHz)		I_{DD}		1.8		mA	8)
Supply current (Vdd = 2.8 V, f_c =40 MHz)		I_{DD}		2.0		mA	8)
Supply current (Vdd = 2.8 V, f_c =26 MHz)		I_{DD}		TBD		mA	9)
Supply current (Vdd = 2.8 V, f_c =40 MHz)		I_{DD}		5.5		mA	9)
Compensation Range ±2.0 ppm		T_C	-30		85	°C	
Compensation Range ±2.5 ppm		T_C	-40		85	°C	
Compensation Range linear part		a1	-0.7		0.0	ppm/K	
Compensation Inflection Point		INF	20.5		36	°C	
Compensation Range Cubic Part		a3		95		ppm^2/K^3	
Amplitude Start up Time		T_{START}		2		ms	
Phase noise	@ 10Hz	φ_n			-90	dBc/Hz	6)
	@ 100Hz				-113		
	@ 1kHz				-136		
	@ 10kHz				-148		
	@ 100kHz				-155		

Note 1: Frequency division by two is selected by PROM bit DIV: 0=no division, 1=div by 2.
Thus IC output frequency range is 6.5 MHz – 40 MHz.
Note 2: Depending on a crystal pulling.
Note 3: V_{DD} ± 5%. DA must be high during measurement.
Note 4: R_L = 10 kΩ ± 10%, C = 10 pF ± 10%. DA must be in HIGH state during measurement.
Note 5: 0.8 V / 1.0 V output is selected by PROM bit AMPL: 0 = 0.8 Vpp, 1 = 1.0 Vpp, sine wave mode only.
Note 6: Not measured in production testing; guaranteed by design.
Note 7: Max power consumption is 15 mW when maximum V_{DD} is used.
Note 8: Sine wave output.
Note 9: CMOS output.

IC OUTLINE

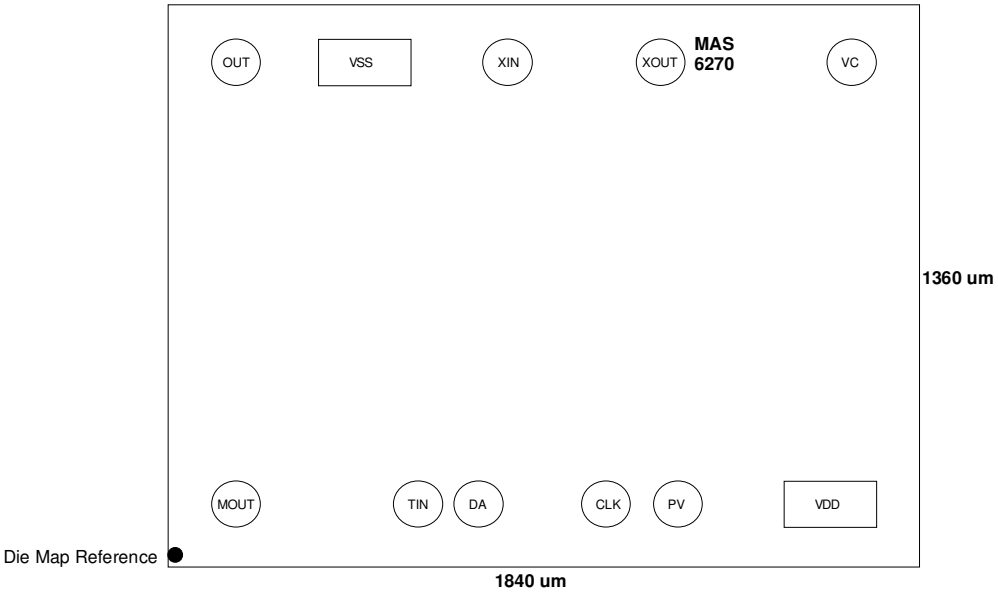


Figure 2. IC outlines.

Note 1: MAS6270 pads are round with 80 µm diameter at opening, except both VDD and VSS are rectangular 180 x 80 µm.
Note 2: Pins CLK, DA and PV can either be connected to VSS or left floating, and pin TIN must be left floating in VCTCXO module end-user application.
Note 3: Die map reference is the actual left bottom corner of the sawn chip.
Note 4: See coordinates in pin description on page 2.

SAMPLES IN SBDIL 20 PACKAGE

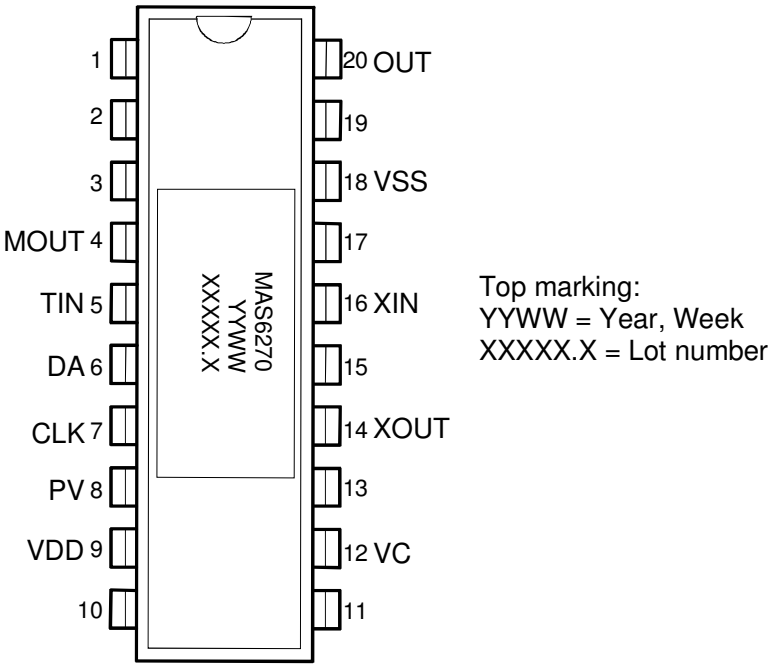


Figure 3. MAS6270 SBDIL-20 package.

DEVICE OUTLINE CONFIGURATION

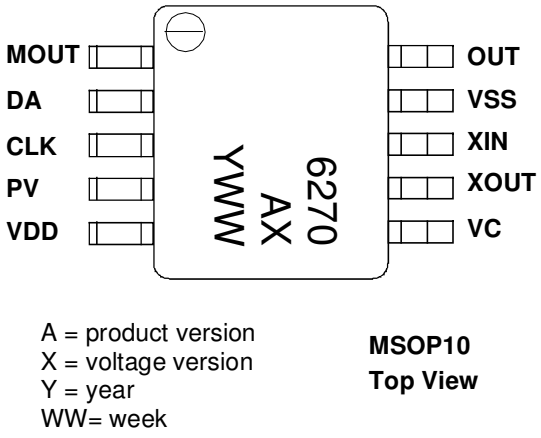
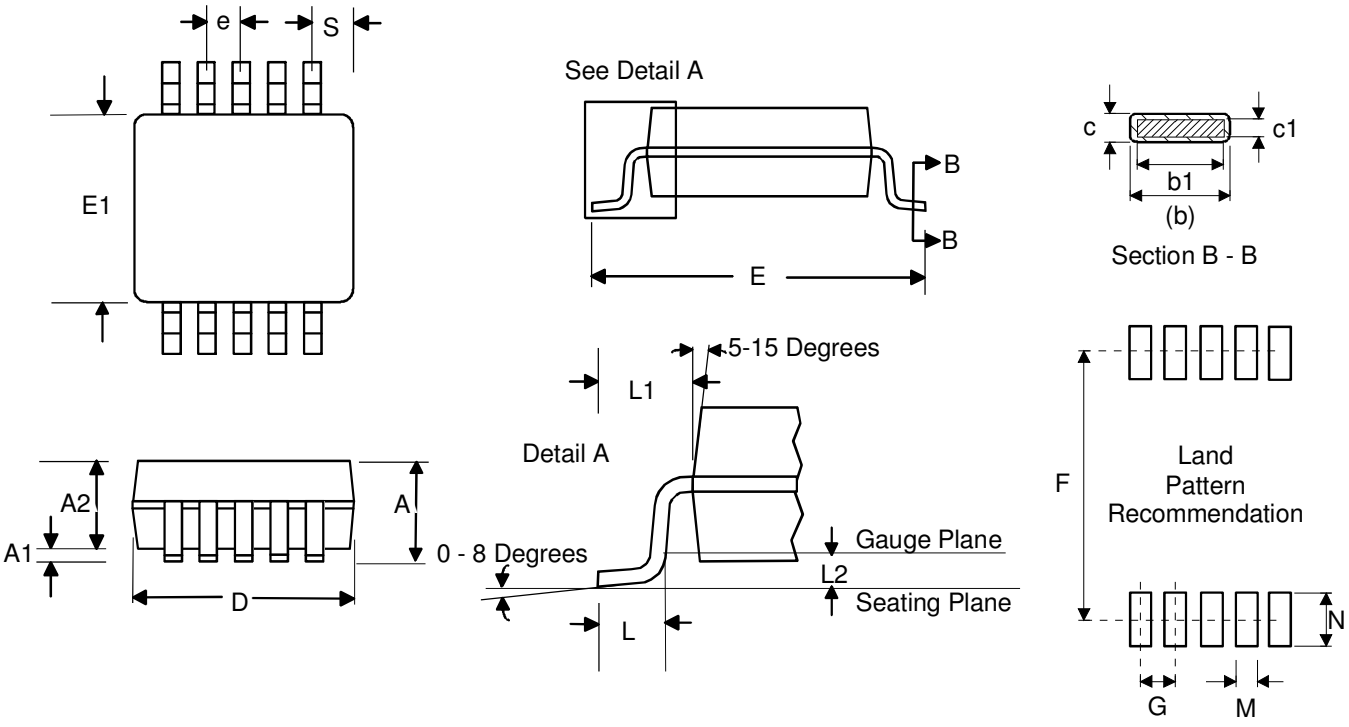


Figure 4. MAS6270 MSOP-10 package

PACKAGE (MSOP-10) OUTLINE



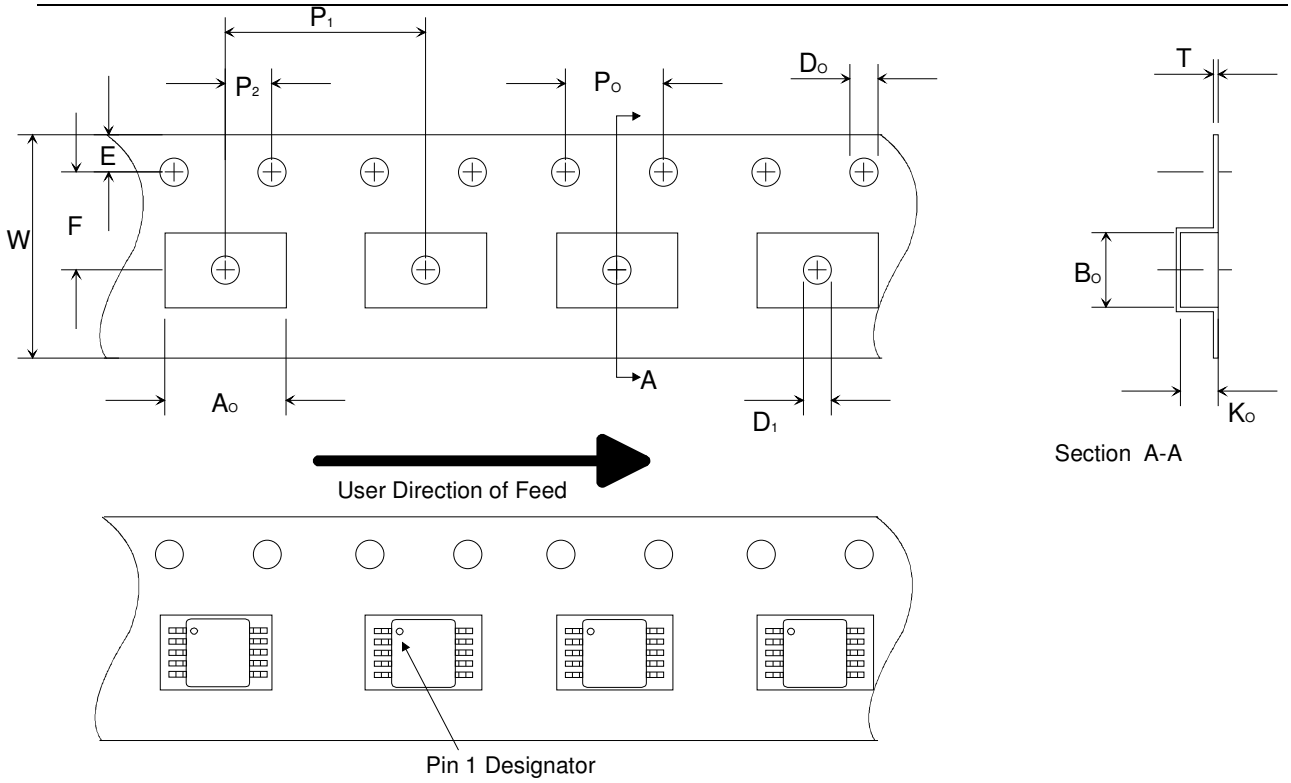
Symbol	Min	Nom	Max	Unit
A	--	--	1.10	mm
A1	0.00	--	0.15	mm
A2	0.75	0.85	0.95	mm
b	0.15	--	0.30	mm
b1	0.15	---	0.25	mm
c	0.08		0.23	mm
c1	0.08		0.18	mm
D		3.00 BSC		mm
E		4.90 BSC		mm
E1		3.00 BSC		mm
e		0.50 BSC		mm
F		4.8		mm
G		0.50		mm
L (Terminal length for soldering)	0.40	0.60	0.80	mm
L1		0.95 REF		
L2		0.25 BSC		mm
M		0.41		mm
N		1.02		mm
S		0.50		Mm

Dimensions do not include mold or interlead flash, protrusions or gate burrs.
Reference Standard : JEDEC MO-187 BA.

SOLDERING INFORMATION

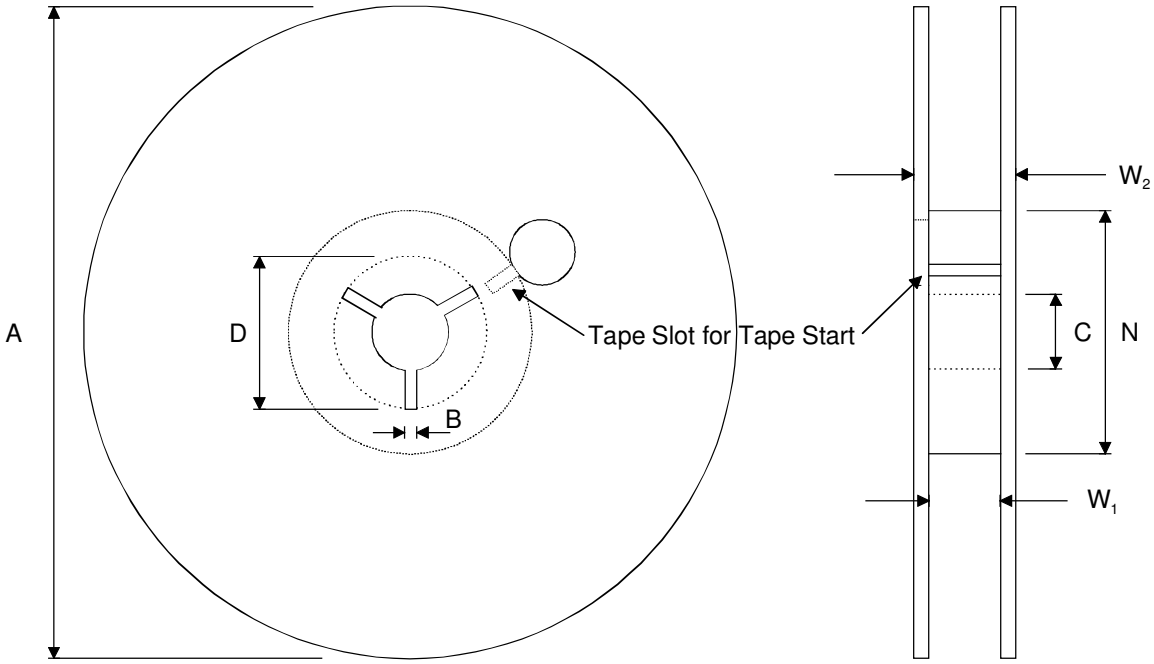
Resistance to Soldering Heat	According to RSH test IEC 68-2-58/20 2*220°C
Maximum Reflow Temperature	235°C
Maximum Number of Reflow Cycles	2
Seating Plane Co-planarity	max 0.08 mm
Lead Finish	Solder plate 7.62 - 25.4 µm, material Sn 85% Pb 15%

EMBOSSED TAPE SPECIFICATIONS



Dimension	Min/Max	Unit
Ao	5.00 ±0.10	mm
Bo	3.20 ±0.10	mm
Do	1.50 +0.1/-0.0	mm
D1	1.50 min	mm
E	1.75	mm
F	5.50 ±0.05	mm
Ko	1.45 ±0.10	mm
Po	4.0	mm
P1	8.0 ±0.10	mm
P2	2.0 ±0.05	mm
T	0.3 ±0.05	mm
W	12.00 +0.30/-0.10	mm

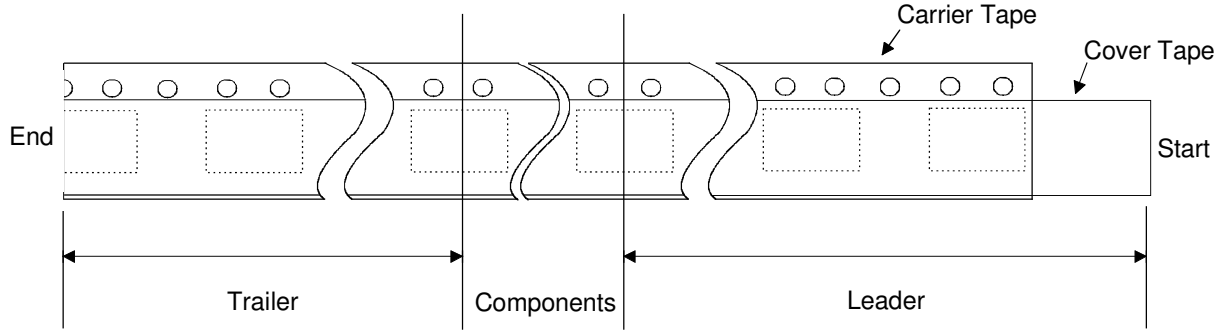
REEL SPECIFICATIONS



5000 Components on Each Reel

Reel Material: Conductive, Plastic Antistatic or Static Dissipative

Carrier Tape Material: Conductive



Dimension	Min	Max	Unit
A		330	mm
B	1.5		mm
C	12.80	13.50	mm
D	20.2		mm
N	50		mm
W_1 (measured at hub)	12.4	14.4	mm
W_2 (measured at hub)		18.4	mm
Trailer	160		mm
Leader	390, of which minimum 160 mm of empty carrier tape sealed with cover tape		mm
Weight		1500	g

ORDERING INFORMATION

Product Code	Product	Package	Comments
MAS6270AA1WA900	IC for 6.5MHz to 40MHz VCTCXO, sine wave output	EWS tested wafers 215 µm	Die Size 1.840 x 1.360 mm
MAS6270AB1WA900	IC for 6.5MHz to 40MHz VCTCXO, CMOS output	EWS tested wafers 215 µm	Die Size 1.840 x 1.360 mm
MAS6270AA1SM106	IC for 6.5MHz to 40MHz VCTCXO, sine wave output	MSOP-10	T&R 5000 pcs / r, Pb free RoHS
MAS6270AB1SM106	IC for 6.5MHz to 40MHz VCTCXO, CMOS output	MSOP-10	T&R 5000 pcs / r, Pb free RoHS

Contact Micro Analog Systems Oy for other wafer thickness options.

◆ **The formation of product code**

Product name	Design version	Package type	Delivery format
MAS6270	AA1 = sine wave output	WA9 = 215 µm thick EWS tested wafer	00 = bare wafer
	AB1 = CMOS output	SM1 = MSOP Pb free RoHS	06 = tape & reel

LOCAL DISTRIBUTOR

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