

# RF Power Field Effect Transistors

## N-Channel Enhancement-Mode Lateral MOSFETs

Designed for CDMA base station applications with frequencies from 1930 to 1990 MHz. Suitable for CDMA and multicarrier amplifier applications. To be used in Class AB and Class C for PCN-PCS/cellular radio applications.

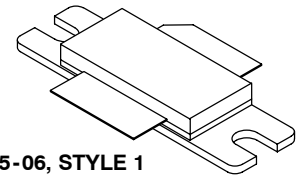
- Typical Single-Carrier W-CDMA Performance:  $V_{DD} = 28$  Volts,  $I_{DQ} = 1600$  mA,  $P_{out} = 56$  Watts Avg., Full Frequency Band, 3GPP Test Model 1, 64 DPCH with 50% Clipping, Channel Bandwidth = 3.84 MHz, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF.  
Power Gain — 17.9 dB  
Drain Efficiency — 29.5%  
Device Output Signal PAR — 5.9 dB @ 0.01% Probability on CCDF  
ACPR @ 5 MHz Offset — -36 dBc in 3.84 MHz Channel Bandwidth
- Capable of Handling 10:1 VSWR, @ 32 Vdc, 1960 MHz, 130 Watts CW Output Power

### Features

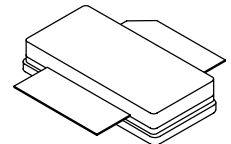
- 100% PAR Tested for Guaranteed Output Power Capability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Internally Matched for Ease of Use
- Integrated ESD Protection
- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- Optimized for Doherty Applications
- RoHS Compliant
- In Tape and Reel. R3 Suffix = 250 Units per 56 mm, 13 inch Reel.

**MRF6S19200HR3**  
**MRF6S19200HSR3**

**1930-1990 MHz, 56 W AVG., 28 V**  
**SINGLE W-CDMA**  
**LATERAL N-CHANNEL**  
**RF POWER MOSFETs**



**CASE 465-06, STYLE 1**  
**NI-780**  
**MRF6S19200HR3**



**CASE 465A-06, STYLE 1**  
**NI-780S**  
**MRF6S19200HSR3**

**Table 1. Maximum Ratings**

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DSS}$	-0.5, +66	Vdc
Gate-Source Voltage	$V_{GS}$	-6.0, +10	Vdc
Operating Voltage	$V_{DD}$	32, +0	Vdc
Storage Temperature Range	$T_{stg}$	-65 to +150	°C
Case Operating Temperature	$T_C$	150	°C
Operating Junction Temperature <sup>(1,2)</sup>	$T_J$	225	°C
CW Operation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	CW	130 0.49	W W/°C

**Table 2. Thermal Characteristics**

Characteristic	Symbol	Value <sup>(2,3)</sup>	Unit
Thermal Resistance, Junction to Case Case Temperature 110°C, 89 W CW Case Temperature 100°C, 55 W CW	$R_{\theta JC}$	0.35 0.36	°C/W

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at <http://www.freescale.com/rf>. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.freescale.com/rf>. Select Documentation/Application Notes - AN1955.

**Table 3. ESD Protection Characteristics**

Test Methodology	Class
Human Body Model (per JESD22-A114)	1B (Minimum)
Machine Model (per EIA/JESD22-A115)	A (Minimum)
Charge Device Model (per JESD22-C101)	IV (Minimum)

**Table 4. Electrical Characteristics** ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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**Off Characteristics**

Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 66 \text{ Vdc}$ , $V_{GS} = 0 \text{ Vdc}$ )	$I_{DSS}$	—	—	10	$\mu\text{Adc}$
Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 28 \text{ Vdc}$ , $V_{GS} = 0 \text{ Vdc}$ )	$I_{DSS}$	—	—	1	$\mu\text{Adc}$
Gate-Source Leakage Current ( $V_{GS} = 5 \text{ Vdc}$ , $V_{DS} = 0 \text{ Vdc}$ )	$I_{GSS}$	—	—	10	$\mu\text{Adc}$

**On Characteristics**

Gate Threshold Voltage ( $V_{DS} = 10 \text{ Vdc}$ , $I_D = 372 \mu\text{Adc}$ )	$V_{GS(th)}$	1	2	3	Vdc
Gate Quiescent Voltage ( $V_{DD} = 28 \text{ Vdc}$ , $I_D = 1600 \text{ mAdc}$ , Measured in Functional Test)	$V_{GS(Q)}$	2	3	4	Vdc
Drain-Source On-Voltage ( $V_{GS} = 10 \text{ Vdc}$ , $I_D = 3.71 \text{ Adc}$ )	$V_{DS(on)}$	0.1	0.2	0.3	Vdc

**Dynamic Characteristics** <sup>(1)</sup>

Reverse Transfer Capacitance ( $V_{DS} = 28 \text{ Vdc} \pm 30 \text{ mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0 \text{ Vdc}$ )	$C_{rss}$	—	2.3	—	pF
Output Capacitance ( $V_{DS} = 28 \text{ Vdc} \pm 30 \text{ mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0 \text{ Vdc}$ )	$C_{oss}$	—	185	—	pF
Input Capacitance ( $V_{DS} = 28 \text{ Vdc}$ , $V_{GS} = 0 \text{ Vdc} \pm 30 \text{ mV(rms)ac}$ @ 1 MHz)	$C_{iss}$	—	503	—	pF

**Functional Tests** (In Freescale Test Fixture, 50 ohm system)  $V_{DD} = 28 \text{ Vdc}$ ,  $I_{DQ} = 1600 \text{ mA}$ ,  $P_{out} = 56 \text{ W Avg.}$ ,  $f = 1932.5 \text{ MHz}$  and  $f = 1987.5 \text{ MHz}$ , Single-Carrier W-CDMA, 3GPP Test Model 1, 64 DPCH, 50% Clipping, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @  $\pm 5 \text{ MHz}$  Offset.

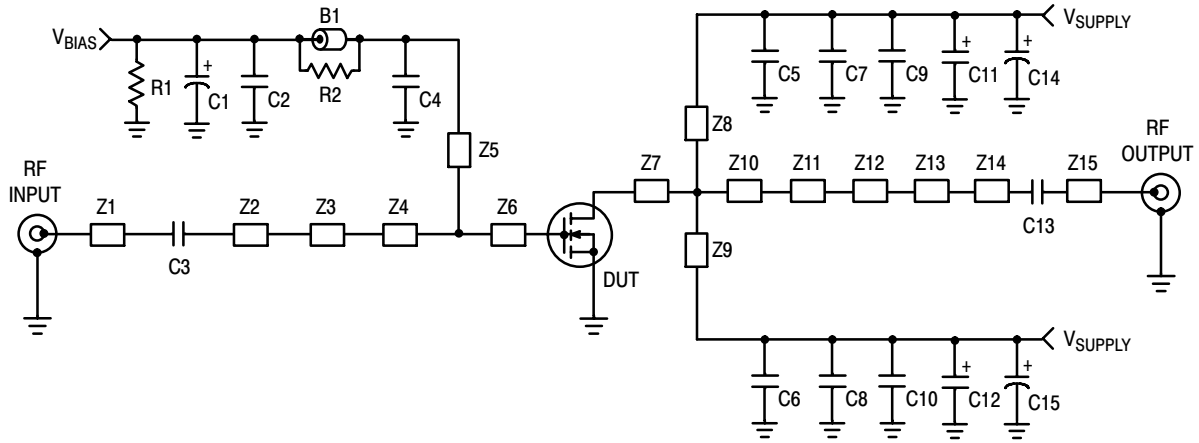
Power Gain	$G_{ps}$	15	17.9	19	dB
Drain Efficiency	$\eta_D$	26	29.5	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	5.5	5.9	—	dB
Adjacent Channel Power Ratio	ACPR	—	-36	-34	dBc
Input Return Loss	IRL	—	-14	-8	dB

1. Part internally matched both on input and output.

(continued)

**Table 4. Electrical Characteristics** ( $T_C = 25^\circ\text{C}$  unless otherwise noted) (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>Typical Performances</b> (In Freescale Test Fixture, 50 ohm system) $V_{DD} = 28\text{ Vdc}$ , $I_{DQ} = 1600\text{ mA}$ , 1930-1990 MHz Bandwidth					
IMD Symmetry @ 130 W PEP, $P_{out}$ where IMD Third Order Intermodulation $\cong 30\text{ dBc}$ (Delta IMD Third Order Intermodulation between Upper and Lower Sidebands $> 2\text{ dB}$ )	$IMD_{sym}$	—	20	—	MHz
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	$VBW_{res}$	—	50	—	MHz
Gain Flatness in 60 MHz Bandwidth @ $P_{out} = 56\text{ W Avg.}$	$G_F$	—	0.6	—	dB
Average Deviation from Linear Phase in 60 MHz Bandwidth @ $P_{out} = 130\text{ W CW}$	$\Phi$	—	1.94	—	$^\circ$
Average Group Delay @ $P_{out} = 130\text{ W CW}$ , $f = 1960\text{ MHz}$	Delay	—	2.44	—	ns
Part-to-Part Insertion Phase Variation @ $P_{out} = 130\text{ W CW}$ , $f = 1960\text{ MHz}$ , Six Sigma Window	$\Delta\Phi$	—	59.4	—	$^\circ$
Gain Variation over Temperature ( $-30^\circ\text{C}$ to $+85^\circ\text{C}$ )	$\Delta G$	—	0.04	—	dB/ $^\circ\text{C}$



Z1	0.859" x 0.084" Microstrip	Z10	0.547" x 1.203" Microstrip
Z2	0.470" x 0.084" Microstrip	Z11	0.119" x 0.755" Microstrip
Z3	0.362" x 0.244" Microstrip	Z12	0.222" x 0.365" Microstrip
Z4	0.145" x 1.040" Microstrip	Z13	0.225" x 0.220" Microstrip
Z5	0.040" x 0.257" Microstrip	Z14	0.192" x 0.084" Microstrip
Z6	0.418" x 1.040" Microstrip	Z15	0.843" x 0.084" Microstrip
Z7	0.103" x 1.203" Microstrip	PCB	Arlon CuClad 250GX-0300-55-22, 0.030", $\epsilon_r = 2.55$
Z8, Z9	0.198" x 0.160" Microstrip		

**Figure 1. MRF6S19200HR3(HSR3) Test Circuit Schematic**

**Table 5. MRF6S19200HR3(HSR3) Test Circuit Component Designations and Values**

Part	Description	Part Number	Manufacturer
B1	Short Ferrite Bead	2743019447	Fair Rite
C1	10 $\mu$ F, 50 V Electrolytic Capacitor	EMVY500ADA100MF55G	Nippon Chemi-Con
C2, C9, C10	0.1 $\mu$ F, 100 V Capacitors	CDR33BX104AKYS	Kemet
C3, C13	33 pF Chip Capacitors	ATC100B330JT500XT	ATC
C4, C5, C6	10 pF Chip Capacitors	ATC100B100CT500XT	ATC
C7, C8	10 $\mu$ F, 50 V Capacitors	GRMSSDRG1H106KA88B	Murata
C11, C12	22 $\mu$ F, 35 V Tantalum Capacitors	T491X226K035AT	Kemet
C14, C15	22 $\mu$ F, 50 V Electrolytic Capacitors	EMVY500ADA220MF55G	Nippon Chemi-Con
R1	1000 $\Omega$ , 1/4 W Chip Resistor	CRCW12061001FKEA	Vishay
R2	10 $\Omega$ , 1/4 W Chip Resistor	CRCW120610R1FKEA	Vishay

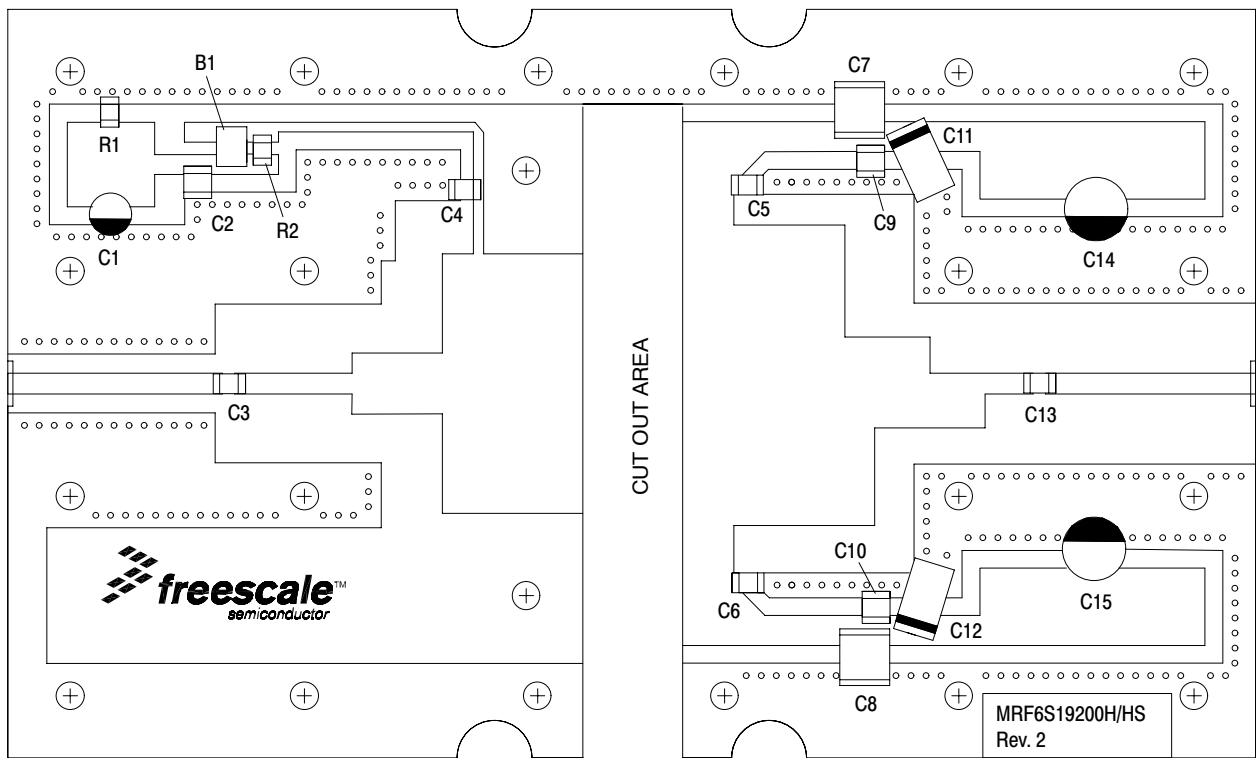
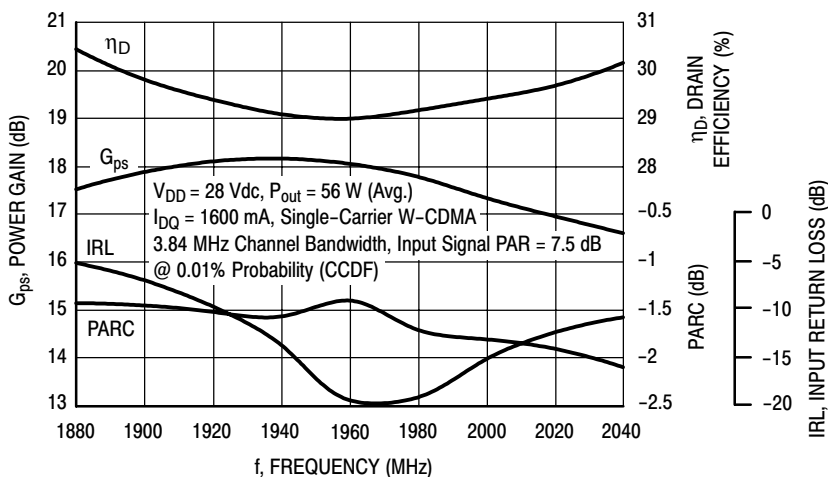
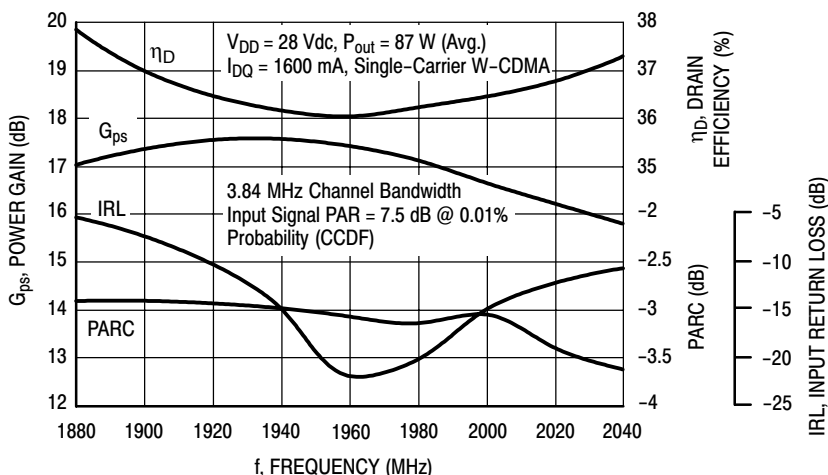


Figure 2. MRF6S19200HR3(HSR3) Test Circuit Component Layout

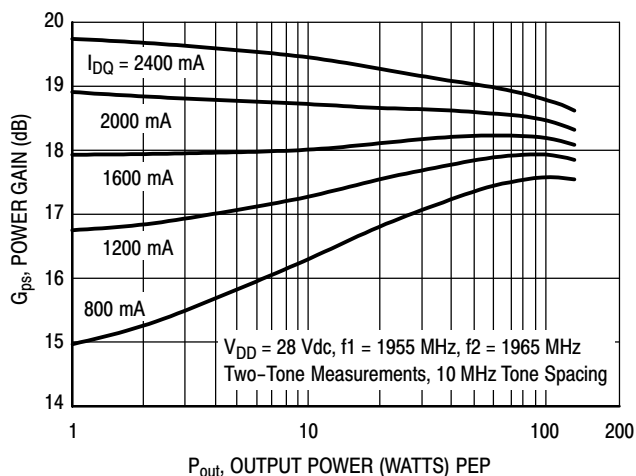
## TYPICAL CHARACTERISTICS



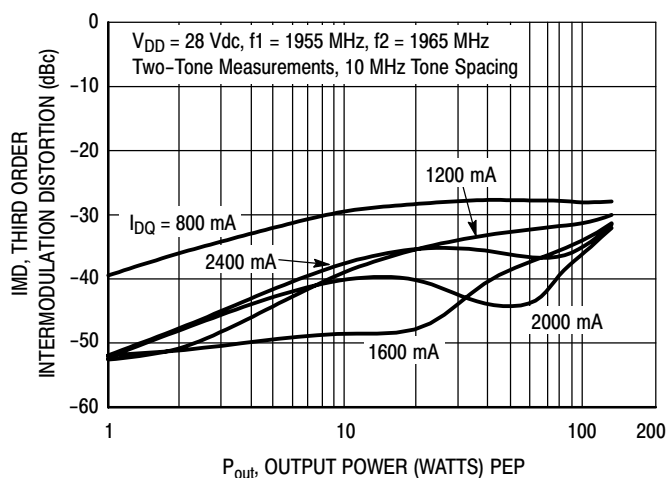
**Figure 3. Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @  $P_{out} = 56$  Watts Avg.**



**Figure 4. Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @  $P_{out} = 87$  Watts Avg.**



**Figure 5. Two-Tone Power Gain versus Output Power**



**Figure 6. Third Order Intermodulation Distortion versus Output Power**

## TYPICAL CHARACTERISTICS

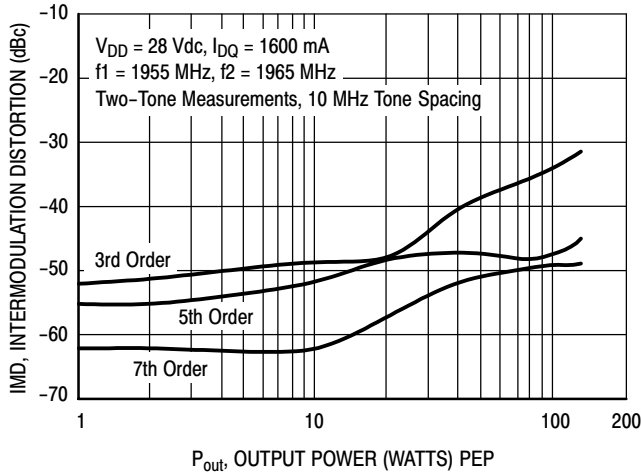


Figure 7. Intermodulation Distortion Products versus Output Power

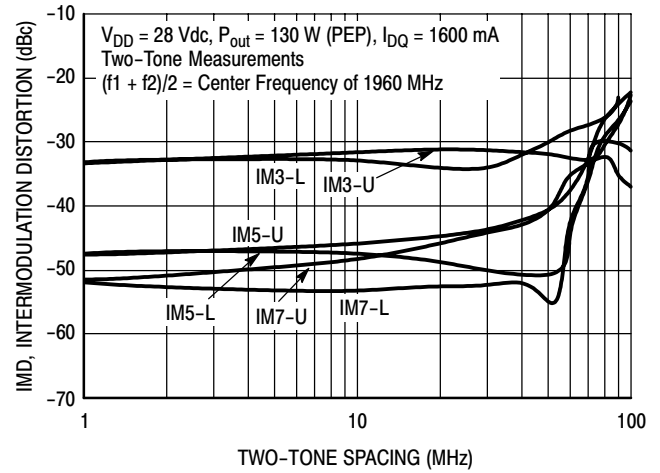


Figure 8. Intermodulation Distortion Products versus Tone Spacing

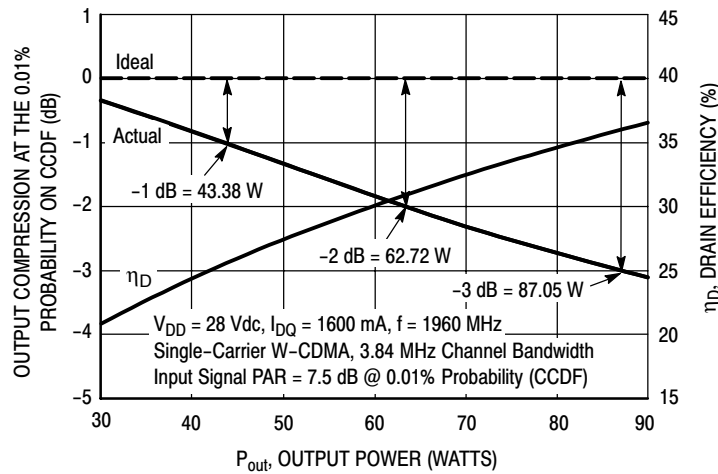


Figure 9. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

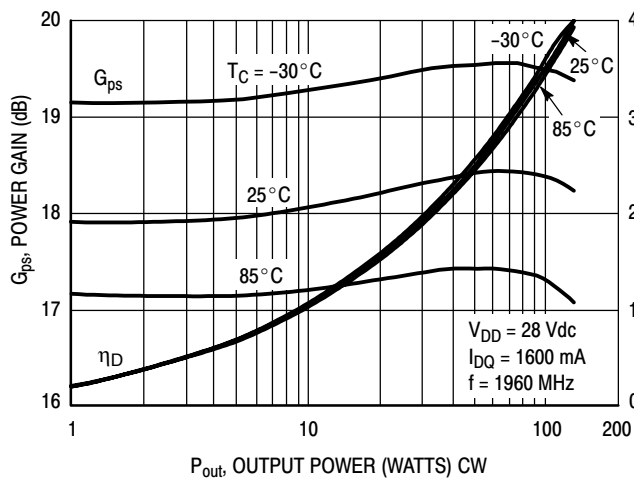


Figure 10. Power Gain and Drain Efficiency versus CW Output Power

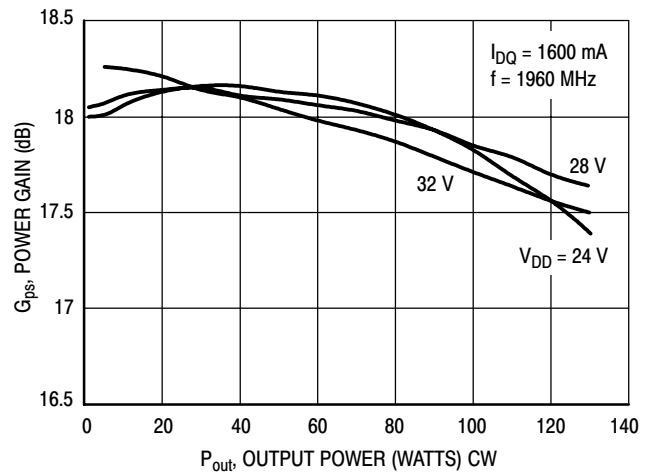
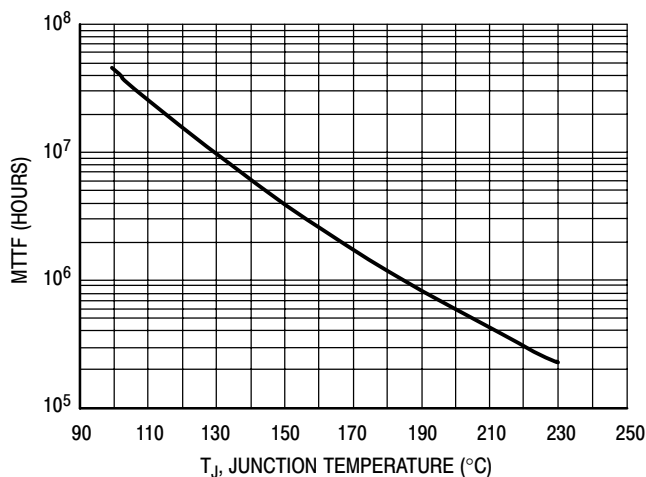


Figure 11. Power Gain versus Output Power

## TYPICAL CHARACTERISTICS

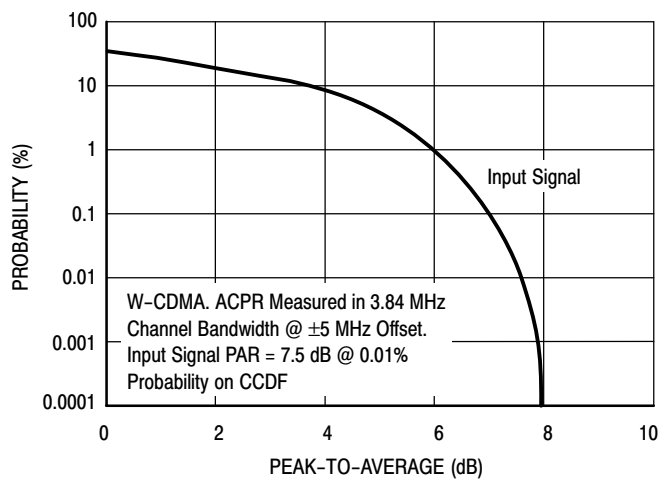


This above graph displays calculated MTTF in hours when the device is operated at  $V_{DD} = 28$  Vdc,  $P_{out} = 56$  W Avg., and  $\eta_D = 29.5\%$ .

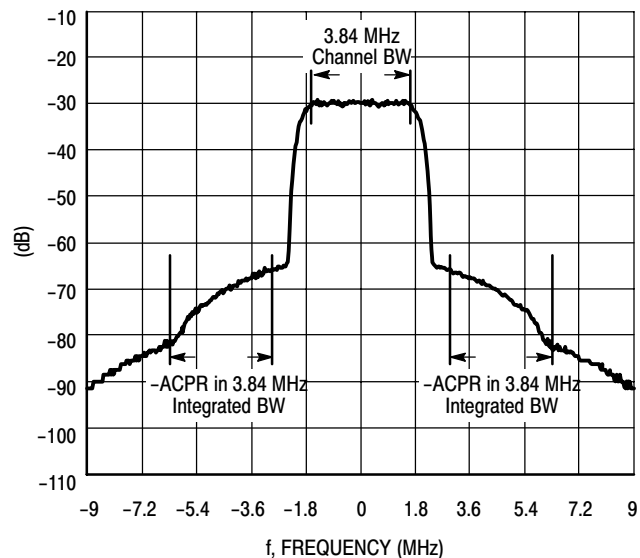
MTTF calculator available at <http://www.freescale.com/rf>. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.

**Figure 12. MTTF versus Junction Temperature**

## W-CDMA TEST SIGNAL

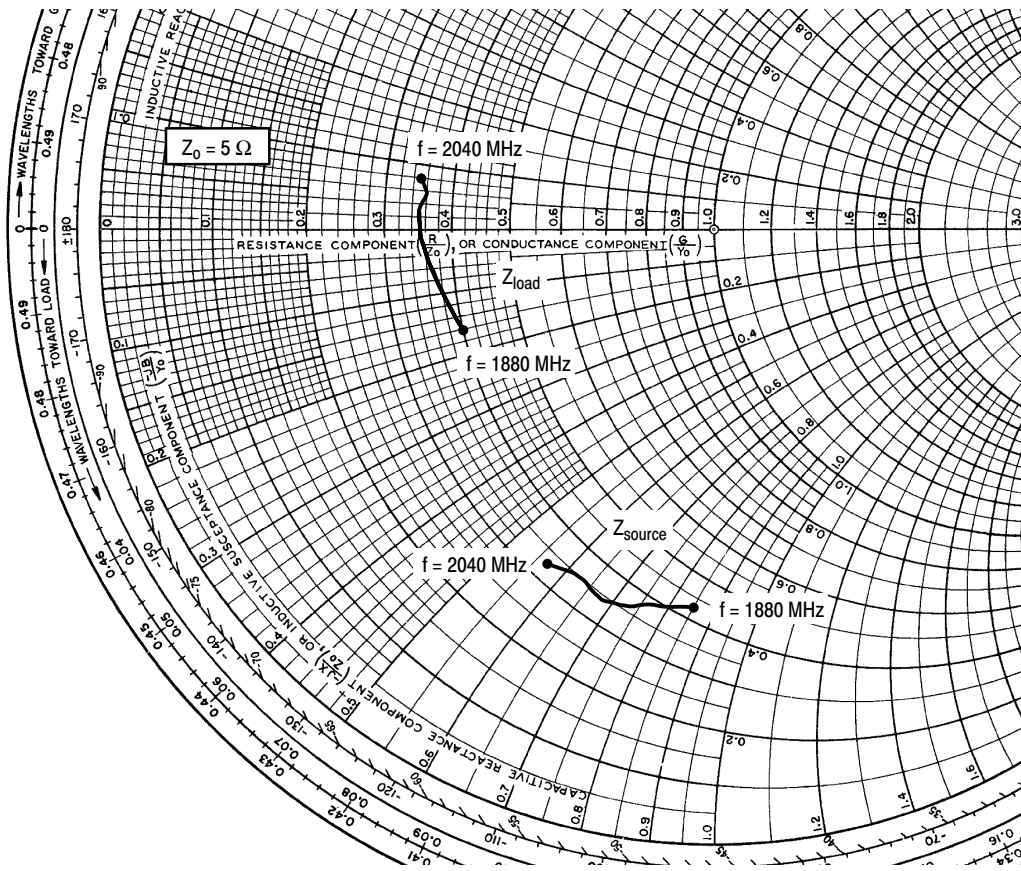


**Figure 13. CCDF W-CDMA 3GPP, Test Model 1, 64 DPCH, 50% Clipping, Single-Carrier Test Signal**



**Figure 14. Single-Carrier W-CDMA Spectrum**





$V_{DD} = 28 \text{ Vdc}$ ,  $I_{DQ} = 1600 \text{ mA}$ ,  $P_{out} = 56 \text{ W Avg.}$

f MHz	$Z_{source}$ $\Omega$	$Z_{load}$ $\Omega$
1880	$2.11 - j4.27$	$1.99 - j0.79$
1900	$2.05 - j4.11$	$1.96 - j0.64$
1920	$1.98 - j3.95$	$1.92 - j0.49$
1940	$1.92 - j3.80$	$1.86 - j0.34$
1960	$1.82 - j3.63$	$1.78 - j0.20$
1980	$1.72 - j3.40$	$1.74 + j0.01$
2000	$1.74 - j3.17$	$1.77 + j0.15$
2020	$1.71 - j3.02$	$1.78 + j0.29$
2040	$1.66 - j2.85$	$1.75 + j0.42$

$Z_{source}$  = Test circuit impedance as measured from gate to ground.

$Z_{load}$  = Test circuit impedance as measured from drain to ground.

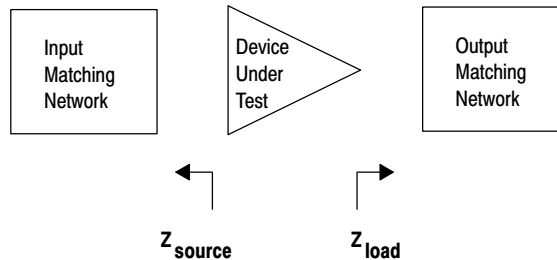
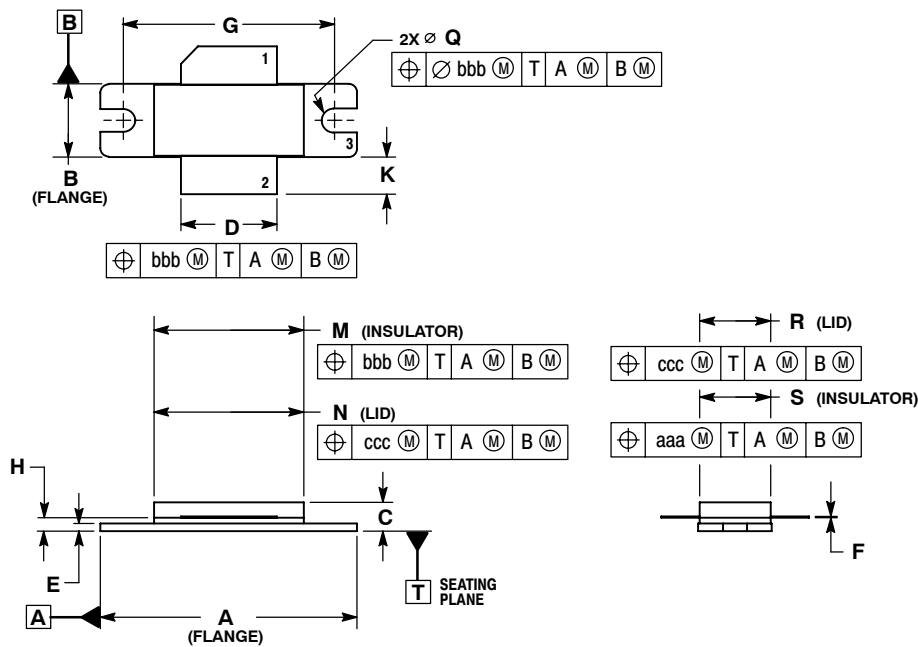


Figure 15. Series Equivalent Source and Load Impedance

## PACKAGE DIMENSIONS

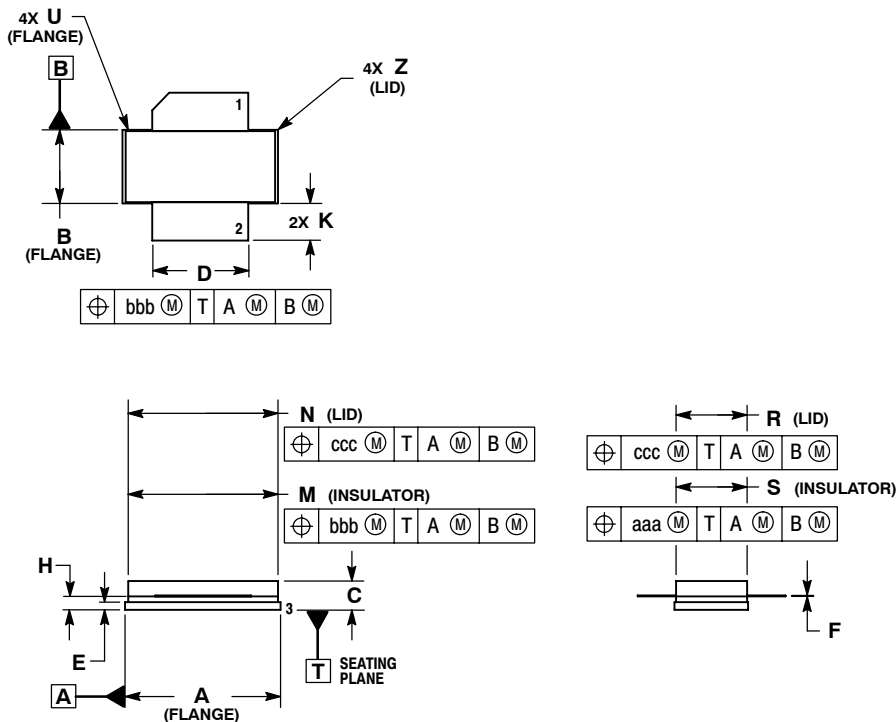


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
  2. CONTROLLING DIMENSION: INCH.
  3. DELETED
  4. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.335	1.345	33.91	34.16
B	0.380	0.390	9.65	9.91
C	0.125	0.170	3.18	4.32
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
G	1.100 BSC		27.94 BSC	
H	0.057	0.067	1.45	1.70
K	0.170	0.210	4.32	5.33
M	0.774	0.786	19.66	19.96
N	0.772	0.788	19.60	20.00
Q	Ø.118	Ø.138	Ø3.00	Ø3.51
R	0.365	0.375	9.27	9.53
S	0.365	0.375	9.27	9.52
aaa	0.005 REF		0.127 REF	
bbb	0.010 REF		0.254 REF	
ccc	0.015 REF		0.381 REF	

- STYLE 1:  
 PIN 1. DRAIN  
 2. GATE  
 3. SOURCE

**CASE 465-06  
 ISSUE G  
 NI-780  
 MRF6S19200HR3**



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
  2. CONTROLLING DIMENSION: INCH.
  3. DELETED
  4. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.805	0.815	20.45	20.70
B	0.380	0.390	9.65	9.91
C	0.125	0.170	3.18	4.32
D	0.495	0.505	12.57	12.83
E	0.035	0.045	0.89	1.14
F	0.003	0.006	0.08	0.15
H	0.057	0.067	1.45	1.70
K	0.170	0.210	4.32	5.33
M	0.774	0.786	19.61	20.02
N	0.772	0.788	19.61	20.02
R	0.365	0.375	9.27	9.53
S	0.365	0.375	9.27	9.52
U	---	0.040	---	1.02
Z	---	0.030	---	0.76
aaa	0.005 REF		0.127 REF	
bbb	0.010 REF		0.254 REF	
ccc	0.015 REF		0.381 REF	

- STYLE 1:  
 PIN 1. DRAIN  
 2. GATE  
 5. SOURCE

**CASE 465A-06  
 ISSUE H  
 NI-780S  
 MRF6S19200HSR3**

MRF6S19200HR3 MRF6S19200HSR3

## PRODUCT DOCUMENTATION

Refer to the following documents to aid your design process.

### Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

### Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

## REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Mar. 2008	<ul style="list-style-type: none"><li>• Initial Release of Data Sheet</li></ul>

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