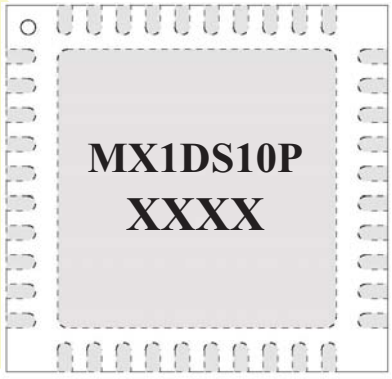
MX1DS10P Datasheet

CENTELLAX

15 GHz Ultra - Variable Broadband Prescaler

Features

- Wide Operating Range: 0.05 - 15GHz
- Variable Divide Ratios: 2 to 2^{20}
- Single-Ended and/or Differential Drive
- High Input Sensitivity
- Size: 6mm x 6mm
- Single - 3.3V Power Supply
- Low SSB Phase Noise: -153 @ 10KHz



RoHS · WEEE · COMPLIANT

40 pin Quad Flat No Lead (QFN)
6x6 mm pkg, 0.5mm pad pitch
JEDEC MO-220 Compliant

Marking Information:
MX1DS10P = Device Part Number
XXXX = Lot Code

Description

The MX1DS10P is a broadband 0.05GHz to 15GHz prescaler with a variable divide ratio between 2 and 1048576 (=2^{20}). All inputs and outputs are DC coupled using CML logic levels. The IC used in this part is manufactured in an advanced Silicon Germanium (SiGe) process. The part requires a single 3.3V supply and measures only 6mm x 6mm.

Pad Metallization

The QFN package pad metallization consists of a 300-800 micro-inch (typical thickness 435 micro-inch or 11.04um) 100% matte Sn plate. The plating covers a Cu (C194) leadframe. The packages are manufactured with a >1hr 150C annealing/heat treating process, and the matte (non-glossy) plating, specifically to mitigate tin whisker growth.

Application

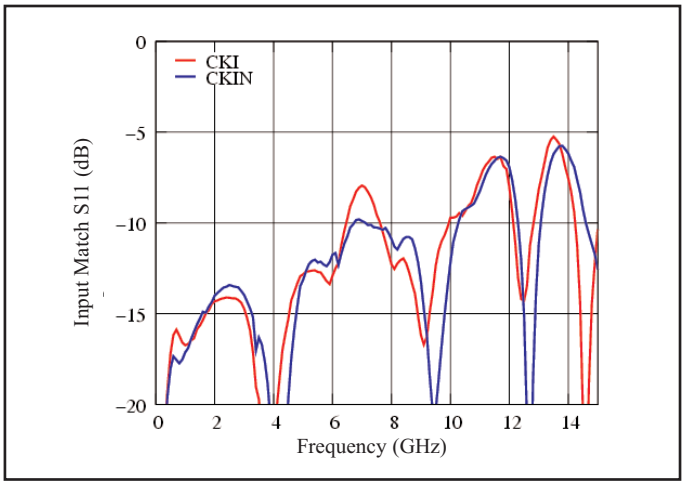
The MX1DS10P is ideal for phase locked loops and other synthesizers requiring large and variable divide ratios. Other applications include trigger generation for high-speed measurement systems. The MX1DS10P can be employed in high frequency phase locked loops that can take advantage of the low 1/f noise of SiGe HBT's. General purpose test instrumentation systems will also benefit from the high input sensitivity and broad frequency range.

Key Specifications (T=25 ºC)

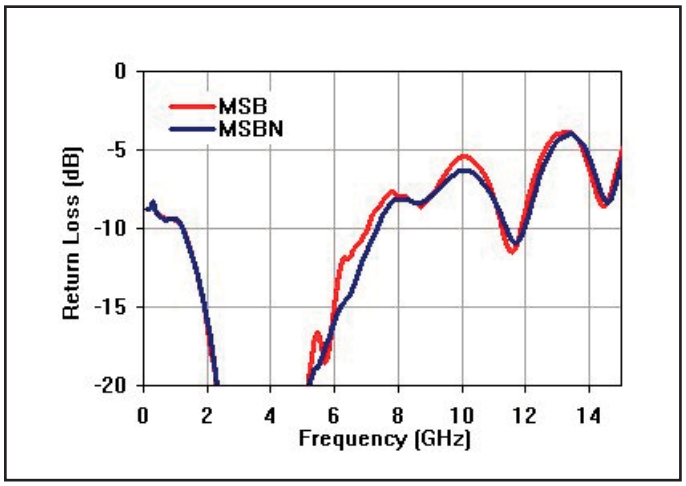
Vee = -3.3V, Iee = 430mA, Zo = 50Ω

Parameter	Description	Minimum	Typical	Maximum
Clk_{in} (GHz)	Input Clock Frequency	0.05	-	15
Clk_{pwr} (dBm)	Input Clock Power Max	-	-	10
Clk_{pwr} (dBm)	Input Clock Power Min	-	-10	-
D_{out} (V_{ppk})	Output Voltage Swing	0.5	1.0	-

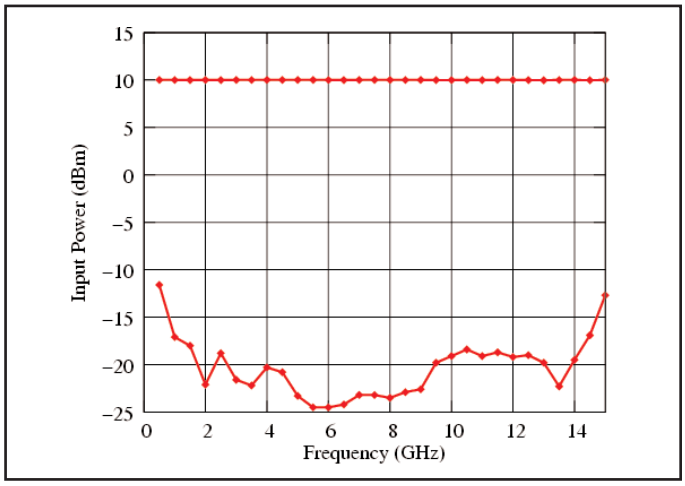
Parameter	Description	DC-6GHz	6-10GHz	10-15GHz
S11 (dB)	Input Match (Typical)	-12	-7	-5
S22 (dB)	Output Match (Typical)	-7	-5	-3



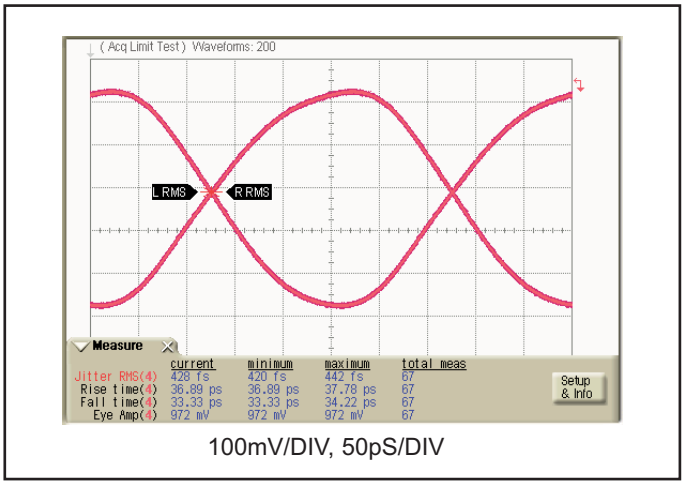
Return Loss of Differential Input Ports



Return Loss of Differential Output Ports

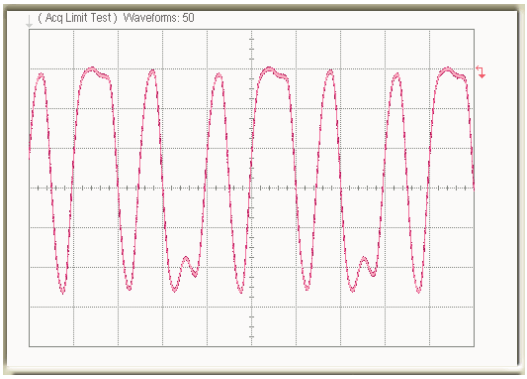


Input Sensitivity Window



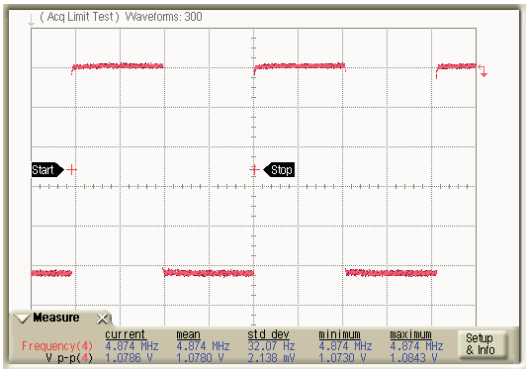
100mV/DIV, 50pS/DIV

Divide-by-2 Output (Input: 10GHz; Output: 5GHz)



100 mV/DIV, 200pS/DIV

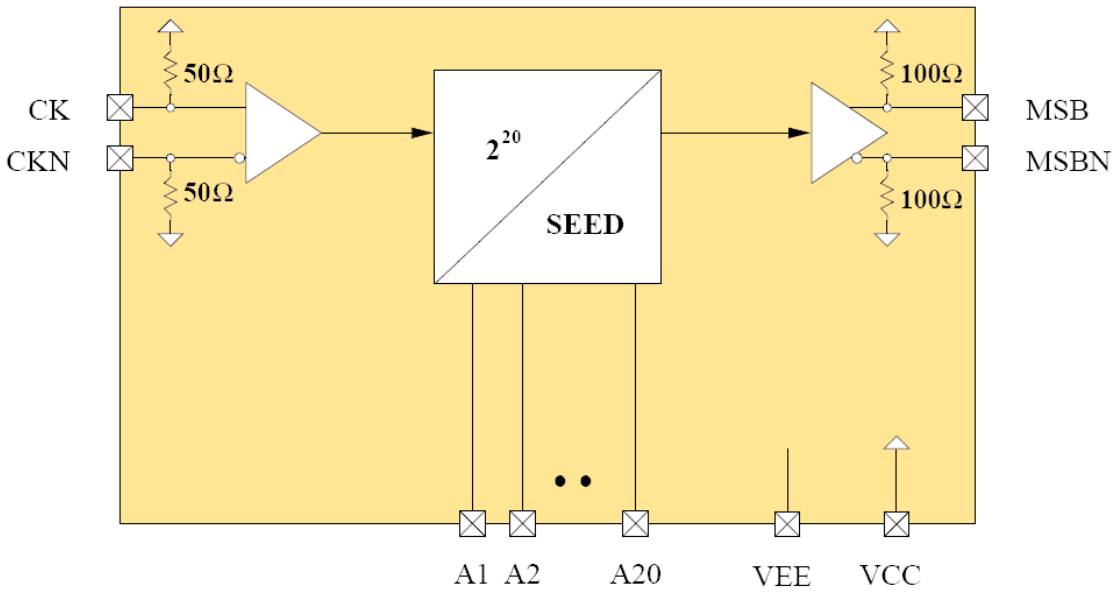
Divide-by-(8/3) Output (Input: 10GHz; Output: 3.75GHZ)



100 mV/DIV, 50nS/DIV

Divide-by-2048 Output (Input: 10GHz: Output: 4.9MHz)

Functional Block Diagram



SEED = A1 + (A2 x 2^1) + (A3 x 2^2) + ...+ (A20 x 2^{19}) (Maximum valid SEED = 2^{19})

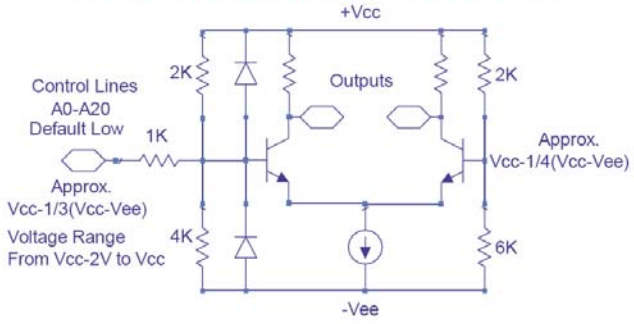
Divide Ratio = 2^{20} / SEED (Lowest valid divide ratio = 2)

$Freq_{out}$ = $Freq_{clk}$ / (Divide Ratio)

Pin Description

Port Name	Description	Additional Comments
CK	Clock Input, Positive Terminal	Negative CML signal levels
CKN	Clock Input, Negative Terminal	Negative CML signal levels
MSB	Divided Output, Positive Terminal	Negative CML signal levels
MSBN	Divided Output, Negative Terminal	Negative CML signal levels
A1,A2...A20	Divide Ratio Selectors	Divide ratio = Value of the binary seed A1...A20
VCC	RF & DC Ground	-
VEE	-3.3V @ 430mA	Negative Supply Voltage
Paddle	Backside of die	Must be connected to good heatsink (see text)

Simplified Control Logic Schematic



Application Notes

Low Frequency Operation

Low frequency operation is limited by external bypass capacitors and the slew rate of the input clock. The next paragraph shows the calculations for the bypass capacitors. If DC coupled, the device operates down to DC for square-wave inputs. Sine-wave inputs are limited to ~50MHz due to the 10dBm max input power limitation.

The values of the coupling capacitors for the high-speed inputs and outputs (I/O's) is determined by the lowest frequency the IC will be operated at.

$$C >> \frac{1}{2 \cdot \pi \cdot 50\Omega \cdot f_{lowest}}$$

For example to use the device below 30kHz, coupling capacitors should be larger than 0.1uF.

IC Assembly

The device is designed to operate with either single-ended or differential inputs. Figures 1, 2 & 3 show the IC assembly diagrams for positive and negative supply voltages. In either case the supply should be capacitively bypassed to the ground to provide a good AC ground over the frequency range of interest. The backside of the chip should be connected to a good thermal heat sink.

All RF I/O's are connected to VCC through on-chip termination resistors. This implies that when Vcc is not DC grounded (as in the case of positive supply), the RF I/O's should be AC coupled through series capacitors unless the connecting circuit can generate the correct levels through level shifting.

ESD Sensitivity

Although SiGe IC's have robust ESD sensitivities, preventive ESD measures should be taken while storing, handling, and assembling.

Inputs are more ESD susceptible as they could expose the base of a BJT or the gate of a MOSFET. For this reason, all the inputs are protected with ESD diodes. These inputs have been tested to withstand voltage spikes up to 400V.

Negative CML Logic Levels for DC Coupling (T=25 ºC)

Assuming 50Ω Terminations at Inputs and Outputs

Parameter		Minimum	Typical	Maximum
Differential	Logic Input$_{high}$	Vcc	Vcc	Vcc
	Logic Input$_{low}$	Vcc - 0.05V	Vcc - 0.3V	Vcc - 1V
Single	Logic Input$_{high}$	Vcc + 0.05V	Vcc + 0.3V	Vcc + 1V
	Logic Input$_{low}$	Vcc - 0.05V	Vcc - 0.3V	Vcc - 1V
Differential & Single	Logic Output$_{high}$	Vcc	Vcc	Vcc
	Logic Output$_{low}$	Vcc - 0.2V	Vcc - 0.3V	Vcc - 0.4V

Differential vs Single-Ended

The MX1DS10P is fully differential to maximize signal-to-noise ratios for high-speed operation. All high speed inputs and outputs are terminated to Vcc with on-chip resistors (refer to functional block diagram for specific resistor values). The maximum DC voltage on any terminal must be limited to V_{max} to prevent damaging the termination resistors with excessive current. Regardless of bias conditions, the following equation should be satisfied when driving the inputs differentially:

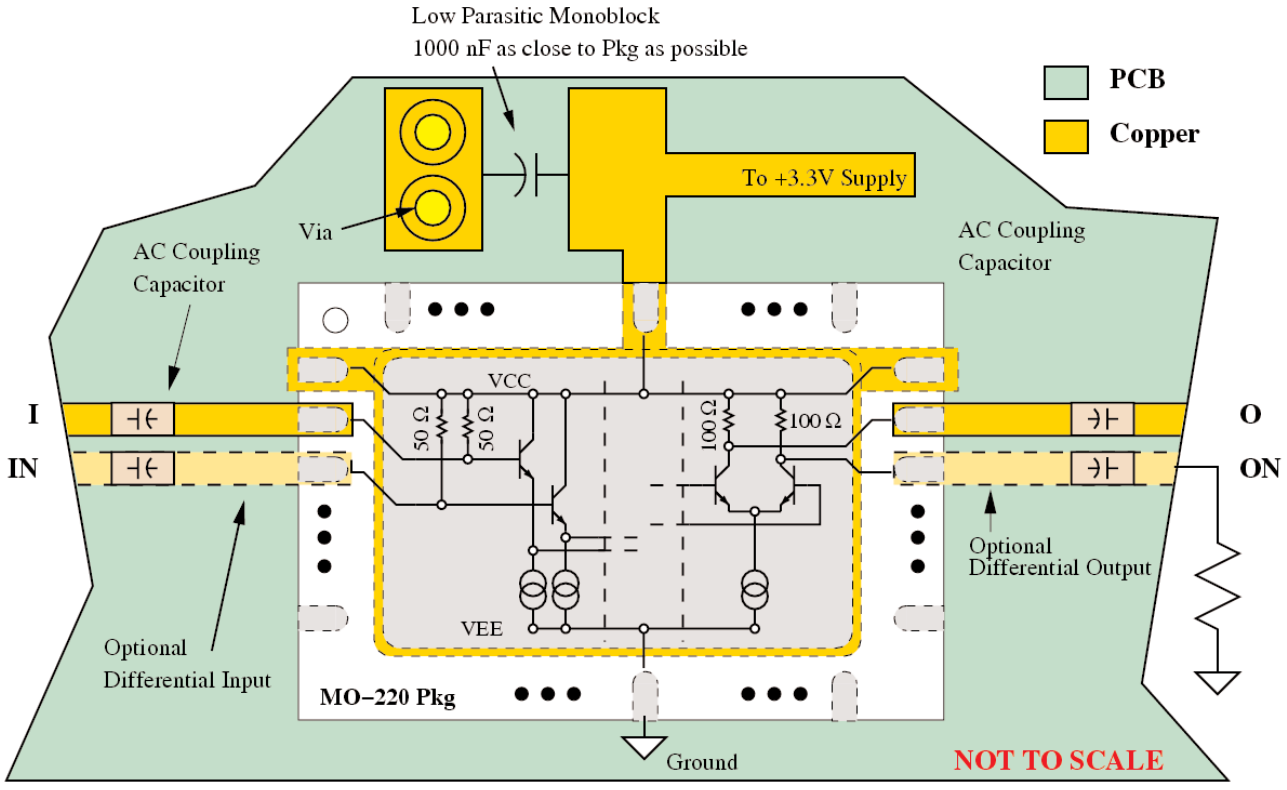
$$I\ V_{dm}/2 + V_{cm}\ I < Vcc \geq V_{max}$$

where V_{dm} is the differential input signal and V_{cm} is the common-mode voltage.

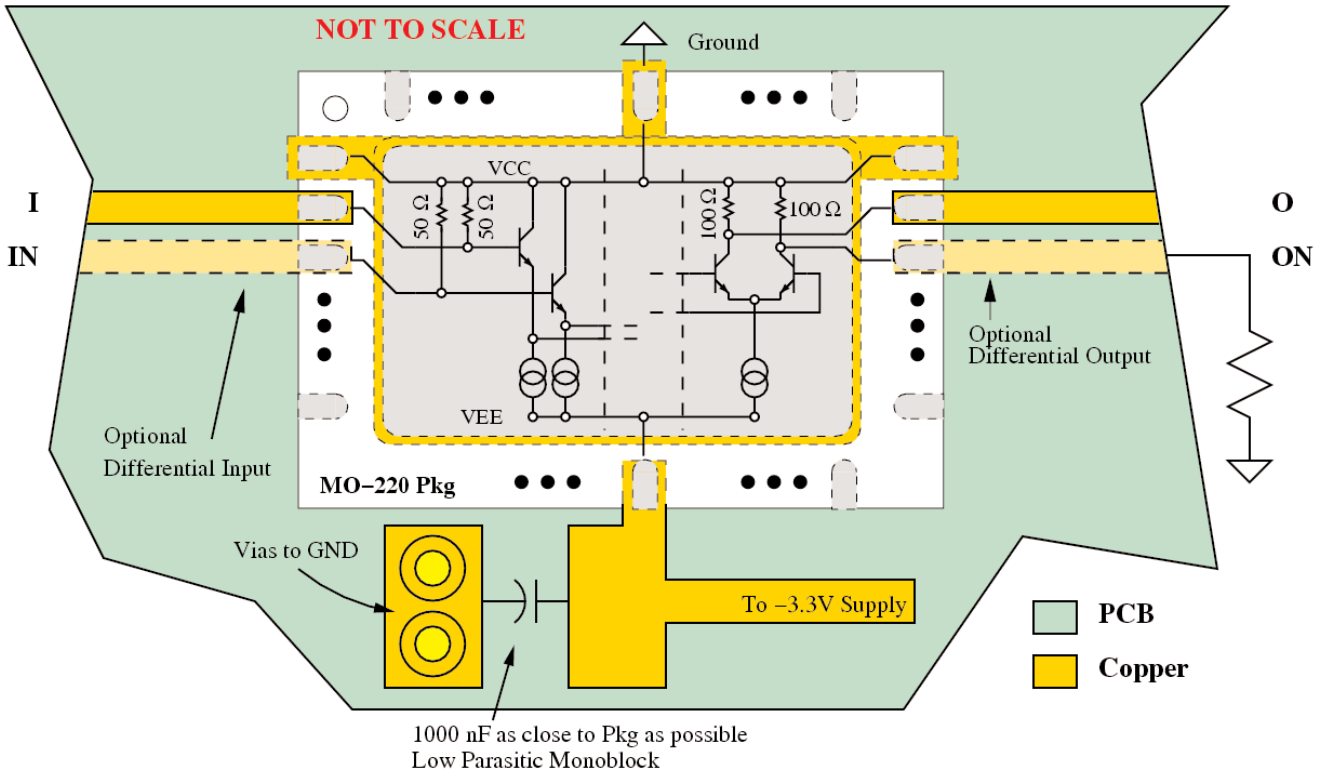
In addition to the maximum input signal levels, single-ended operation imposes additional restrictions: the average DC value of the waveform at IC should be equal to Vcc for single-ended operation. In practice, this is easily achieved with a single capacitor on the input acting as a DC block. The value of the capacitor should be large enough to pass the lowest frequencies of interest. Use the positive terminals for single-ended operation while terminating the negative terminal to Vcc.

Note that a potential oscillation mechanism exists if both inputs are static and have identical DC voltages; a small DC offset on either input is sufficient to prevent possible oscillations. Tying unused inputs directly to Vcc shorts out the internal 50Ω bias resistor, imposing a DC offset sufficient to prevent oscillations. Driving the differential inputs with DC blocks, or driving the single-ended inputs without terminating unused inputs, is not recommended without taking additional steps to eliminate the potential oscillation issues.

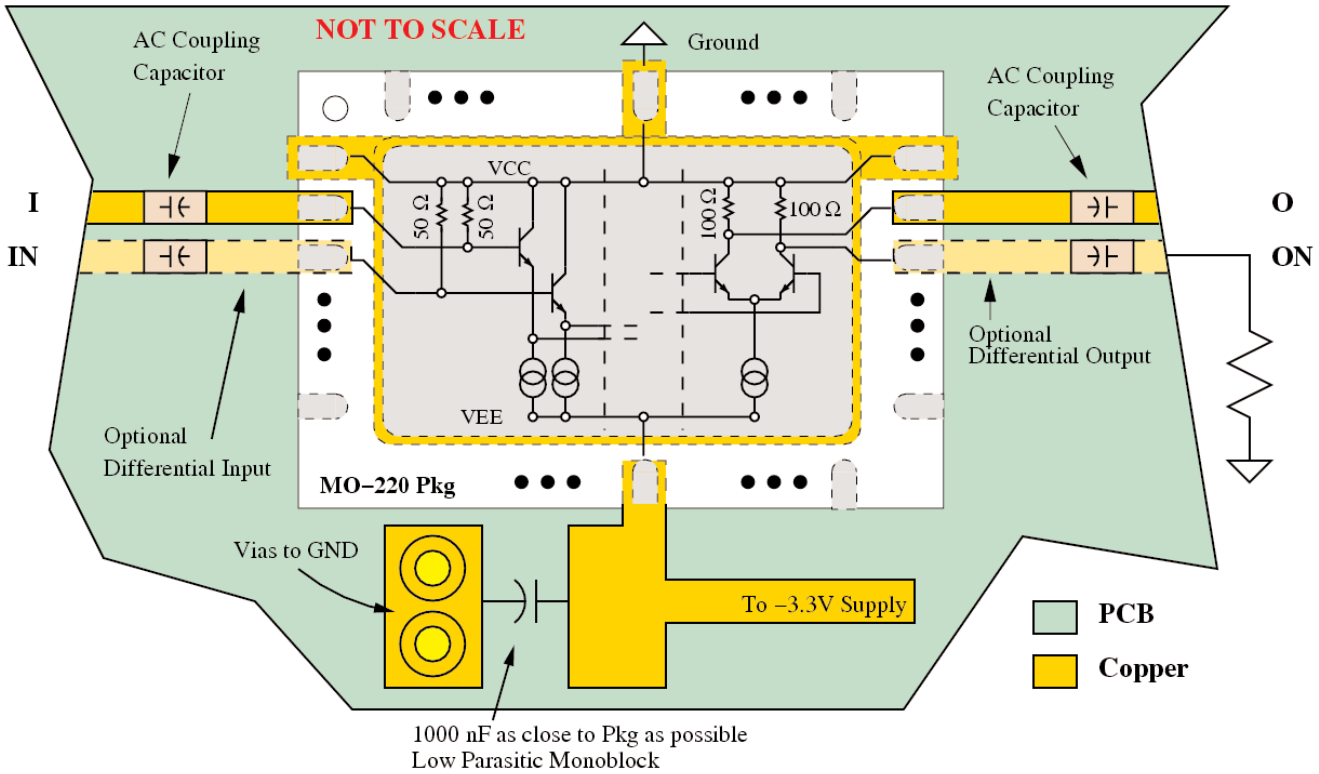
Positive Supply (AC Coupling)



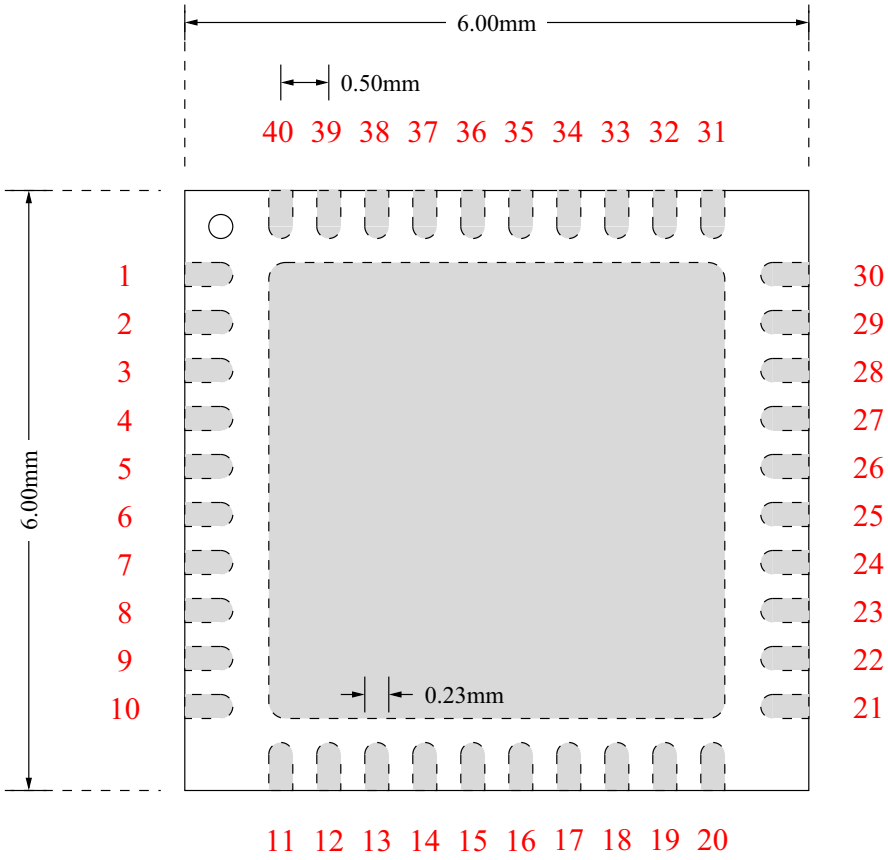
Negative Supply (DC Coupling)



Negative Supply (AC Coupling)



MX1DS10P Physical Characteristics



Pkg Size:	**6.00 x 6.00 mm**
Pkg Size Tolerance:	**+/- 0.25 mm**
Pkg Thickness:	**0.9 +/- 0.1 mm**
Pad Dimensions:	**0.23 x 0.4 mm**
Center Paddle:	**4.2 x 4.2 mm**
JEDEC Designator:	**MO-220**

TOP VIEW

MX1DS10P Pin Definition

Pin Function		Operational Notes
5,14,22,26,37 (Vcc)	RF and DC Ground	0V
1,6,9,13,17,27,34 (Vee)	Negative Supply Voltage	Nominally -3.3V
31,32,35,36		No Connection
2 (A4)	Divide Ratio Selector	Defaults to logic 0, connect to 0V for logic 1
3 (A5)	Divide Ratio Selector	Defaults to logic 0, connect to 0V for logic 1
4 (A6)	Divide Ratio Selector	Defaults to logic 0, connect to 0V for logic 1
7 (CKN)	Clock Input	Negative Terminal of differential Input
8 (CK)	Clock Input	Positive Terminal of differential Input
10 (A7)	Divide Ratio Selector	Defaults to logic 0, connect to 0V for logic 1
11 (A8)	Divide Ratio Selector	Defaults to logic 0, connect to 0V for logic 1
12 (A9)	Divide Ratio Selector	Defaults to logic 0, connect to 0V for logic 1
15 (A10)	Divider Ratio Selector	Defaults to logic 0, connect to 0V for logic 1
16 (A11)	Divide Ratio Selector	Defaults to logic 0, connect to 0V for logic 1
18 (A12)	Divide Ratio Selector	Defaults to logic 0, connect to 0V for logic 1
19 (A13)	Divide Ratio Selector	Defaults to logic 0, connect to 0V for logic 1

MX1DS10P Pin Definition (continued)

Pin Function		Operational Notes
20 (A14)	Divide Ratio Selector	Defaults to logic 0, connect to 0V for logic 1
21 (A15)	Divide Ratio Selector	Defaults to logic 0, connect to 0V for logic 1
23 (A16)	Divide Ratio Selector	Defaults to logic 0, connect to 0V for logic 1
24 (A17)	Divide Ratio Selector	Defaults to logic 0, connect to 0V for logic 1
25 (A18)	Divide Ratio Selector	Defaults to logic 0, connect to 0V for logic 1
28 (MSBN)	Divider Output	Negative Terminal of differential output
29 (MSB)	Divider Output	Positive Terminal of differential output
30 (A19)	Divider Ratio Selector	Defaults to logic 0, connect to 0V for logic 1
33 (A20)	Divider Ratio Selector	Defaults to logic 0, connect to 0V for logic 1
38 (A1)	Divider Ratio Selector	Defaults to logic 0, connect to 0V for logic 1
39 (A2)	Divider Ratio Selector	Defaults to logic 0, connect to 0V for logic 1
40 (A3)	Divider Ratio Selector	Defaults to logic 0, connect to 0V for logic 1

Absolute Maximum Ratings

Parameter	Value	Unit
Supply Voltage (Vcc-Vee)	-4.0	V
RF input power (CK, CKN)	+10	dBm
Max DC Voltage Level (MSB, MSBN)	Vcc+1V	V
Min DC Voltage Level (MSB, MSBN)	Vcc-1V	V
Max DC Voltage Level (A1,A2,...A20)	Vcc	V
Min DC Voltage Level (A1,A2,...A20)	Vee	V
Operating Temperature	-40 to 85	ºC
Storage Temperature	-85 to 150	ºC