HD153109

Color Palette with Triple 6-bit DA Converter

The HD153109 is a triple 6-bit video DAC with color palette RAM, designed specifically for high performance high resolution color graphics. The HD153109 supports up to 256 simultaneous colors from a 262, 144 color palette and generates RS-343A/170A compatible red, green and blue video signals.

The HD153109 realizes high speed, high density and low power dissipation by implementing in Hi-Bi CMOS process.

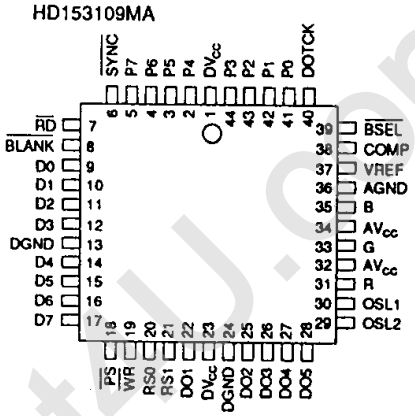
Features

- Displays 256 colors simultaneously among total 262, 144 colors
- Provides R-G-B 3 channels 6-bit DA converter on a chip
- Pixel word mask to control display
- Personal system/2™ compatible
- Extractable G (green) digital outputs from the CLT. (color look up table) enables application to lap top computers (Selectable of DAC outputs and digital outputs)
- DAC's outputs level can be set by 1 registor
- Programmable pedestral (0 or 7.5 IRE)
- DA converter consists of 3 channels, all of which can composite $\overline{\text{SYNC}}$ signal
- Selectable of $\overline{\text{SYNC}}$ signal composite and $\overline{\text{SYNC}}$ signal non-composite (HD153109FS only)
- At digital output, unrequired signals can be cut off. (HD153109FS and HD153109MA only)
- Maximum dotting rate of 50/65 MHz
- Low power dissipation of 650 mW typical
- Supporting TTL interface
- Less external parts

The "Personal System/2" is a registered trademark of IBM Corp.

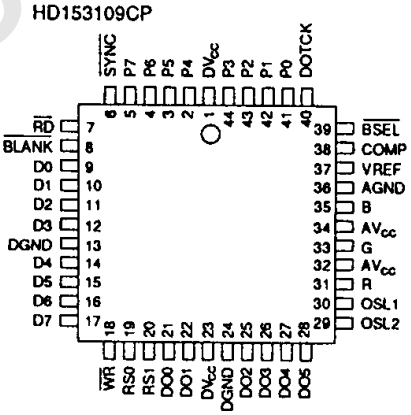
Pin Arrangement

HD153109MA



(MP-44S)

HD153109CP

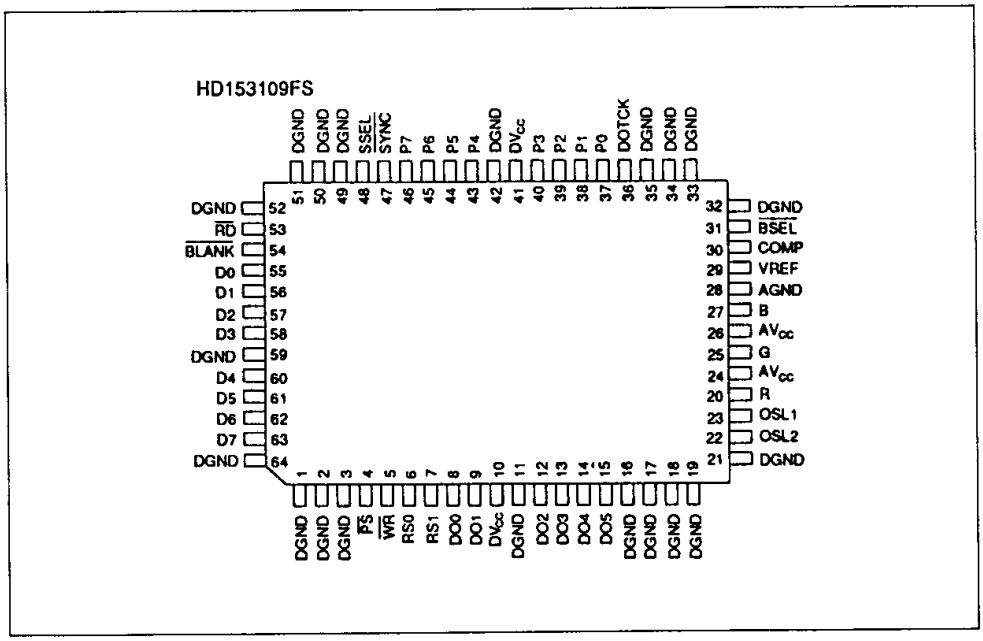


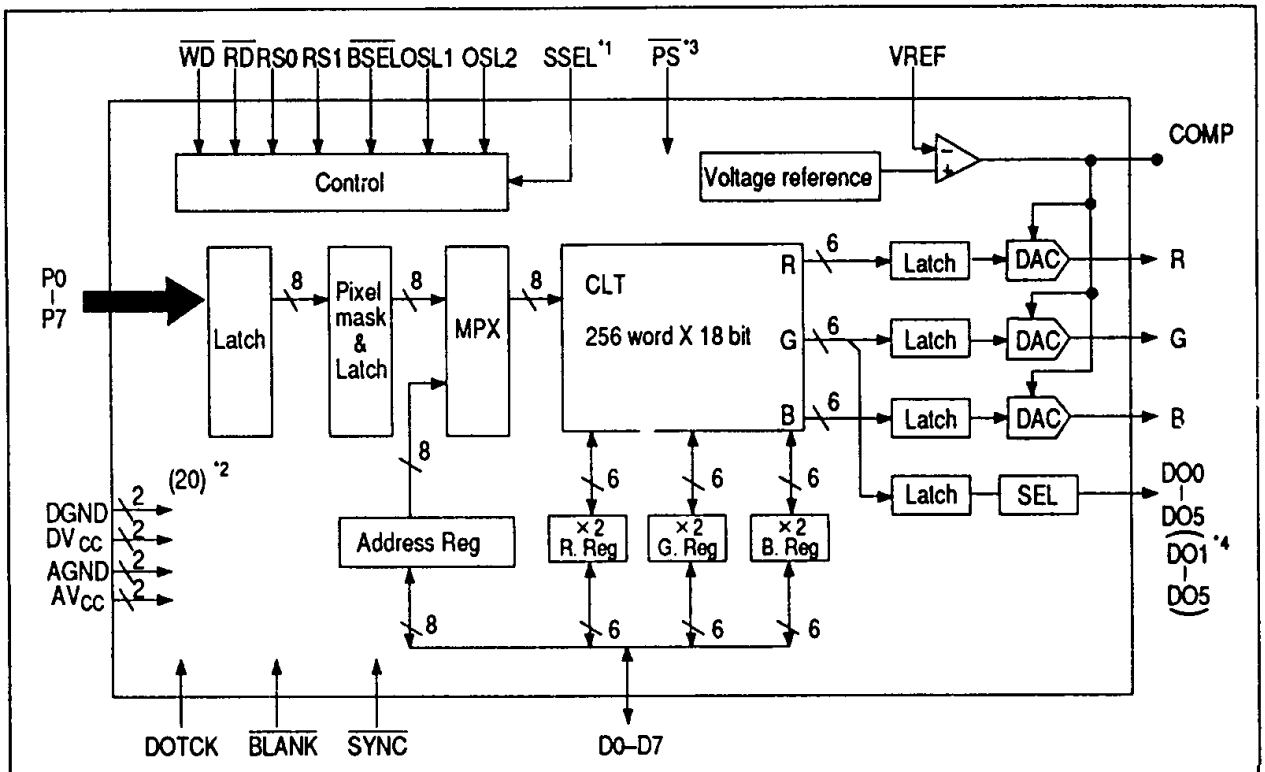
(CP-44)

Ordering Information

Type No.	Maximum operating frequency	Package
HD153109CP	50 MHz	44 pin PLCC (CP-44)
HD153109CP-65	65 MHz	
HD153109FS	50 MHz	64 pin QFP (FP-64B)
HD143109FS-65	65 MHz	
HD153109MA	50 MHz	44 pin shrink MSP (MP-44S)
HD153109FS-65	65 MHz	

Pin Arrangement (cont)





Notes:
1. SSEL is only provided on the HD153109FS. It is not provided on the HD153109CP or HD153109MA.
2. The figure in parentheses is for the HD153109FS.
3. $\overline{PS}$ is only provided on the HD153109FS and HD153109MA. It is not provided on the HD153109CP.
4. The HD153109MA is not provided with the DO0 output.

Figure 2 Block Diagrams

Table 1 Pin Description

Pin name	Pin number HD153109CP	HD153109FS	HD153109MA	Description
P0 to P7	41, 42, 43, 44, 2, 3, 4, 5	37, 38, 39, 40, 43, 44, 45, 46	41, 42, 43, 44, 2, 3, 4, 5	Pixel select inputs. P7 is MSB and P0 is LSB.
D0 to D7	9, 10, 11, 12, 14, 15, 16, 17	55, 56, 57, 58, 60, 61, 62, 63	9, 10, 11, 12, 14, 15, 16, 17	Data input/output terminal when writing/reading CLT and registers (address register, pixel mask register and R, G, B register) D7 is MSB and D0 is LSB.
$\overline{RD}$	7	53	7	Clock terminal when reading CLT and registers (address register, pixel mask register and R, G, B register)
$\overline{WR}$	18	5	19	Clock terminal when writing CLT and registers (address register, pixel mask register and R, G, B register)
RS0, RS1	19, 20	6, 7	20, 21	Terminal to select CLT, address register and pixel mask register
DO0 to DO5 (DO1 to DO5)*	21, 22, 25, 26 27, 28	8, 9, 12, 13, 14, 15	22, 25, 26, 27, 28	Terminal to extract green digital signal from the palette DO5 is MSB and DO0 is LSB. Since the HD153109MA is not provided with a DO0 output, DO5 is MSB and DO1 is LSB.
VREF	37	29	37	Terminal to connect a reference resistor to determine the output level of DAC analog signal (R_{VREF} = 12 kΩ typ.)
COMP	38	30	38	Terminal to connect a capacitor for phase-compensation
OSL1, OSL2	30, 29	22, 21	30, 29	Terminal to select an output of digital signals
R, G, B	31, 33, 35	23, 25, 27	31, 33, 35	DAC analog outputs
$\overline{BLANK}$	8	54	8	Terminal to set the DAC analog signal on BLANK level
$\overline{BSEL}$	39	31	39	Terminal to set pedestral (0 or 7.5 IRE)
DOTCK	40	36	40	Clock input to do operation of digital and analog parts. When this clock rises, CLT and input data of $\overline{BLANK}$ is taken and analog signals are output.
SSEL	—	48	—	Terminal to select SYNC level (0 or 40 IRE)

* The HD153109MA is not provided with the DO0 output.

Pin Description (cont)

Pin name	Pin number HD153109CP	HD153109FS	HD153109MA	Description
$\overline{SYNC}$	6	47	6	• HD153109FS Terminal to set the analog signal of DAC on SYNC level. when SSEL = 'H', DAC output level will be SYNC level. • HD153109CP CRT synchronous signal inputs
$\overline{PS}$	—	4	18	When only digital output is used and DAC is not used, unrequired signal to DAC and RAM red and blue cells (total 12 bits) can be cut off by setting this terminal 'L'.
DV_{CC}	1, 23	10, 41	1, 23	Digital power
DGND	13, 24	1, 2, 3, 11, 16, 17, 18, 19, 20, 32, 33, 34, 35, 42, 49, 50, 51, 52, 59, 64	13, 24	Digital GND
AV_{CC}	32, 34	24, 26	32, 34	Analog power
AGND	36	28	36	Analog GND

2

Functions

Access to CLT and registers

RS0 and RS1 select the CLT or a register. (See table 2)

Address register: The address register is a register which is set with the address of CLT from D0 to D7 when a data write/read operation is performed to/from CLT. Write/read is performed to/from this register with D0 as the LSB and D7 as the MSB.
When data is to be written to CLT, the address register is selected by RS0 = '0' and RS1 = '0', and then the write address is set to the address register from D0 to D7 (see figure 7).
When data is to be read from CLT, the address register is selected by RS0 = '1' and RS1 = '1', and then the read address is set to the address register from D0 to D7 (see figure 8). Also, the address register contents are read out as shown in figures 10 and 11.

Pixel mask register: The pixel mask can change the displayed color without changing the contents of the video memory or CLT. To use the pixel mask, select the pixel mask register by RS0 = '0' and RS1 = '1' and then set the pixel mask data from D0 (LSB) to D7 (MSB) (see figures 13 and 14). The color palette LSI inputs the logical product (AND) of the address data from P0 (LSB) to P7 (MSB) and the value set in the pixel mask register for use as the CLT address. As a result, the address data is masked when the value in the pixel mask register is '0' and is canceled when the value in the pixel mask register is '1'.
An example of how the value set in the pixel mask register determines the CLT address value from the address data input value is shown below in table 3.

RGB register: There are two types of RGB register -- a register for holding color data to be written to CLT and a register for holding color data read from CLT. Each register is comprised of 18 bits.
When data is to be written to or read from CLT, the RGB register is selected by RS0 ='1' and RS1 = '0', and then the data is read from or written to D0 (LSB) to D5 (MSB). At this time, values D6 and D7 can be either '0' or '1'. Data is written or read in the RGB sequence (see figures 7 and 8).

Table 2 Register Selection

RS1	RS0	Selection
0	0	Address register (write mode)
1	1	Address register (read mode)
0	1	CLT
1	0	Pixel mask register

Table 3 Pixel Mask Example

Pixel mask register	1	0	1	0	1	1	0	1
Address input (P7 to P0)	Pd7	Pd6	Pd5	Pd4	Pd3	Pd2	Pd1	Pd0
CLT address value	Pd7	0	Pd5	0	Pd3	Pd2	0	Pd0

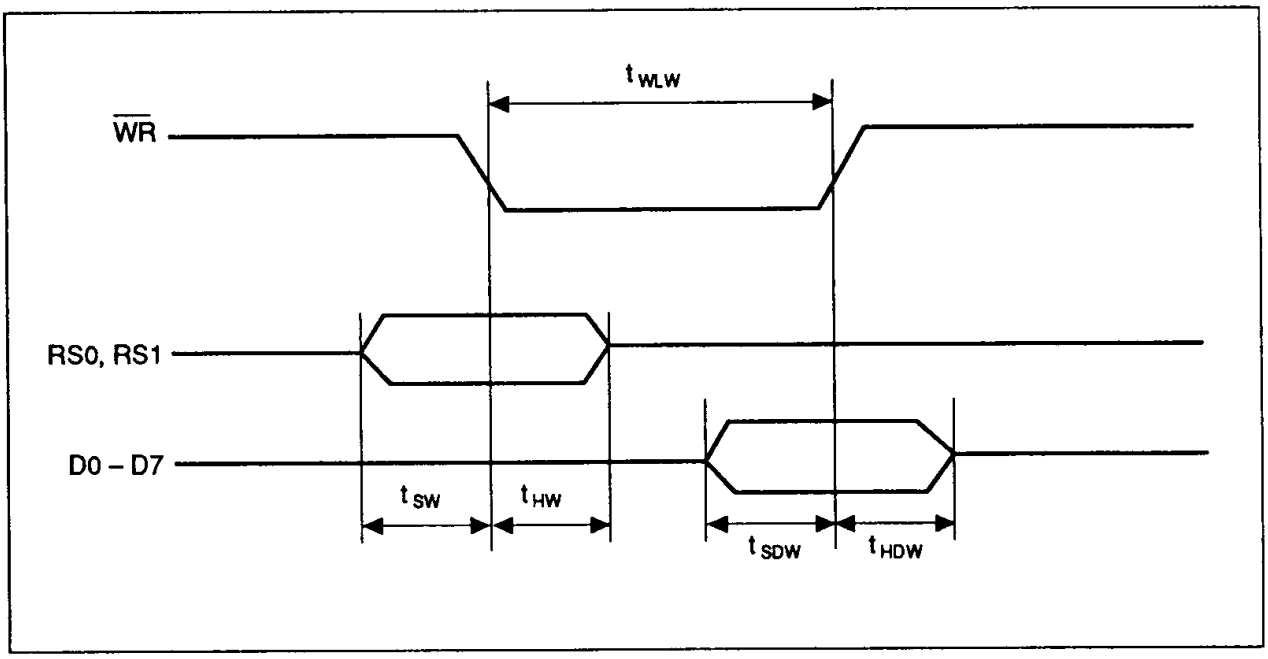


Figure 3 Data Write Timing

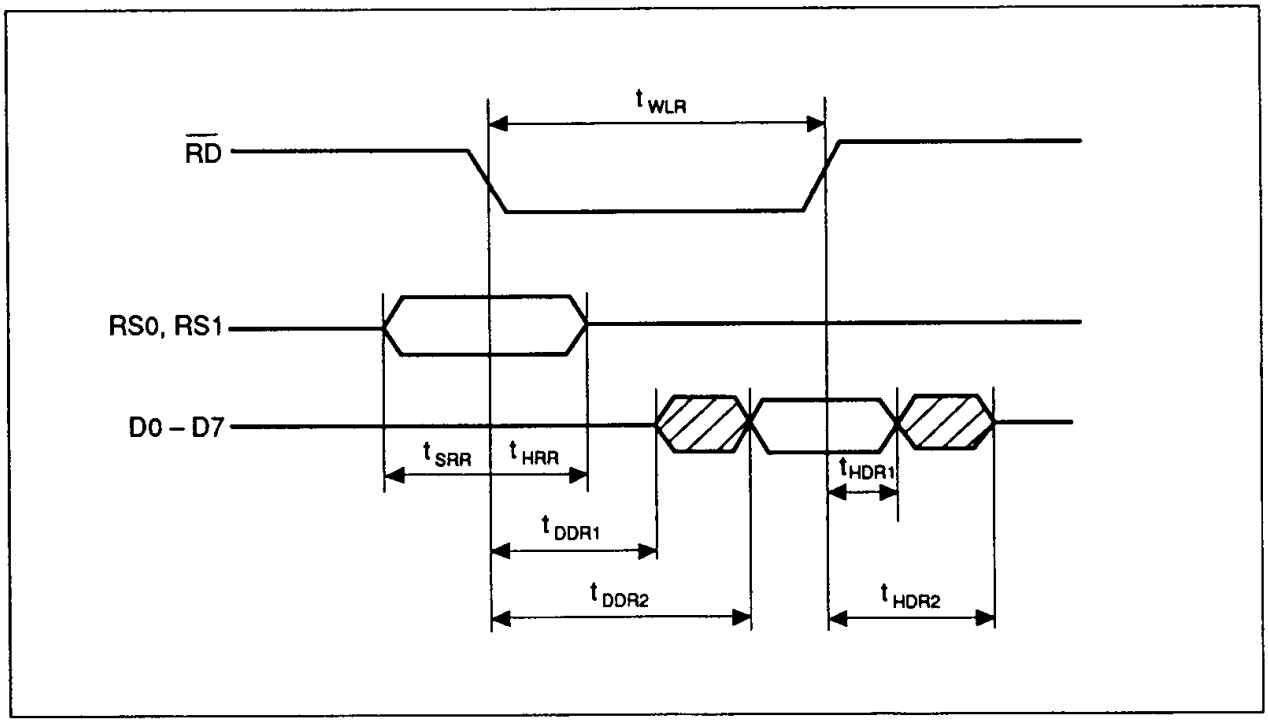


Figure 4 Data Read Out Timing

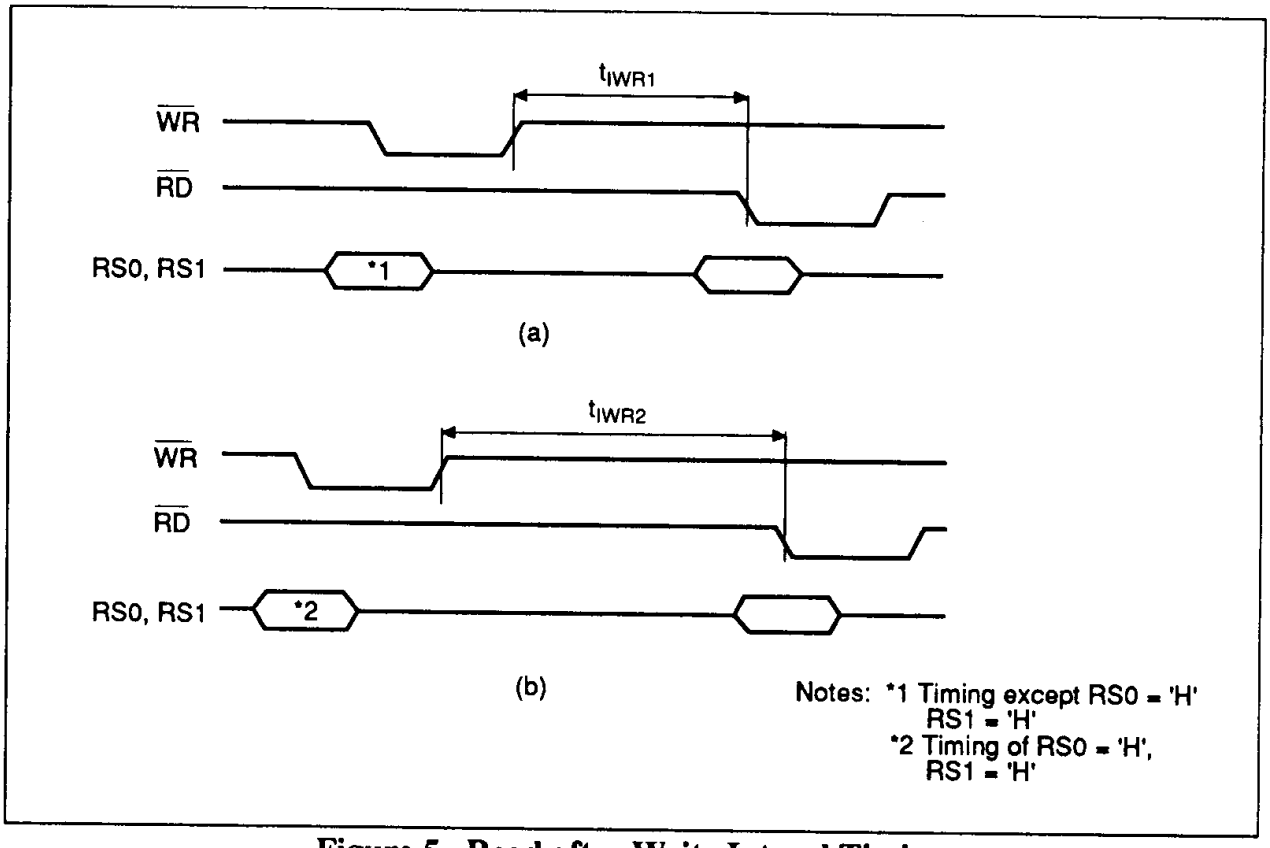


Figure 5 Read after Write Inteval Timing

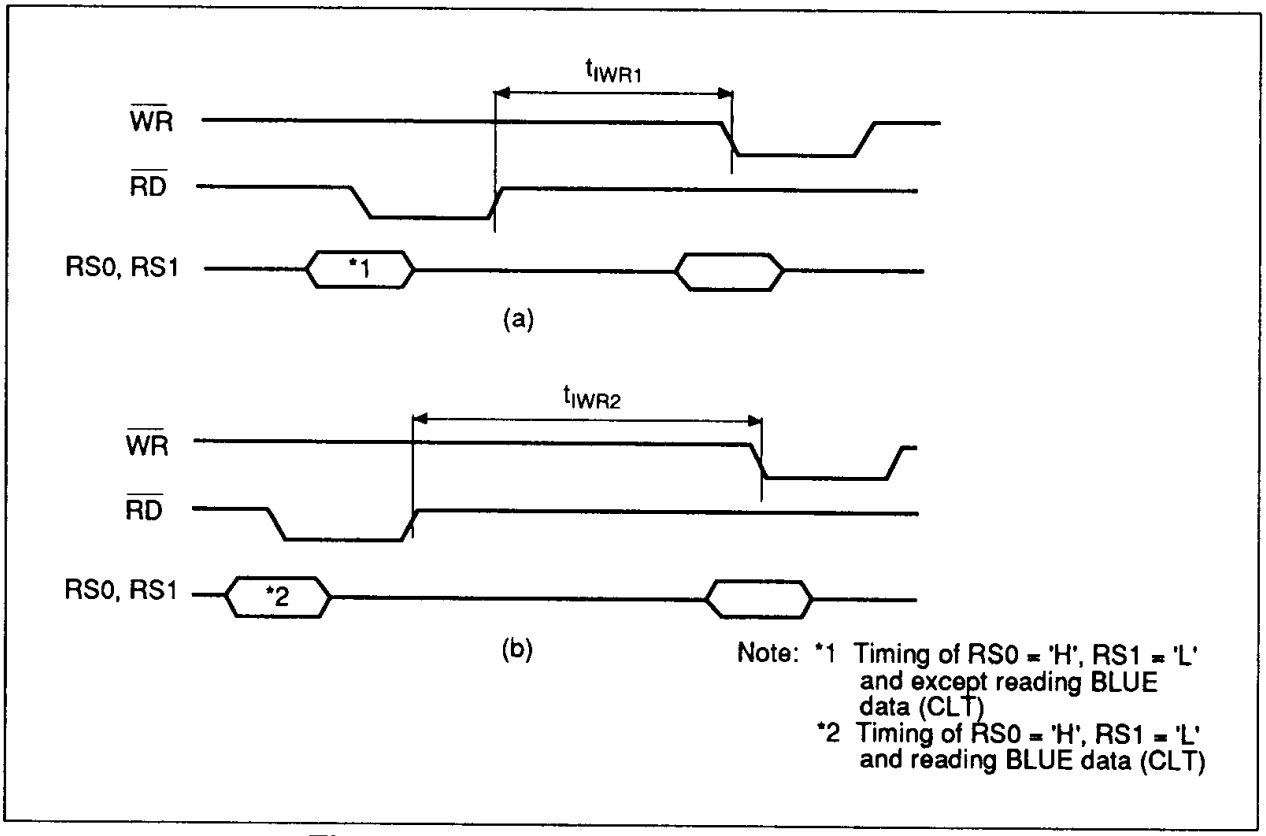
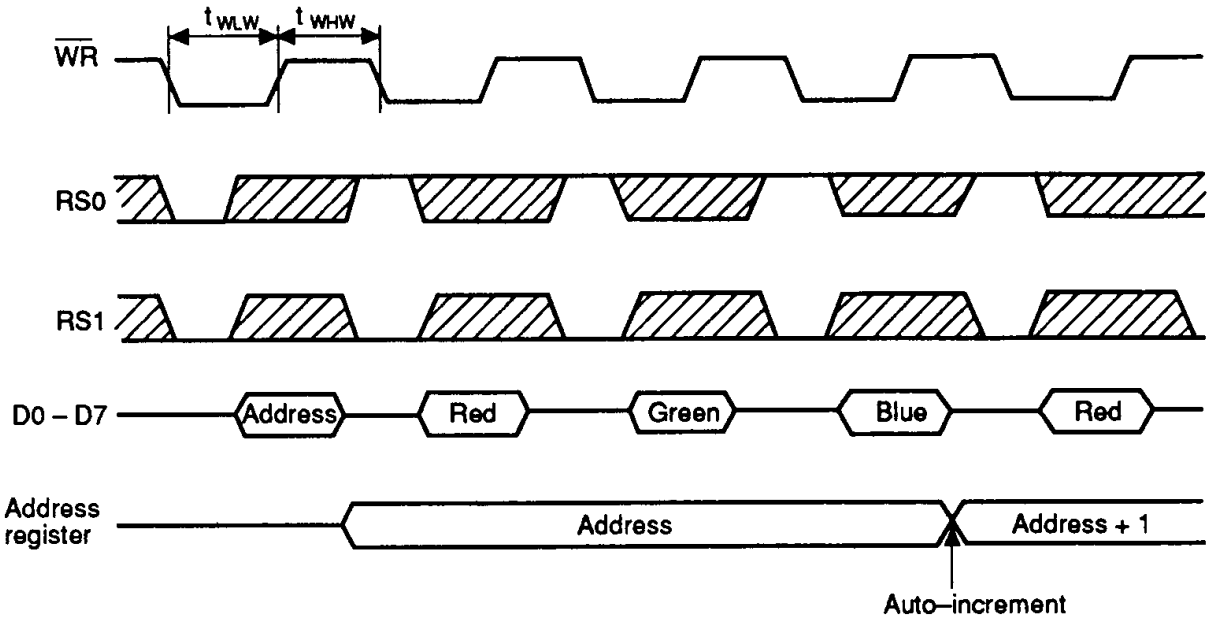
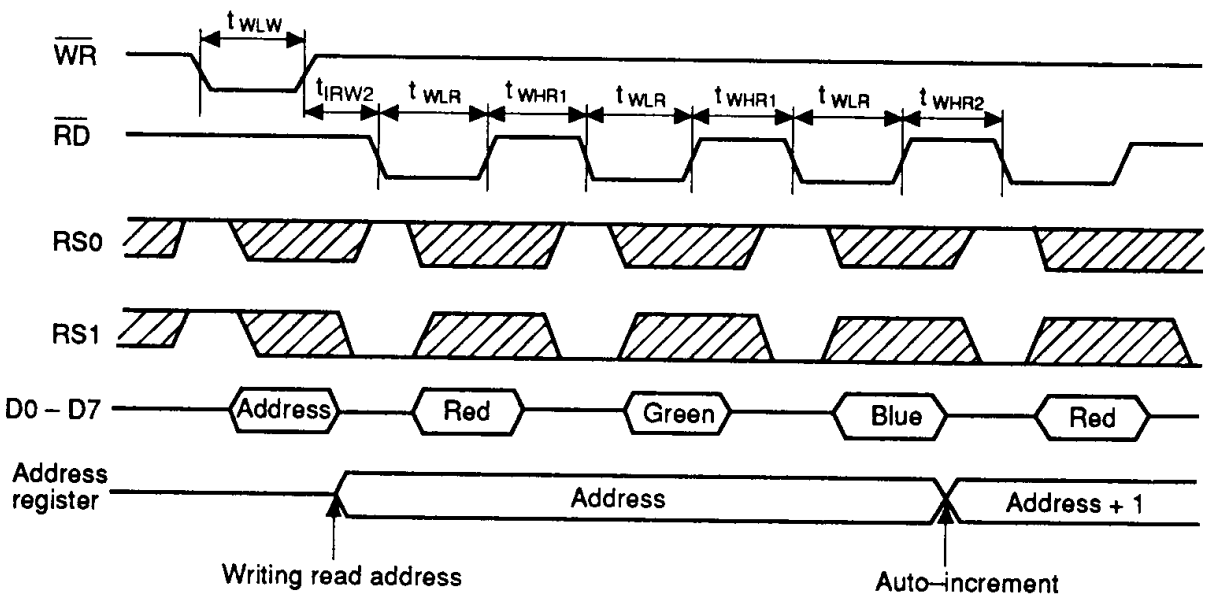


Figure 6 Write after Read Interval Timing



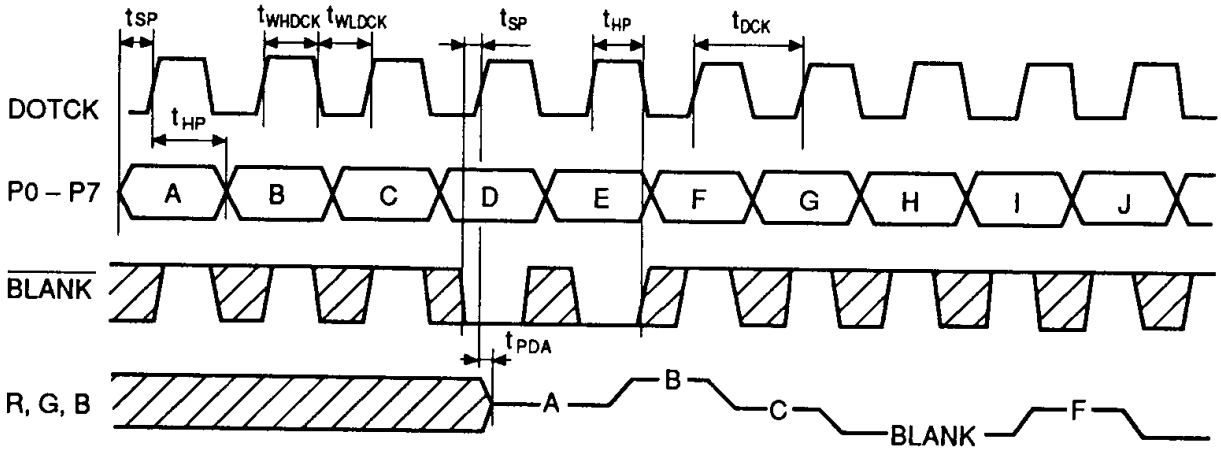
1. Write address information into the address register.
2. Apply each NRZ data at D0 to D5 inputs in the order of red, green and blue. Total 18 bits of R, G, B data are written into CLT, simultaneously.
3. When data write is completed, the address information increases by 1. Continuously, the next data is applied in the order of R, G and B to be written.

Figure 7 Data Write to CLT



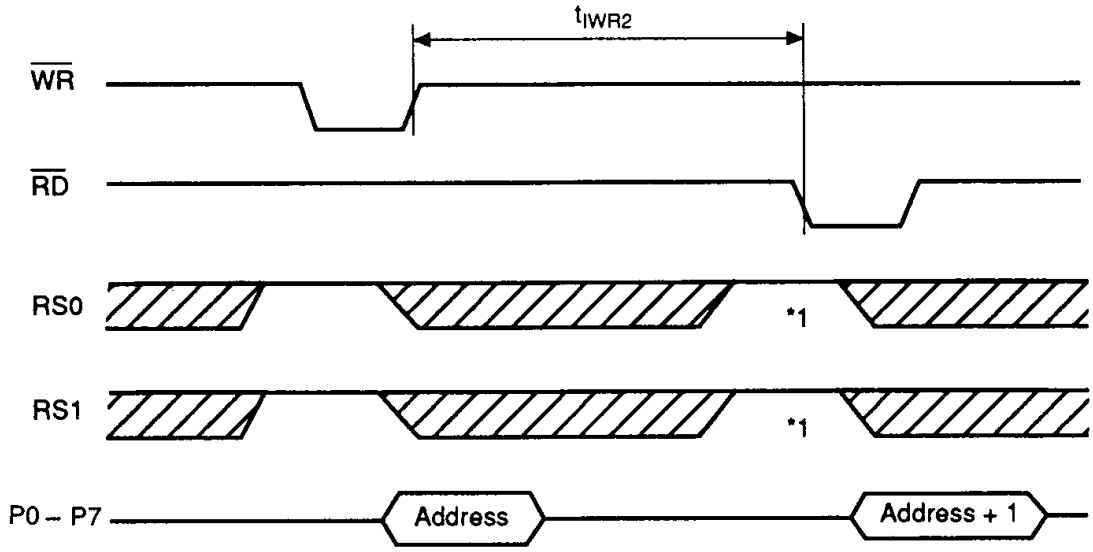
1. Read address is written into the address register.
2. By $\overline{RD}$, the contents of CLT is read out from D0 to D5 in the order of R, G and B.
3. When the data is read out until blue, the address increases by 1. Then the next address can be read out in the order of R, G and B.

Figure 8 Read Out from CLT



Video output provides data at the address indicated by address data P0 – P7, as analog signal outputs. Then, the video signal output delays by 3 clocks from the clock of the address taken into by DOTCK.

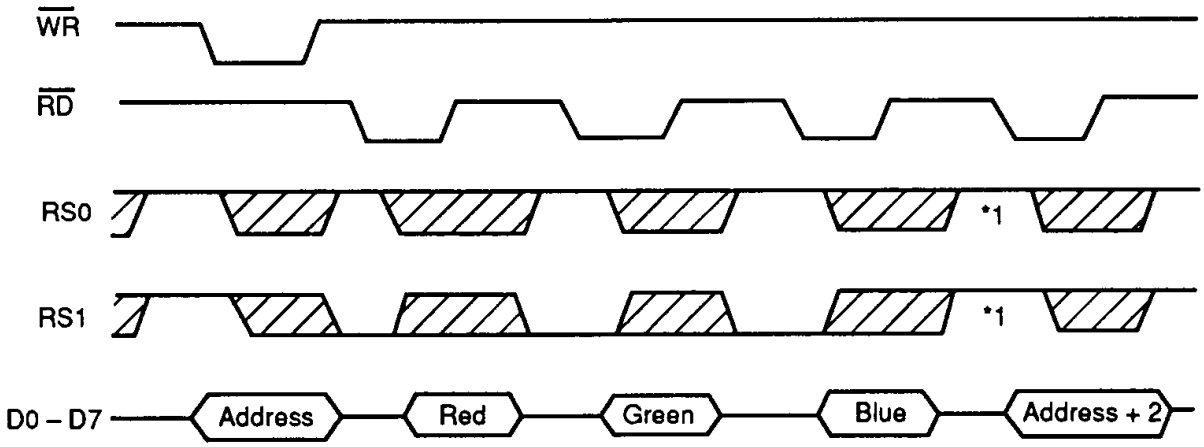
Figure 9 Video Output



1. By $\overline{WR}$, the read address is written.
2. By $\overline{RD}$, the information of an address register is read out. Then, the address information read out is +1 increased one.

Note: 1. Address register can be read out even when RS0 and RS1 are 'L' and 'L'.

Figure 10 Read Out of Address Register (1)



1. By $\overline{WR}$, the read address is written.
2. By $\overline{WR}$, CLT contents are read out in the order of red, green and blue.
3. By $\overline{RD}$, address register informations are read out. Then, the address information to be read out is +2 increased one, corresponding to the count up of reading red, green and blue.

Note: 1. Address register can be read out even when RS0 and RS1 are 'L' and 'L'.

Figure 11 Read Out of Address Register (2)

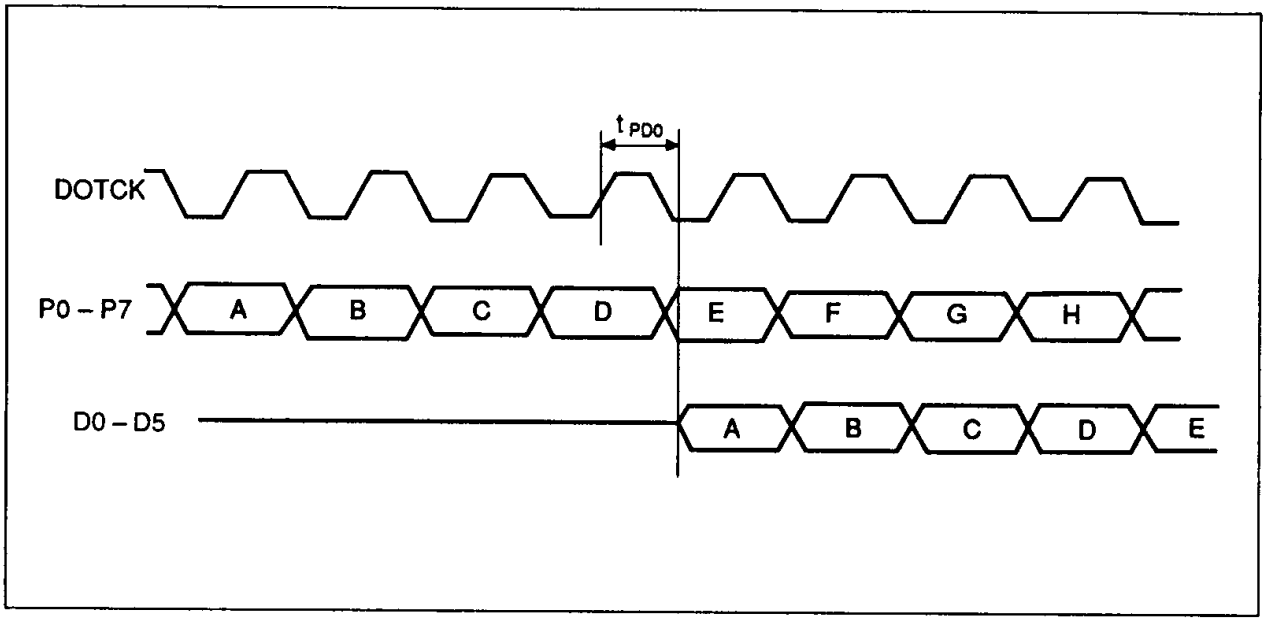


Figure 12 Digital Output

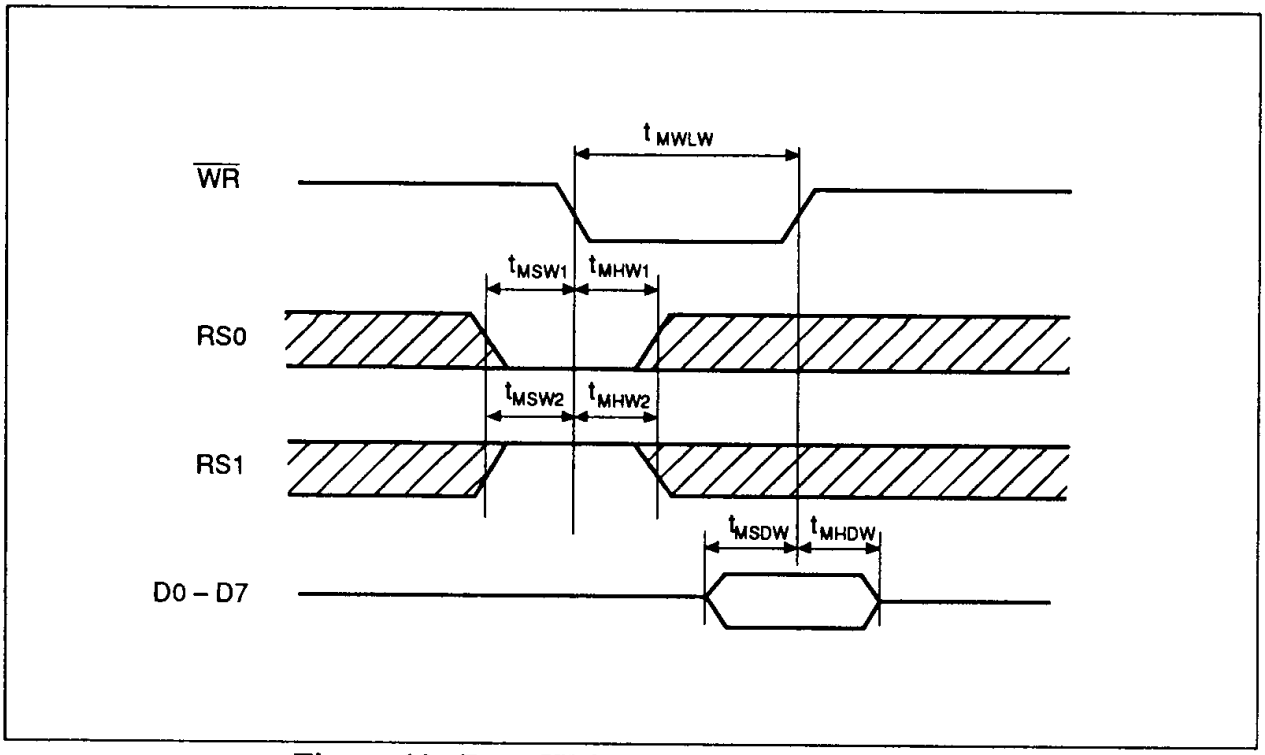


Figure 13 Data Write to Pixel Mask Register

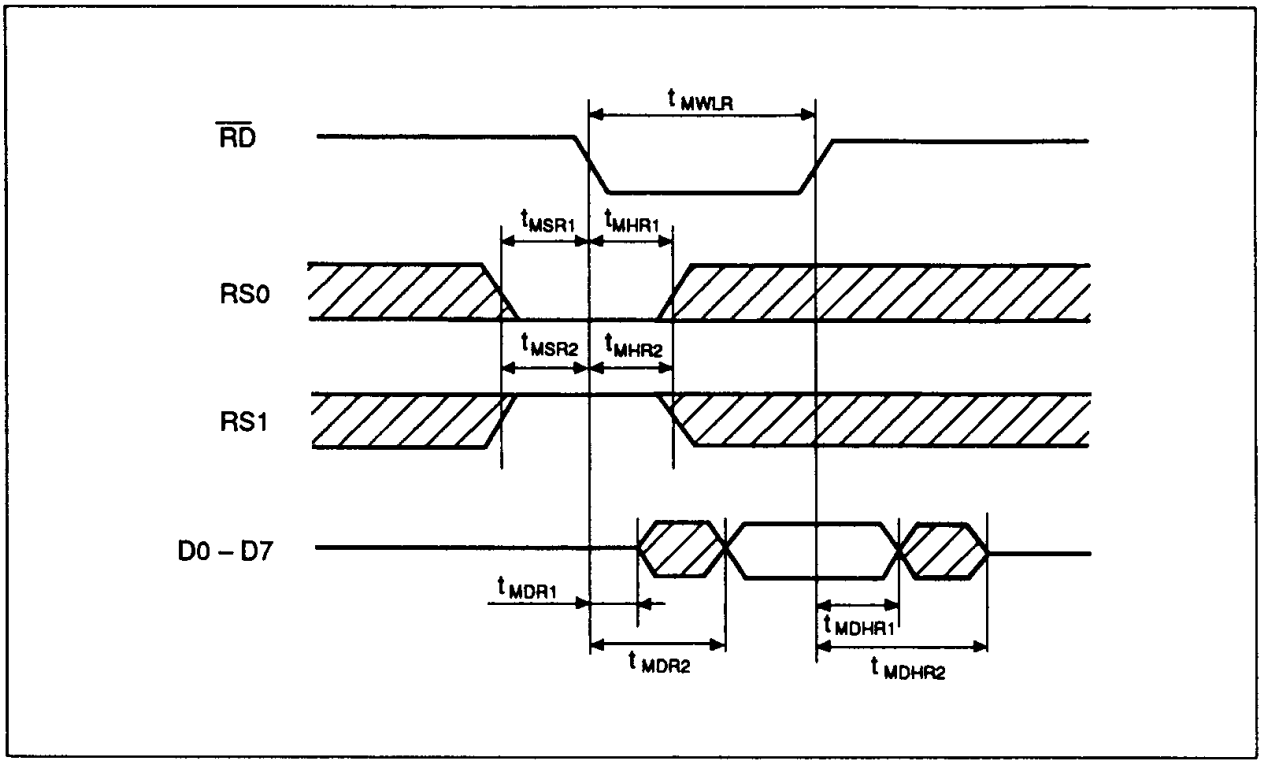


Figure 14 Read Out from Pixel Mask Register

The following two levels are selectable for the video output by fixing BSEL 'L' or 'H'.
Please select according to the CRT spec.

When SYNC signals are not composed, the output waveforms will be like;

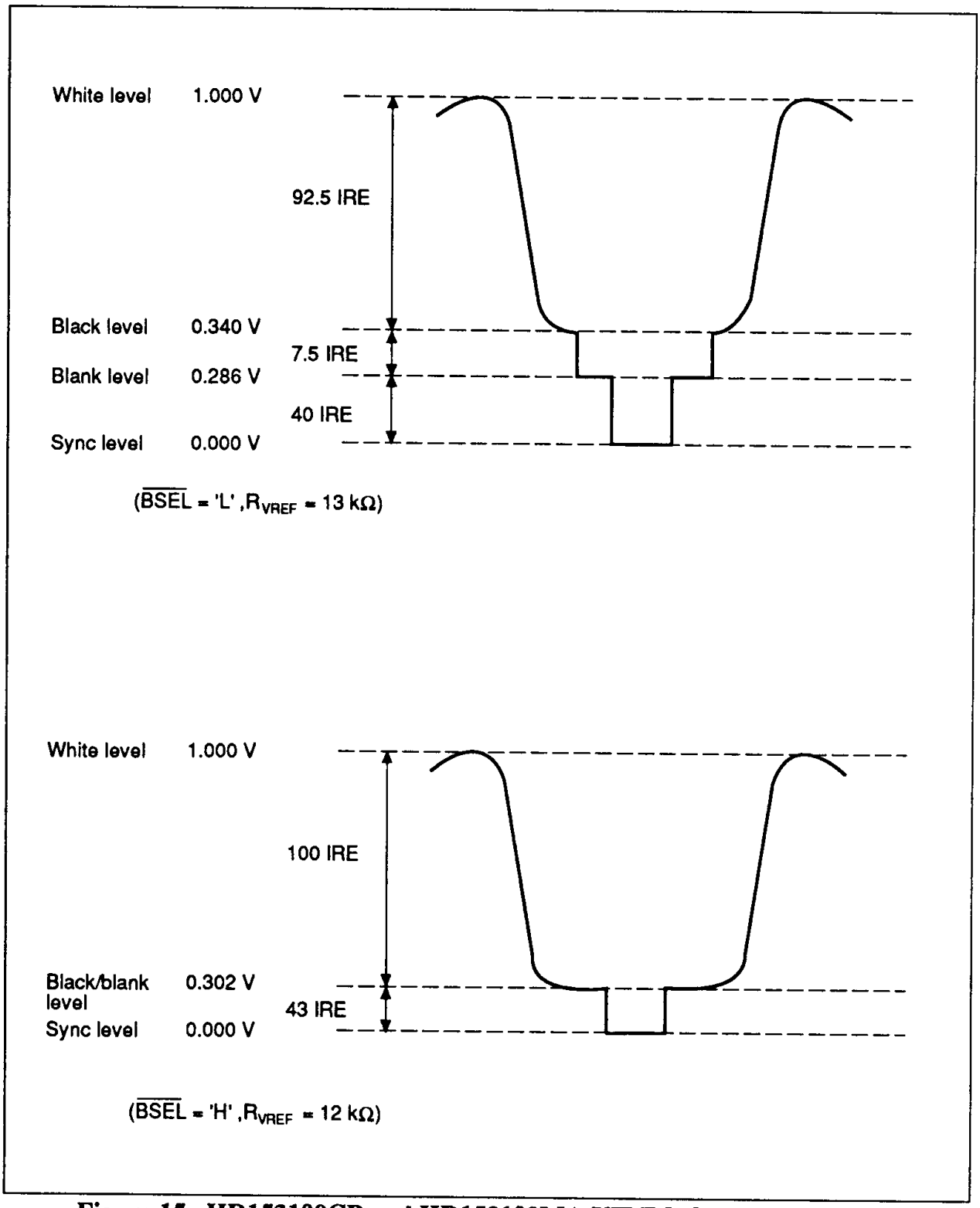


Figure 15 HD153109CP and HD153109MA VIDEO Output Waveform (In case of $\overline{\text{SYNC}}$ signal composite)

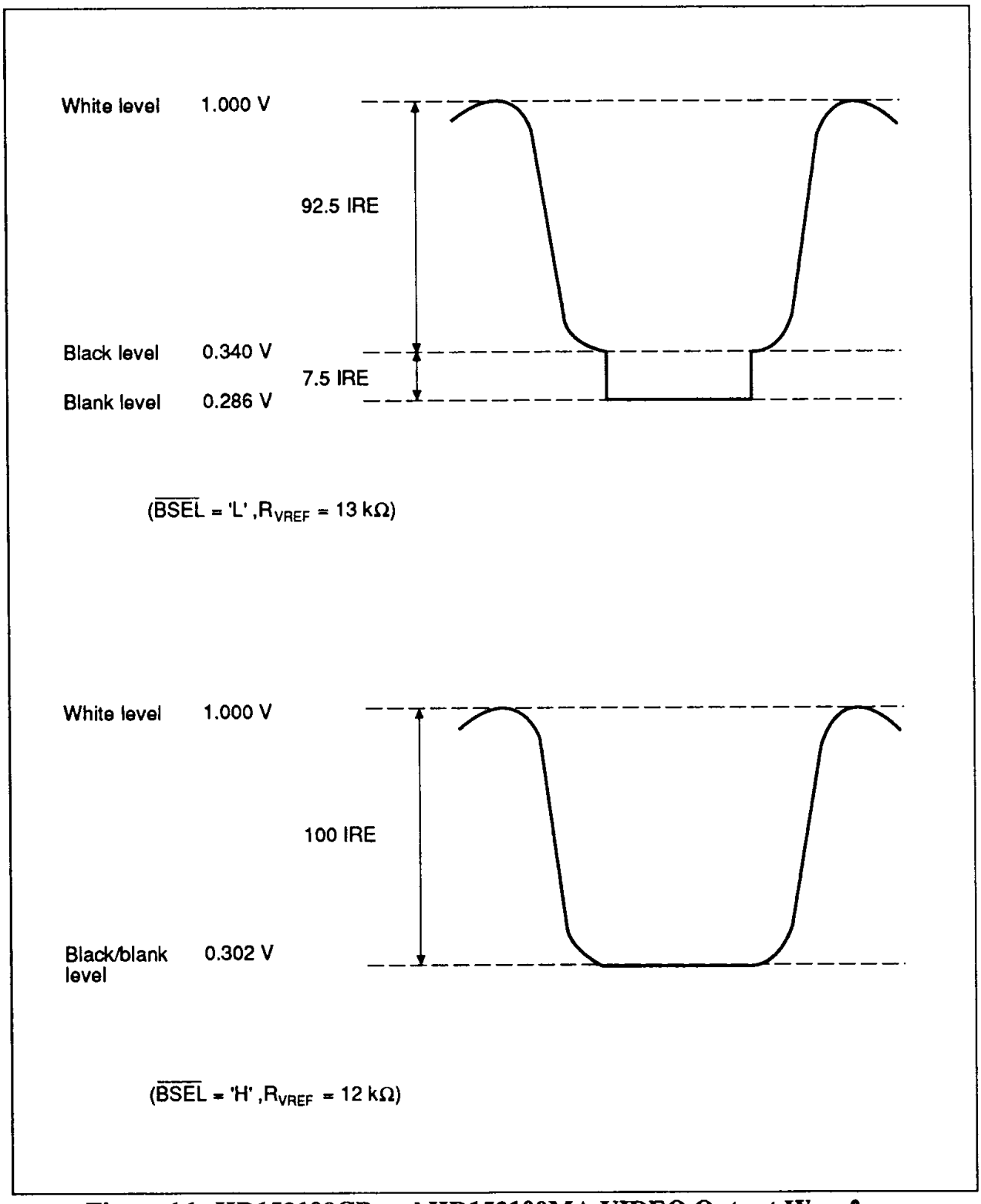
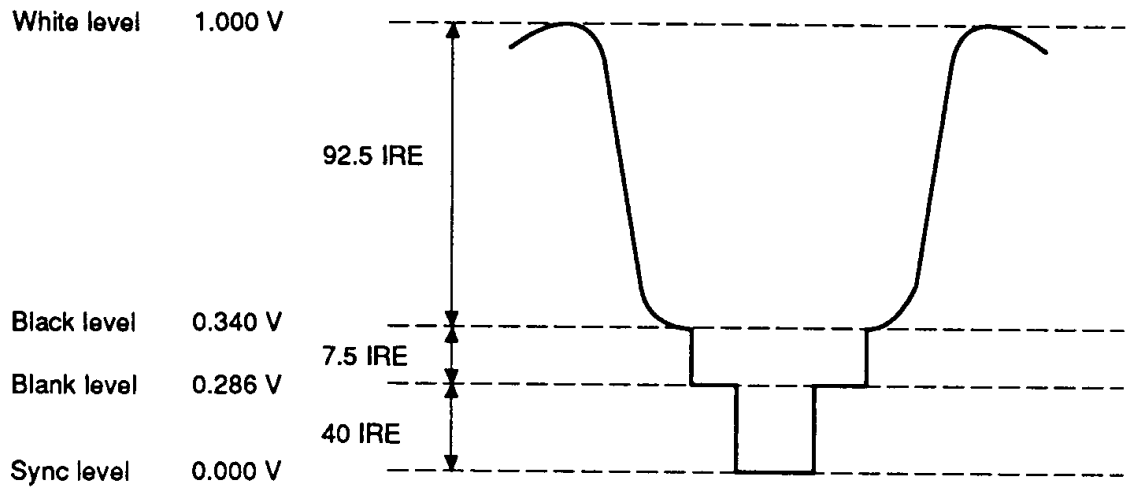
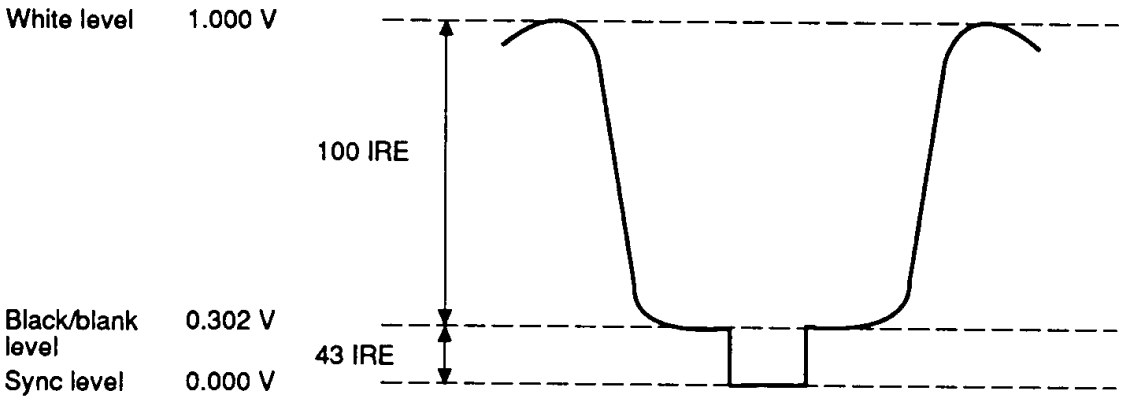


Figure 16 HD153109CP and HD153109MA VIDEO Output Waveform (In case of $\overline{\text{SYNC}}$ signal non-composite)

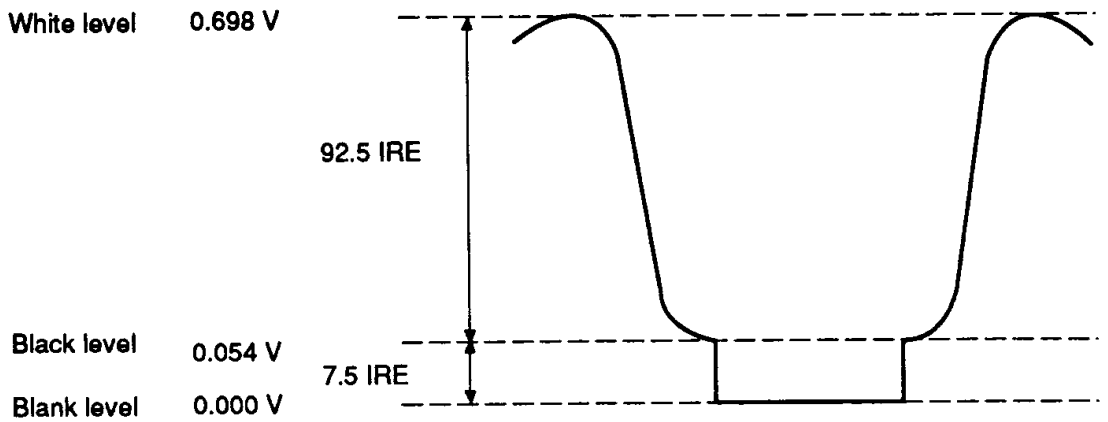


(SSEL = 'H', $\overline{BSEL}$ = 'L', R_{VREF} = 13 kΩ)

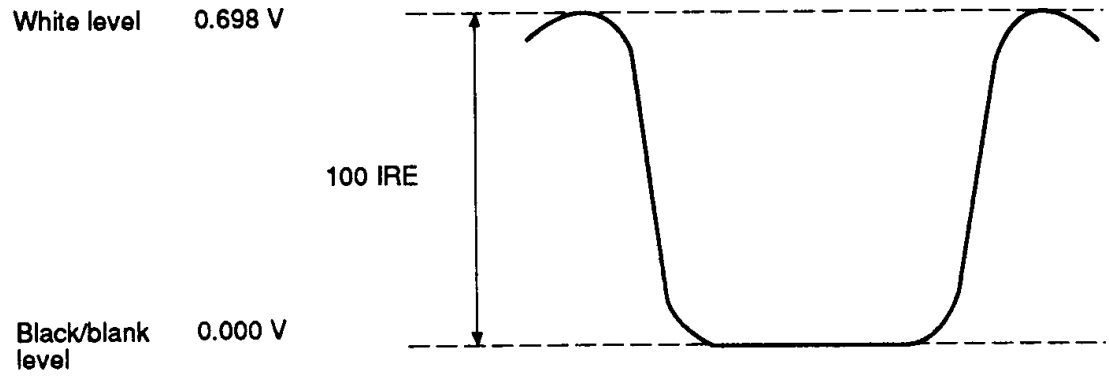


(SSEL = 'H', $\overline{BSEL}$ = 'H', R_{VREF} = 12 kΩ)

Figure 17 HD153109FS VIDEO Output Waveform (In case of $\overline{SYNC}$ signal composite)



(SSEL = 'L', $\overline{BSEL}$ = 'L' ,R_{VREF} = 13 kΩ)



(SSEL = 'L', $\overline{BSEL}$ = 'H' ,R_{VREF} = 12 kΩ)

Figure 18 HD153109FS VIDEO Output Waveform (Incase of $\overline{SYNC}$ signal non-composite)

Switch of DAC outputs and Digital Output: OSL1 and OSL2 are used to switch the DAC output and digital output. (See table 4)

Table 4

OSL1	OSL2	Output
0	0	DAC output
1	1	DAC output and digital output (green)
0	1	Prohibited
1	0	Prohibited

Correspondance of CLT with Each Register

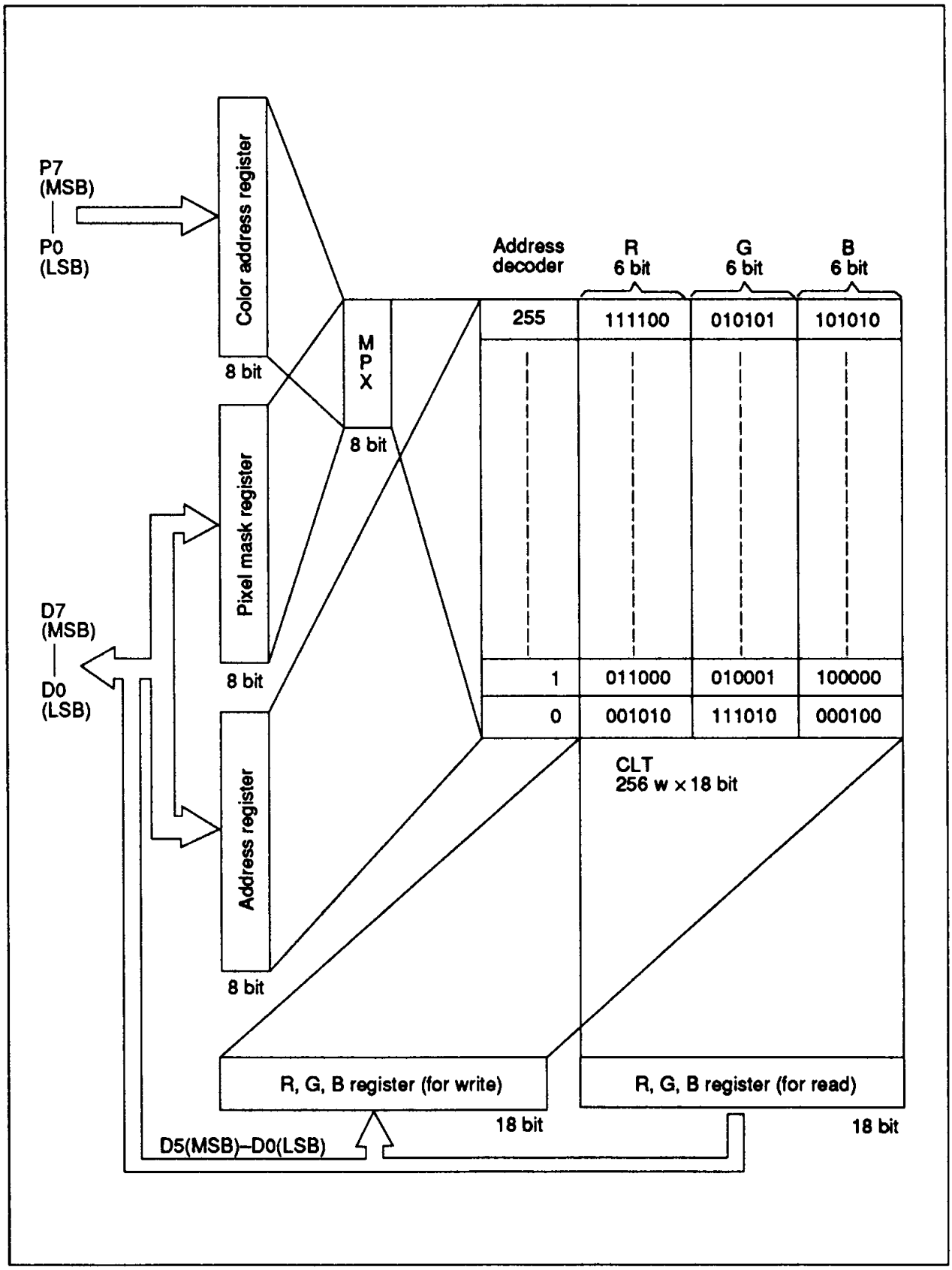


Figure 19 Correspondance of CLT with Each Register

Example Construction of a Standard System

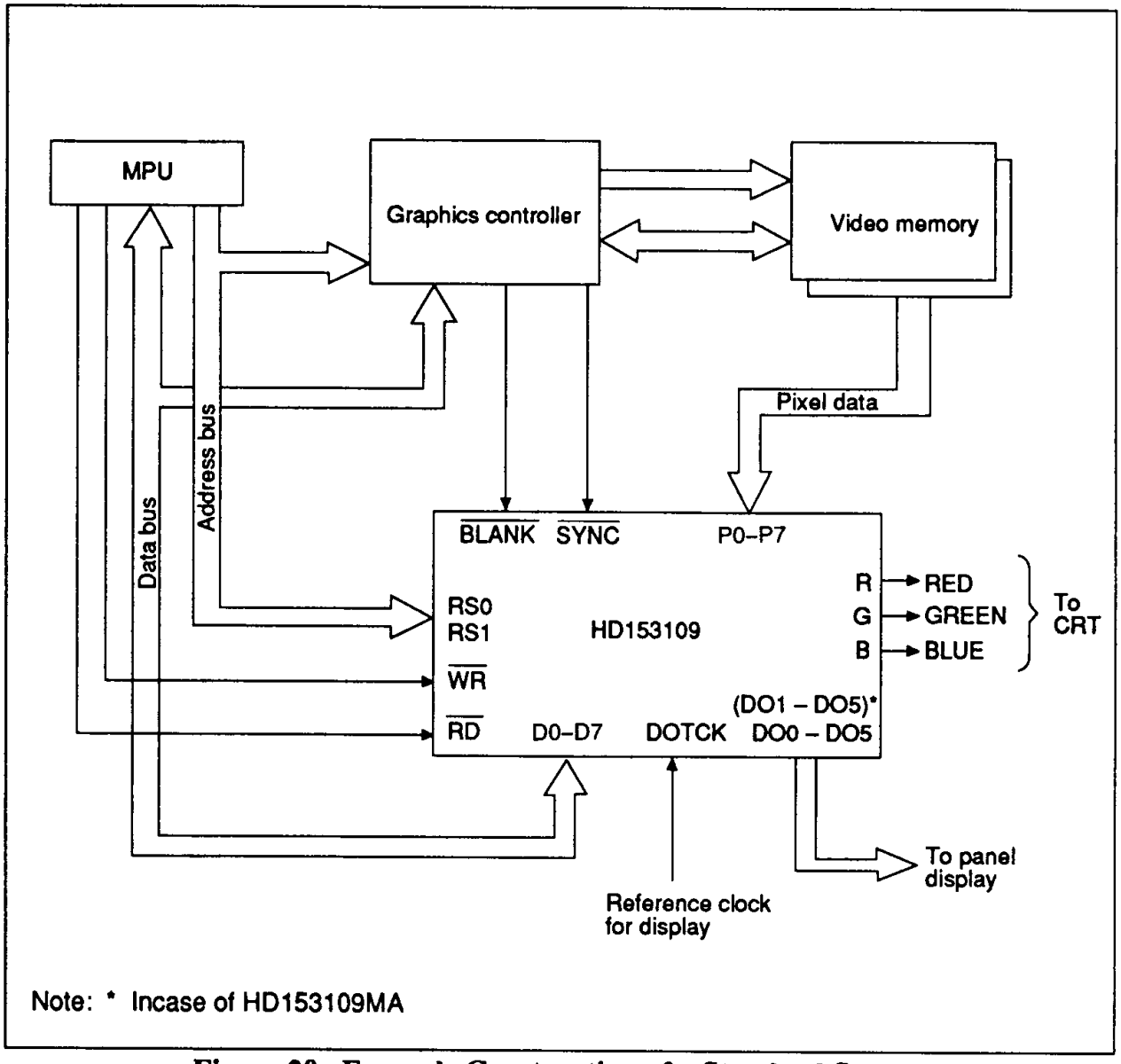


Figure 20 Example Construction of a Standard System

Table 5 Absolute Maximum Ratings (Ta = 25 °C)

Item	Symbol	Rating	Unit
Power supply voltage	V_{CC}	7.0	V
Input voltage	V_{IN}	0 to V_{CC}	V
Operating temperature	T_{opr}	0 to +70 (+60)*	°C
Storage temperature	T_{str}	–55 to +150	°C

Note: * HD153109MA only

Electrical Characteristics

Table 6 DAC Characteristics (V_{CC} = 5 V, Ta = 25 °C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Resolution		6	6	6	bits	
Max. operating frequency	f_{CLK}	—	—	50/65	MHz	
Analog output voltage (R_{VREF} = 12 kΩ)	V_A(Full)	–15	—	15	% of FSR	
	V_A(Zero)	–2	—	2	% of FSR	
Differential linearity	DLE	–1	—	+1	LSB	
Integral linearity	ILE	–1	—	+1	LSB	
Output rise time (20 % to 80 %)	tr	—	—	10	ns	C_L = 15 pF
Output fall time (80 % to 20 %)	tf	—	—	10	ns	C_L = 15 pF
Setting time	ts	—	—	30	ns	C_L = 15 pF
Glitch energy	E_G	—	90	—	PVS	

Table 7 DC Characteristics

(Unless otherwise specified, V_{CC} = 5 V + 5 %, Ta = 0 to +70 °C, (Ta = 0 to +60 °C)*1)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Input "High" level voltage	V_{IH}	2.0	—	V_{CC}	V	
Input "Low" level voltage	V_{IL}	–0.3	—	0.8	V	
Input clamp voltage	V_I	—	—	–1.5	V	V_{CC} = 4.75 V I_{IN} = –18 mA
Output "High" level voltage	V_{OH}	2.7	—	—	V	V_{CC} = 4.75 V I_{OH} = –400 µA

DC Characteristics
(Unless otherwise specified, V_{CC} = 5 V + 5 %, Ta = 0 to +70 °C, (Ta = 0 to +60 °C)*1) (cont)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Output "Low" level voltage	V_{OL}	—	—	0.5	V	V_{CC} = 4.75 V I_{OL} = 8 mA
Input current	I_I	—	—	1	mA	V_{CC} = 5.25 V V_I = 5.5 V
"High" level input current	I_{IH}	_	—	20	µA	V_{CC} = 5.25 V V_I = 2.7 V
"Low" level input current	I_{IL}	—	—	–400	µA	V_{CC} = 5.25 V V_I = 0.4 v
Supply current (HD153109FS) (1)*2	I_{CC}	—	130	190	mA	V_{CC} = 5.25 V
Supply current (HD153109FS) (2)*3	I_{CC}	—	80	130	mA	V_{CC} = 5.25 V
Supply current (HD153109CP) (3)*4	I_{CC}	_	130	190	mA	V_{CC} = 5.25 V

Notes: 1. HD153109MA only
2. PS = 'H', OSL1 = 'L', OSL2 = 'L'
3. PS = 'L', OSL1 = 'H', OSL2 = 'H'
4. OSL1 = 'L', OSL2 = 'L'

Table 8 Digital Parts AC Characteristics (V_{CC} = 5 V, Ta = 25 °C)

		50 MHz		65 MHz				Refer-
Item	Symbol	Min	Max	Min	Max	Unit	Test conditions	ence figure
DOTCK cycle time	t_{DCK}	20	—	15.3	—	ns		9
DOTCK L level time	t_{WLDCK}	8	—	6	—	ns		9
DOTCK H level time	t_{WHDCK}	8	—	6	—	ns		9
Data setup time	t_{sp}	6	—	5	—	ns		9
Data hold time	t_{HP}	6	—	5	—	ns		9
Data output delay time	t_{PDA}	—	30	—	30	ns	C_L = 15 pF	9
$\overline{WR}$ L level time	t_{WLW}	50	—	50	—	ns		3, 7, 8
$\overline{WR}$ H level time	t_{WHW}	4×t_{DCK}	—	4×t_{DCK}	—	ns		7
$\overline{RD}$ L level time	t_{WLR}	50	—	50	—	ns		8
$\overline{RD}$ H level time (1)	t_{WHR1}	4×t_{DCK}	—	4×t_{DCK}	—	ns		8

Digital Parts AC Characteristics (V_{CC} = 5 V, Ta = 25 °C) (cont)

Item	Symbol	50 MHz Min	50 MHz Max	65 MHz Min	65 MHz Max	Unit	Test conditions	Reference figure
$\overline{RD}$ H level time (2)	t_{WHR2}	7×t_{DCK}	—	7×t_{DCK}	—	ns		8
$\overline{WR}$/$\overline{RD}$ interval time (1)	t_{IWR1}	4×t_{DCK}	—	4×t_{DCK}	—	ns		5, 6
$\overline{WR}$/$\overline{RD}$ interval time (2)	t_{IWR2}	7×t_{DCK}	—	7×t_{DCK}	—	ns		5, 6, 8, 9
$\overline{WR}$/RS0, RS1 setup time	t_{SW}	10	—	10	—	ns		3
$\overline{WR}$/RS0, RS1 hold time	t_{HW}	10	—	10	—	ns		3
$\overline{RD}$/RS0, RS1 setup time	t_{SRR}	10	—	10	—	ns		4
$\overline{RD}$/RS0, RS1 hold time	t_{HRR}	10	—	10	—	ns		4
$\overline{WR}$ data setup time	t_{SDW}	10	—	10	—	ns		3
$\overline{WR}$ data hold time	t_{HDW}	10	—	10	—	ns		3
$\overline{RD}$ data output delay time (1)	t_{DDR1}	5	—	5	—	ns	C_L = 15 pF	4
$\overline{RD}$ data output delay time (2)	t_{DDR2}	—	40	—	40	ns	C_L = 15 pF	4
$\overline{RD}$ data output hold time (1)	t_{HDR1}	5	—	5	—	ns	C_L = 15 pF	4
$\overline{RD}$ data output hold time (2)	t_{HDR2}	—	20	—	20	ns	C_L = 15 pF	4
Digital output delay time	t_{PD0}	—	19	—	19	ns	C_L = 15 pF	12
$\overline{WR}$ L level time	t_{MWLW}	50	—	50	—	ns		13
$\overline{RD}$ L level time	t_{MWLR}	50	—	50	—	ns		14
$\overline{WR}$/RS0, RS1 setup time	t_{MSW1}	10	—	10	—	ns		13
	t_{MSW2}	10	—	10	—	ns		13
$\overline{WR}$/RS0, RS1 hold time	t_{MHW1}	10	—	10	—	ns		13
	t_{MHW2}	10	—	10	—	ns		13
$\overline{RD}$/RS0, RS1 setup time	t_{MSR1}	10	—	10	—	ns		14
	t_{MSR2}	10	—	10	—	ns		14
$\overline{RD}$/RS0, Rs1 hold time	t_{MHR1}	10	—	10	—	ns		14
	t_{MHR2}	10	—	10	—	ns		14
$\overline{WR}$ data setup time	t_{MSDW}	10	—	10	—	ns		13

2

Digital Parts AC Characteristics (V_{CC} = 5 V, Ta = 25 °C) (cont)

Item	Symbol	50 MHz Min	50 MHz Max	65 MHz Min	65 MHz Max	Unit	Test conditions	Reference figure
$\overline{WR}$ data hold time	t_{MHDW}	10	—	10	—	ns		13
$\overline{RD}$ data output delay time (1)	t_{MDR1}	5	—	5	—	ns	C_L = 15 pF	14
$\overline{RD}$ data output delay time (2)	t_{MDR2}	—	40	—	40	ns	C_L = 15 pF	14
$\overline{RD}$ data output hold time (1)	t_{MDHR1}	5	—	5	—	ns	C_L = 15 pF	14
$\overline{RD}$ data output hold time (2)	t_{MDHR2}	—	20	—	20	ns	C_L = 15 pF	14

Example of External Parts

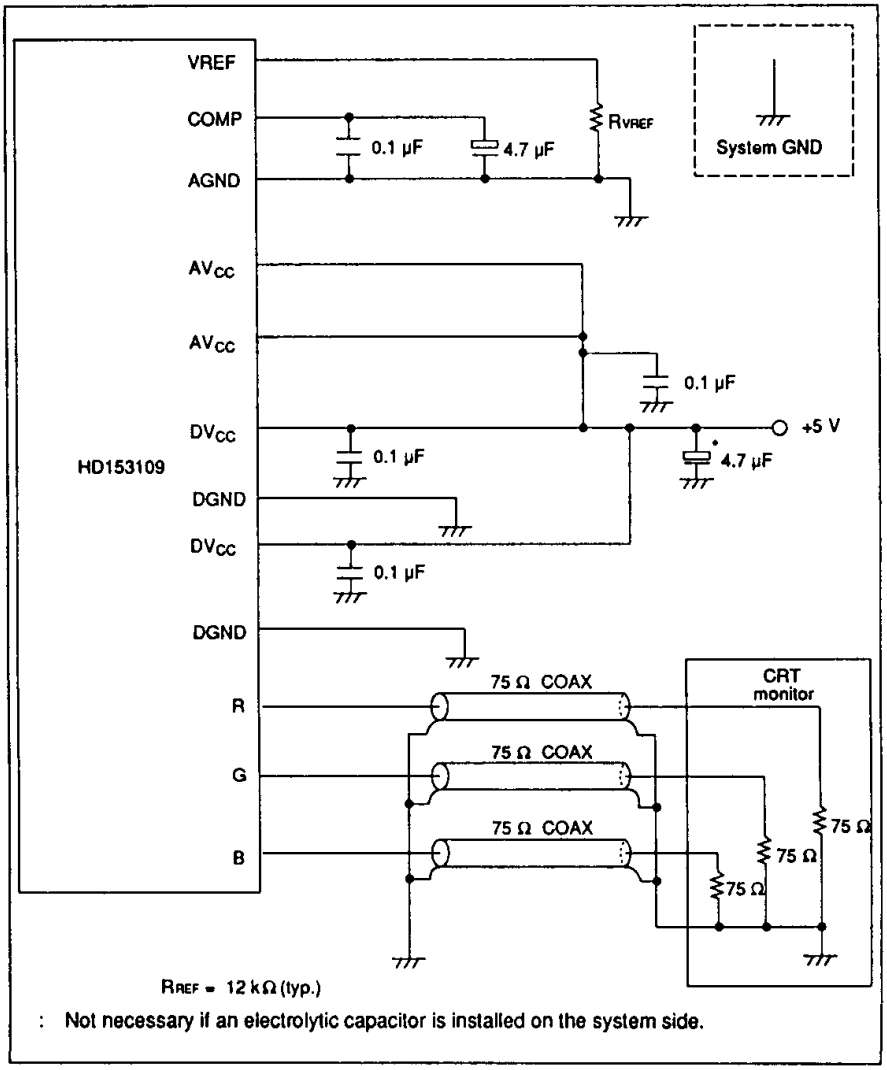


Figure 21 Example of External Parts