HD153108

Color Palette with Triple 4-bit DA Converters

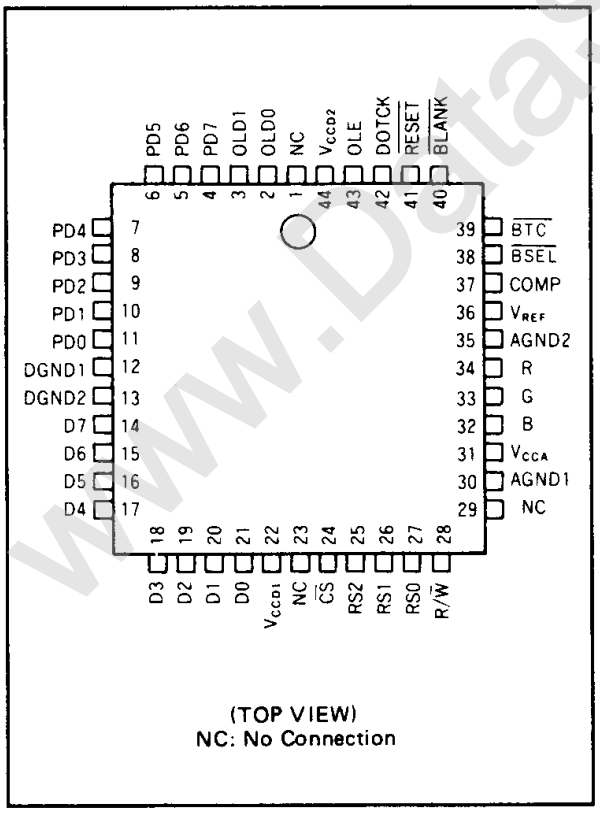
The HD153108 is a triple 4 bit video DAC with dual port RAM, designed specifically for high performance, high resolution color graphics. The HD153108 supports up to 256 simultaneous colors from a 4096 color palette and generates RS-343-A compatible red, green and blue video signals.
The HD153108 realizes high speed, high density and low power dissipation by implementing in Hi-BiCMOS.

Features

- Displays 256 colors simultaneously among total 4096 colors.
- Provides R-G-B 3 channels 4 bit D/A converter on a chip.
- Blanking input to control display.
- Overlay displaying applied for cursor or menu.
- Built in overlay color register to select any 4 colors among 4096 colors.
- Supporting TTL interface.
- Maximum Dotting Rate of 50MHz.
- Utilizing Hi-BiCMOS process of super high speed and low power dissipation.

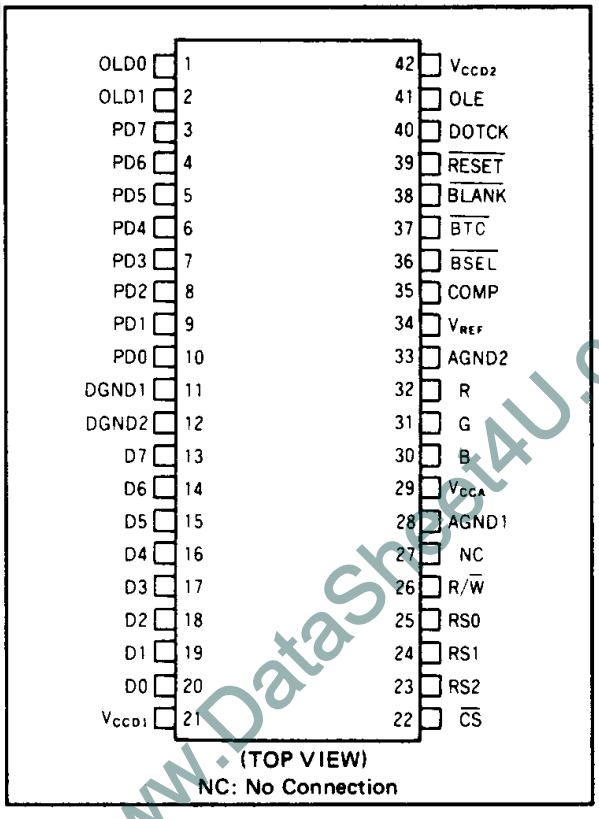
Pin Arrangement

• 44 pin PLCC (CP-44)



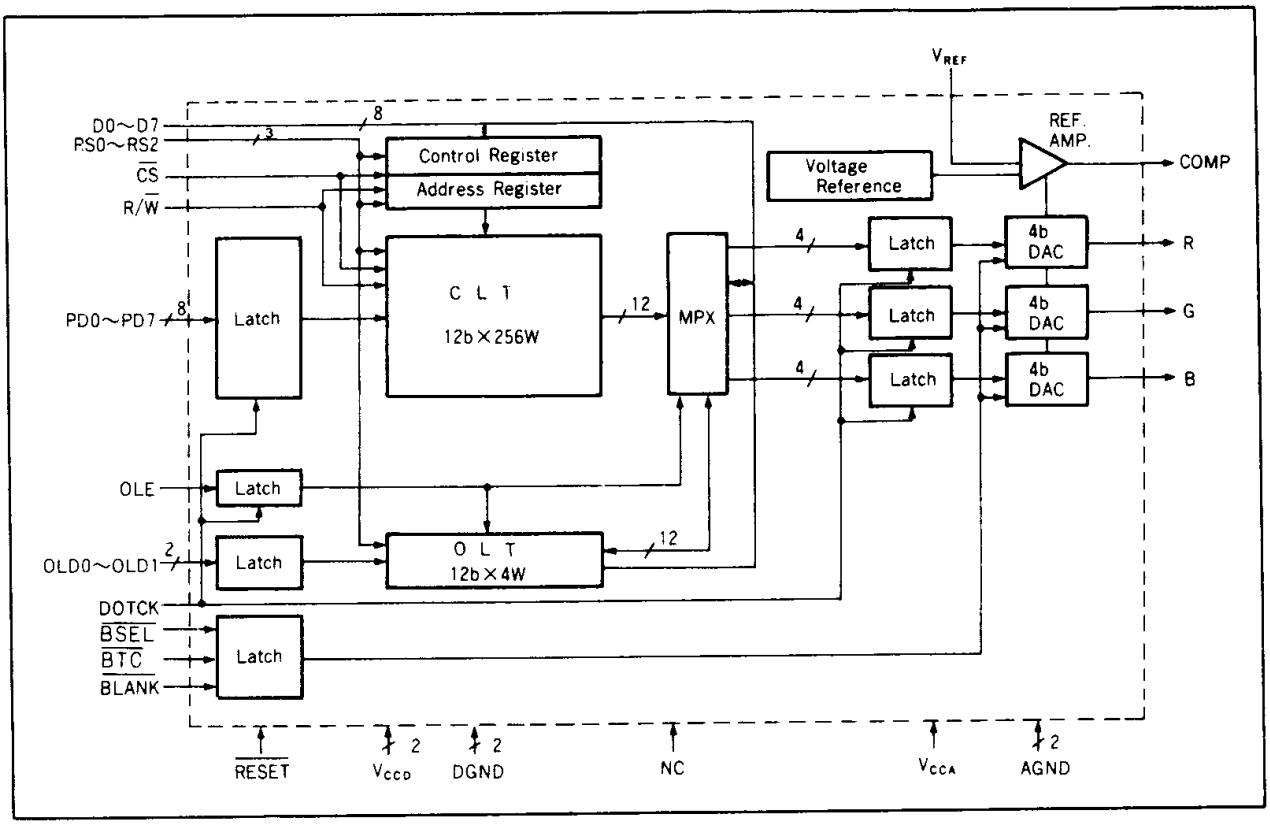
(TOP VIEW)
NC: No Connection

• 42 pin Shrink DIP (DP-42S)



(TOP VIEW)
NC: No Connection

Block Diagram



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Pin Description

Pin Name	Pin Number (*)	Description
NC	1, 23, 29 (–, –, 27)	No Connection pin. Usual GNDed.
OLD0, OLD1	2, 3 (1, 2)	Overlay select inputs.
PD0–PD7	11, 10, 9, 8, 7, 6, 5, 4 (10, 9, 8, 7, 6, 5, 4, 3)	Pixel select inputs.
D0–D7	21, 20, 19, 18, 17, 16, 15, 14 (20, 19, 18, 17, 16, 15, 14, 13)	Data input/output terminal when writing/reading CLT. OLT and registers (Address Register, RGB Register, Read Mask Register, Blink Mask Register, Overlay Control Register, Blink Timing Register).
DGND1	12 (11)	Digital ground.
DGND2	13 (12)	Digital ground.
$\overline{CS}$	24 (22)	Chip select control input when writing/reading CLT, OLT.
RS0–RS2	27, 26, 25 (25, 24, 23)	Terminal to select CLT, OLT and registers. For selection, see register mapping in Table 1.1.
R/$\overline{W}$	28 (26)	Terminal to switch write/read modes of CLT, OLT and registers. The R/$\overline{W}$ signal is activated at CS="0", and R/W="1" takes read mode and R/$\overline{W}$="0" takes write mode.
V_{CCD1}	22 (21)	Digital power.
V_{CCD2}	44 (42)	Digital power.
AGND1	30 (28)	Analog ground.
AGND2	35 (33)	Analog ground.
B	32 (30)	DAC(Blue) analog output.
G	33 (31)	DAC(Green) analog output.
R	34 (32)	DAC(Red) analog output.
V_{REF}	36 (34)	Terminal to connect a reference resistor. A reference resistor must be connected between this terminal and AGND1.
COMP	37 (35)	Terminal to connect a capacitor for phase-compensation. A 0.1μF capacitor and a 4.7μF capacitor must be connected between COMP and AGND1.
$\overline{BSEL}$	38 (36)	Input terminal to set BLANK level. At $\overline{BSEL}$ = "0", the BLANK level is set. At $\overline{BSEL}$ = "1", it's not set. When set, the BLANK level will be 7.5 IRE.
$\overline{BTC}$	39 (37)	Input terminal to provide reference clock when setting the blink timing. For the concrete setting method, refer to the section of blink timing register below. Normally, vertical synchronizing signal is provided.
$\overline{BLANK}$	40 (38)	Composite blank control input. When $\overline{BLANK}$="0". DAC output becomes blank level in any CLT and OLT.

Pin Name	Pin Number (*)	Description
$\overline{RESET}$	41 (39)	Reset signal input for all the F/F in digital part. At $\overline{RESET}$="0", they are reset and initialized.
DOTCK	42 (40)	Clock input to do operation of digital and analog parts. Operating speed is determined by the speed of this clock. When this clock rises, CLT and OLT addresses and each input data of $\overline{BSEL}$, $\overline{BTC}$ and $\overline{BLANK}$ are taken, and analog signals are output. And, it's also used as the reference clock on writing into CLT and OLT.
OLE	43 (41)	Signal input to switch CLT and OLT. OLT is selected at OLE="1" and at OLE="0" CLT is selected. However, when OLE="1", OLD0, OLD1="0" and b6 of overlay control register="1", CLT can be selected.
VCCA	31 (29)	Analog power.

(*) Pin numbers at the upper column indicate those of PLCC-44 and the figures in parentheses at the lower column indicate those of DILP-42 shrink.

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Functional Description

1. Address Register

Address Register is selected by input signal at RS0–RS2 Pins. (Table 1.1) The less significant 2 bits of the register are used as R.G.B pointer, and the more significant 8 bits are used to select words of CLT (Color Lookup Table) and OLT (Overlay Table). (Table 2)

Table 1.1 Register Mapping

RS2	RS1	RS0	Register Contents
0	0	0	Address Register (A0–A9)
0	0	1	Color Lookup Table
0	1	0	Reserved
0	1	1	Overlay Table
1	0	0	Read Mask Register
1	0	1	Blink Mask Register
1	1	0	Overlay Control Register (See Table 1.2)
1	1	1	Blink Timing Register

Table 1.2 Overlay Control Register

Address of Register	Controls
b7	Reserved
b6	CLT Enable
b5	Reserved
b4	Reserved
b3	OLD1 Blink Mask
b2	OLD0 Blink Mask
b1	OLD1 Read Mask
b0	OLD0 Read Mask

Table 2 Address Register Function

Address Register	Value	RS1	Selected Block
A0–A1	00		Red
	01		Green
	10		Blue
A2–A9	$00–$FF	0	Color Lookup Table
	$00	1	Overlay Color 0
	$01	1	Overlay Color 1
	$02	1	Overlay Color 2
	$03	1	Overlay Color 3

2. Access to CLT/OLT

CLT/OLT are accessed by the unit of R, G or B set and the word is selected by address information in the address register. When addresses are written from D0–D7 to A2–A9, A0–A1 are initialized to select R.
Once, initialized, each access to select CLT/OLT increases A0–A1 to select in the order or R→G→B. Written data to R and G are latched internally until the data is written to B, write to R, G and B is taken simultaneously. After access to B, A2–A9 increase by 1 and A0–A1 select R. (Table 3)

During the OLE terminal is "Low". CLT output of the address defined by PD7–PD0 is selected to be displayed. During OLE "High", OLT output defined by OLD1–OLD0 is displayed. However, even if OLE is "High", OLE0, OLE1="0" and b6 of overlay control register is "High", CLT can be selected (Table 4.)

Table 3 Read/Write Operation Truth Table

	R/$\overline{W}$	RS2	RS1	RS0	A1	A0	Functions
CLT	0	0	0	0	–	–	Write to Address Register ; D0–D7→A2–A9, 00→A0–A1
	0	0	0	1	0	0	Write R(red) data ; +1 increment for A0–A9
	0	0	0	1	0	1	Write G(green) data ; +1 increment for A0–A9
	0	0	0	1	1	0	Write B(blue) data ; +2 increment for A0–A9
	1	0	0	0	–	–	Read from Address Register ; A2–A9→D0–D7, 00→A0–A1
	1	0	0	1	0	0	Read R(red) data ; +1 increment for A0–A9
	1	0	0	1	0	1	Read G(green) data ; +1 increment for A0–A9
	1	0	0	1	1	0	Read B(blue) data ; +2 increment for A0–A9
OLT	0	0	0	0	–	–	Write to Address Register ; D0–D1→A2–A3, 00→A0–A1
	0	0	1	1	0	0	Write R(red) data ; +1 increment for A0–A3
	0	0	1	1	0	1	Write G(green) data ; +1 increment for A0–A3
	0	0	1	1	1	0	Write B(blue) data ; +2 increment for A0–A3
	1	0	0	0	–	–	Read from Address Register ; A2–A3→D0–D1, 00→A0–A1
	1	0	1	1	0	0	Read R(red) data ; +1 increment for A0–A3
	1	0	1	1	0	1	Read G(green) data ; +1 increment for A0–A3
	1	0	1	1	1	0	Read B(blue) data ; +2 increment for A0–A3

Table 4 Pixel Selection & Overlay Control Truth Table

OLE	OLD1	OLD0	Overlay Control Register	PD7–PD0	Selected Block
0	X	X	X	$nn	Color Lookup Table ($nn)
1	0	0	0	X	Overlay color 0
1	0	1	0	X	Overlay color 1
1	1	0	0	X	Overlay color 2
1	1	1	0	X	Overlay color 3
1	0	0	1	$nn	Color Lookup Table ($nn)

3. Internal Registers

1. Read Mask Register
   Read Mask register is used to mask CLT address terminals (PD0–PD7). Read Mask register consists of 8 bits (bR0–bR7). The bR0 corresponds to PD0 and bR7 to PD7. When each bit of the register is "1", the corresponding address input terminal is masked. At "0", the mask is cancelled.
2. Blink Mask Register
   Blink Mask register is used to mask CLT address input terminals (PD0–PD7) being blink conditions. Blink Mask register of 8 bits (bB0–bB7). The bB0 corresponds to PD0 and bB7 to PD7. When each bit of the register is "1", the blink of the corresponding address input terminal is masked. At "0", the mask is cancelled.
   Accordingly, when blinking is not desired, it should normally be masked by setting all bits of the blink mask register to "1".
3. Overlay Control Register
   Overlay Control register is used for read mask of OLT address input terminals, blink mask, and switching OLT to CLT. Overlay Control register consists of 8 bits (b0–b7) (Table 1.2) and b0–b1 are used for read mask of OLD0–OLD1. b2–b3 are used for blink mask and b6 enables selection of CLT (Table 4).
4. Blink Timing Register
   Blink Timing register is used to set the blink on timing and blink off timing of CLT, OLT address input terminals. Blink Timing register consists of 8 bits (b_{T0}–b_{T7}). The least significant 4 bit bT0–bT3 set the blink on time and the most significant 4 bits bT4–bT7 set the blink off timing. Both of the blink on timing and blink off timing are set by the 4(n+1) magnifications of $\overline{BTC}$ signal cycle (Table 5.1, Table 5.2).

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Table 5.1 Blink on Time

b_{T3}	b_{T2}	b_{T1}	b_{T0}	Blink On Time
0	0	0	0	4 × t_{BTC}
0	0	0	1	8 × t_{BTC}
0	0	1	0	12 × t_{BTC}
0	0	1	1	16 × t_{BTC}
0	1	0	0	20 × t_{BTC}
0	1	0	1	24 × t_{BTC}
0	1	1	0	28 × t_{BTC}
0	1	1	1	32 × t_{BTC}
1	0	0	0	36 × t_{BTC}
1	0	0	1	40 × t_{BTC}
1	0	1	0	44 × t_{BTC}
1	0	1	1	48 × t_{BTC}
1	1	0	0	52 × t_{BTC}
1	1	0	1	56 × t_{BTC}
1	1	1	0	60 × t_{BTC}
1	1	1	1	64 × t_{BTC}

Table 5.2 Blink off Time

b_{T7}	b_{T6}	b_{T5}	b_{T4}	Blink Off Time
0	0	0	0	4 × t_{BTC}
0	0	0	1	8 × t_{BTC}
0	0	1	0	12 × t_{BTC}
0	0	1	1	16 × t_{BTC}
0	1	0	0	20 × t_{BTC}
0	1	0	1	24 × t_{BTC}
0	1	1	0	28 × t_{BTC}
0	1	1	1	32 × t_{BTC}
1	0	0	0	36 × t_{BTC}
1	0	0	1	40 × t_{BTC}
1	0	1	0	44 × t_{BTC}
1	0	1	1	48 × t_{BTC}
1	1	0	0	52 × t_{BTC}
1	1	0	1	56 × t_{BTC}
1	1	1	0	60 × t_{BTC}
1	1	1	1	64 × t_{BTC}

t_{BTC}: $\overline{BTC}$ cycle time

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply Voltage	V_{CC}	7.0	V
Input Voltage	V_{IN}	0 to V_{CC}	V
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{str}	−55 to +150	°C

Recommended Operating Conditions

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage	V_{CC}	4.75	5.00	5.25	V
Input "Low" Level Voltage	V_{IL}	0	–	0.8	V
Input "High" Level Voltage	V_{IH}	2.0	–	V_{CC}	V
Operating Temperature	T_{opr}	0	25	70	°C

Electrical Characteristics

DAC Characteristics (V_{CC} = 5V, Ta=25°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Resolution		4	4	4	bits	
Maximum Operating Frequency	f_{CLK}	–	–	50	MHz	
Analog Output Voltage (R_{VREF}=12kΩ)	V_A(Full)	−15	–	15	% of FSR	
	V_A(Zero)	− 2	–	2	% of FSR	
Differential Linearity	DLE	−1/2	–	+1/2	LSB	
Integral Linearity	ILE	−1/2	–	+1/2	LSB	
Output Rise Time (20%–80%)	tr	–	–	10	ns	C_L = 15pF
Output Fall Time (80%–20%)	tf	–	–	10	ns	C_L = 15pF
Settling Time	ts	–	–	30	ns	C_L = 15pF
Glitch Energy	E_G	–	90	–	PVS	

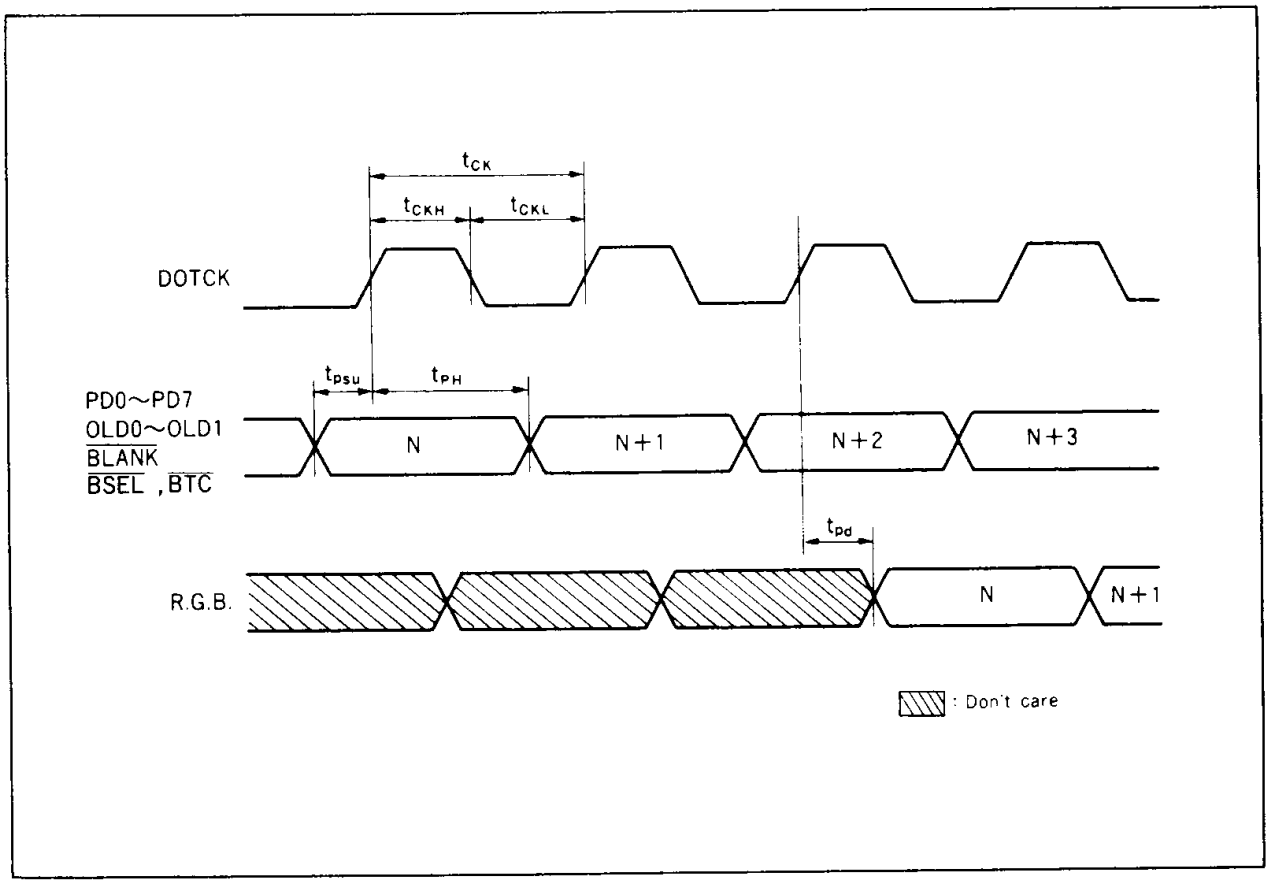
DC Characteristics (V_{CC}=5V±5%, Ta=0 to +70°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input "High" Level Voltage	V_{IH}	2.0	–	V_{CC}	V	
Input "Low" Level Voltage	V_{IL}	−0.3	–	0.8	V	
Input Clamp Voltage	V_I	–	–	−1.5	V	V_{CC} = 4.75V I_{IN} = −18mA
Output "High" Level Voltage	V_{OH}	2.7	–	–	V	V_{CC} = 4.75V I_{OH} = −400μA
Output "Low" Level Voltage	V_{OL}	–	–	0.5	V	V_{CC} = 4.75V I_{OL} = 8mA
Input Current	I_I	–	–	1	mA	V_{CC} = 5.25V V_I = 5.5V
"High" Level Input Current	I_{IH}	–	–	20	μA	V_{CC} = 5.25V V_I = 2.7V
"Low" Level Input Current	I_{IL}	–	–	−400	μA	V_{CC} = 5.25V V_I = 0.4V

Switching Characteristics

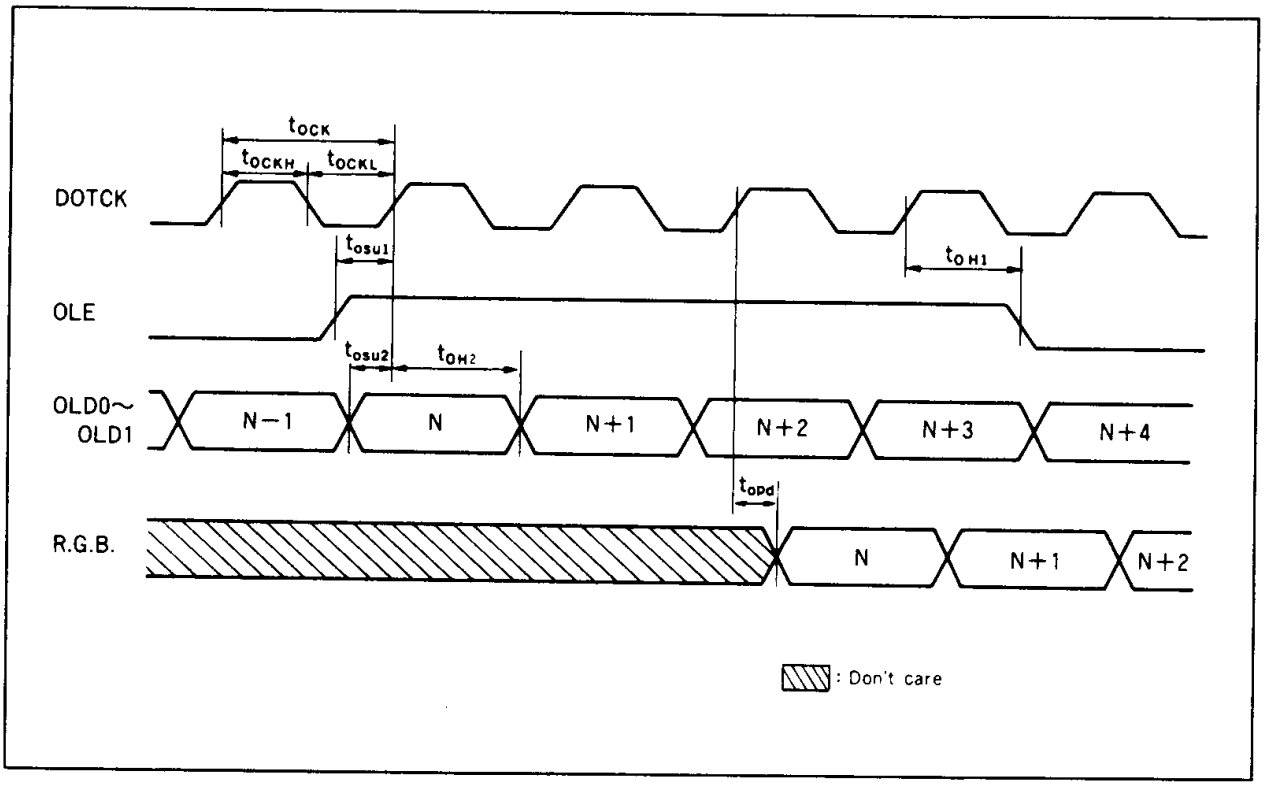
VIDEO Output (CLT) (V_{CC} = 5V, Ta = 25°C)

Item	Symbol	Min.	Max.	Unit	Test Condition
DOTCK Cycle Time	t_{CK}	20	–	ns	
DOTCK Width High	t_{CKH}	8	–	ns	
DOTCK Width Low	t_{CKL}	8	–	ns	
Data Setup Time	t_{PSU}	6	–	ns	
Data Hold Time	t_{PH}	6	–	ns	
Output Delay Time	t_{pd}	–	30	ns	C_L = 15pF



VIDEO Output (OLT) (V_{CC} = 5V, Ta = 25°C)

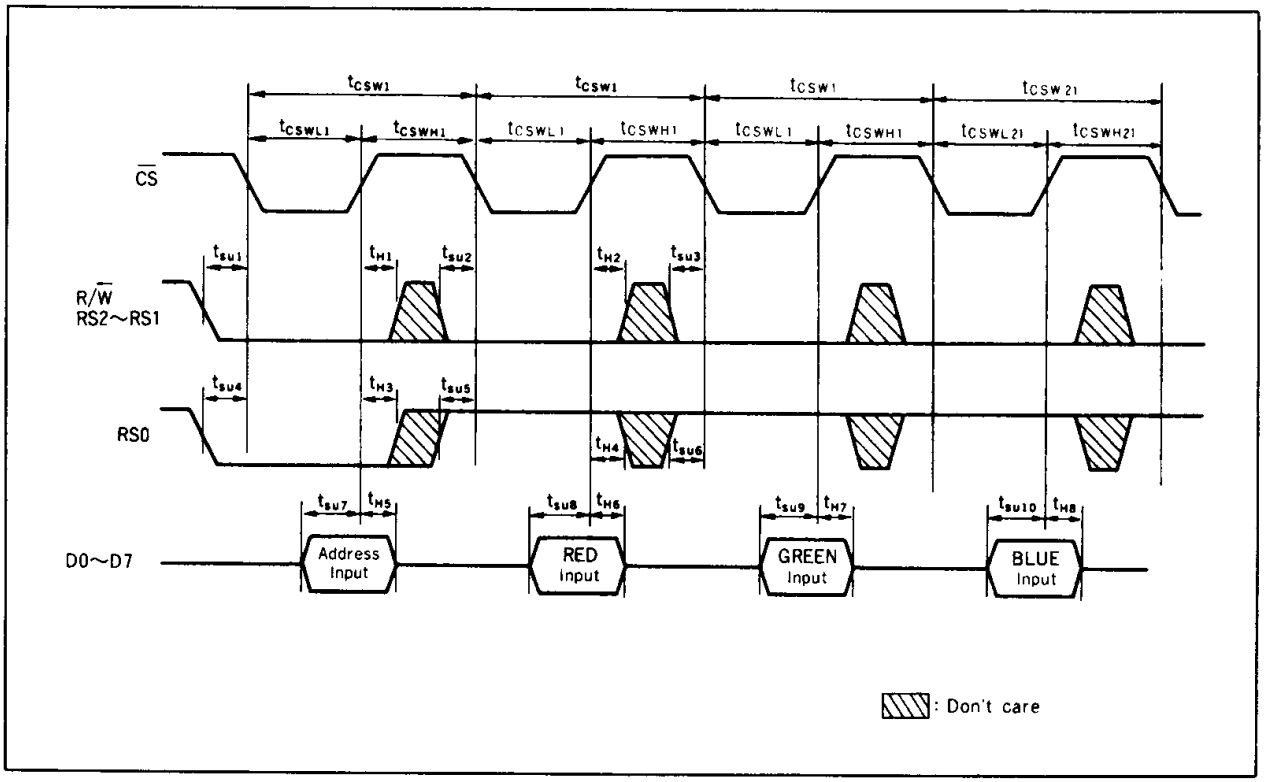
Item	Symbol	Min	Max.	Unit	Test Condition
DOTCK Cycle Time	t_{OCK}	20	–	ns	
DOTCK Width High	t_{OCKH}	8	–	ns	
DOTCK Width Low	t_{OCKL}	8	–	ns	
Data Setup Time	t_{OSU1}	6	–	ns	
Data Setup Time	t_{OSU2}	6	–	ns	
Data Hold Time	t_{OH1}	6	–	ns	
Data Hold Time	t_{OH2}	6	–	ns	
Output Delay Time	$t_{O}pd$	–	30	ns	C_L = 15pF



CLT Access (V_{CC} = 5V, Ta = 25°C)

Item	Symbol	Min.	Max.	Unit	Test Conditions
$\overline{CS}$ Cycle Time	t_{CSW1}	100	–	ns	
$\overline{CS}$ Width Low	t_{CSWL1}	50	–	ns	
$\overline{CS}$ Width High	t_{CSWH1}	50	–	ns	
R/$\overline{W}$, RS2, RS1 Setup Time	t_{SU1}	6	–	ns	
R/$\overline{W}$, RS2, RS1 Setup Time	t_{SU2}	6	–	ns	
R/$\overline{W}$, RS2, RS1 Setup Time	t_{SU3}	6	–	ns	
R/$\overline{W}$, RS2, RS1 Hold Time	t_{H1}	6	–	ns	
R/$\overline{W}$, RS2, RS1 Hold Time	t_{H2}	6	–	ns	
RS0 Setup Time	t_{SU4}	6	–	ns	
RS0 Setup Time	t_{SU5}	6	–	ns	
RS0 Setup Time	t_{SU6}	6	–	ns	
Address Data Setup Time	t_{SU7}	6	–	ns	
RED Data Setup Time	t_{SU8}	6	–	ns	
GREEN Data Setup Time	t_{SU9}	6	–	ns	
BLUE Data Setup Time	t_{SU10}	6	–	ns	
RS0 Hold Time	t_{H3}	6	–	ns	
RS0 Hold Time	t_{H4}	6	–	ns	
Address Data Hold Time	t_{H5}	6	–	ns	
RED Data Hold Time	t_{H6}	6	–	ns	
GREEN Data Hold Time	t_{H7}	6	–	ns	
BLUE Data Hold Time	t_{H8}	6	–	ns	
$\overline{CS}$ Cycle Time	t_{CSW2}	100	–	ns	
$\overline{CS}$ Width Low	t_{CSWL2}	50	–	ns	
$\overline{CS}$ Width High	t_{CSWH2}	50	–	ns	
R/$\overline{W}$, RS0 Setup Time	t_{SU11}	6	–	ns	
R/$\overline{W}$, RS0 Setup Time	t_{SU12}	6	–	ns	
R/$\overline{W}$, RS0 Setup Time	t_{SU13}	6	–	ns	
RS2, RS1 Setup Time	t_{SU14}	6	–	ns	
RS2, RS1 Setup Time	t_{SU15}	6	–	ns	
RS2, RS1 Setup Time	t_{SU16}	6	–	ns	
Address Data Setup Time	t_{SU17}	6	–	ns	
R/$\overline{W}$, RS0 Hold Time	t_{H9}	6	–	ns	
R/$\overline{W}$, RS0 Hold Time	t_{H10}	6	–	ns	
RS2, RS1 Hold Time	t_{H11}	6	–	ns	
RS2, RS1 Hold Time	t_{H12}	6	–	ns	
Address Data Hold Time	t_{H13}	6	–	ns	
RED Output Delay Time	t_{d1}	–	75	ns	C_L = 50pF
GREEN Output Delay Time	t_{d2}	–	75	ns	C_L = 50pF
BLUE Output Delay Time	t_{d3}	–	75	ns	C_L = 50pF
RED Output Hold Time	t_{HZ1}	5	–	ns	
GREEN Output Hold Time	t_{HZ2}	5	–	ns	
BLUE Output Hold Time	t_{HZ3}	5	–	ns	
$\overline{CS}$ Cycle Time	t_{CSW21}	50 + 3 x t_{CK}	–	ns	
$\overline{CS}$ Width Low	t_{CSWL21}	50	–	ns	
$\overline{CS}$ Width High	t_{CSWH21}	3 x t_{CK}	–	ns	

WRITE



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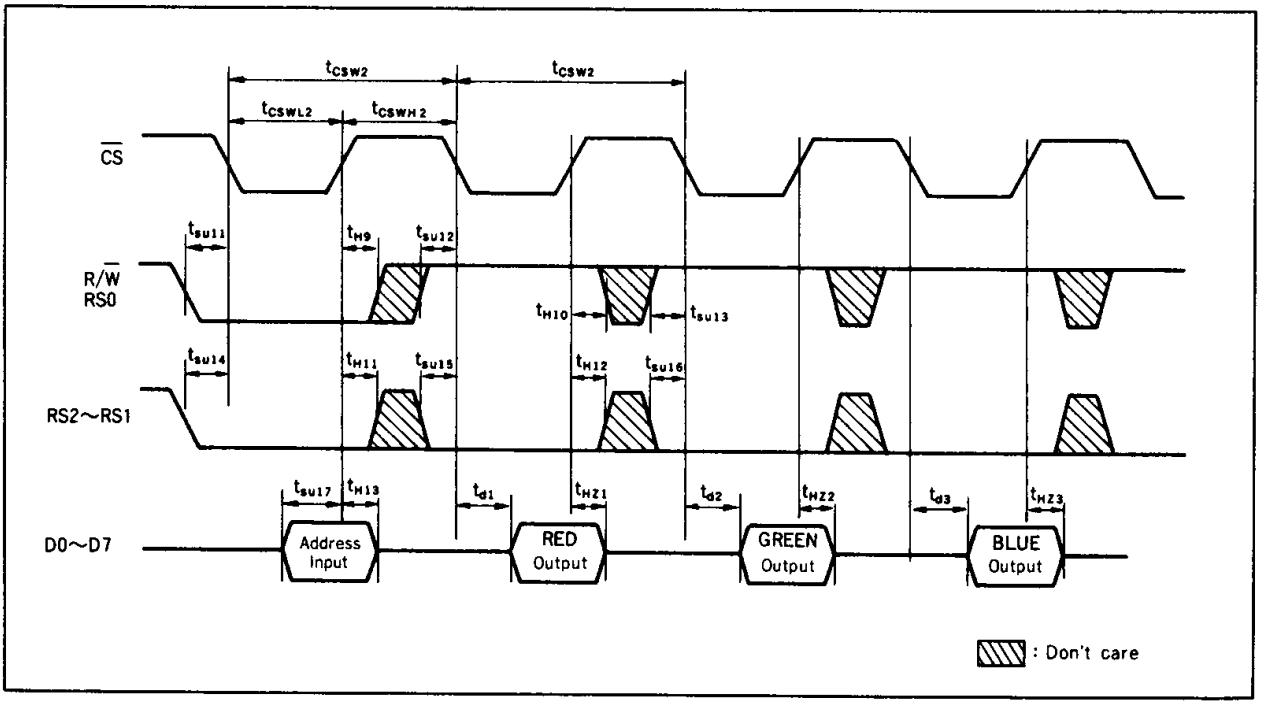

OLT Access (V_{CC} = 5V, Ta = 25°C)

Item	Symbol	Min.	Max.	Unit	Test Conditions
$\overline{CS}$ Cycle Time	t_{CSW3}	100	–	ns	
$\overline{CS}$ Width Low	t_{CSWL3}	50	–	ns	
$\overline{CS}$ Width High	t_{CSWH3}	50	–	ns	
R/$\overline{W}$, RS2 Setup Time	t_{SU18}	6	–	ns	
R/$\overline{W}$, RS2 Setup Time	t_{SU19}	6	–	ns	
R/$\overline{W}$, RS2 Setup Time	t_{SU20}	6	–	ns	
RS1, RS0 Setup Time	t_{SU21}	6	–	ns	
RS1, RS0 Setup Time	t_{SU22}	6	–	ns	
RS1, RS0 Setup Time	t_{SU23}	6	–	ns	
Address Data Setup Time	t_{SU24}	6	–	ns	
RED Data Setup Time	t_{SU25}	6	–	ns	
GREEN Data Setup Time	t_{SU26}	6	–	ns	
BLUE Data Setup Time	t_{SU27}	6	–	ns	
R/$\overline{W}$, RS2 Hold Time	t_{H14}	6	–	ns	
R/$\overline{W}$, RS2 Hold Time	t_{H15}	6	–	ns	
RS1, RS0 Hold Time	t_{H16}	6	–	ns	
RS1, RS0 Hold Time	t_{H17}	6	–	ns	
Address Data Hold Time	t_{H18}	6	–	ns	
RED Data Hold Time	t_{H19}	6	–	ns	
GREEN Data Hold Time	t_{H20}	6	–	ns	
BLUE Data Hold Time	t_{H21}	6	–	ns	
$\overline{CS}$ Cycle Time	t_{CSW4}	100	–	ns	
$\overline{CS}$ Width Low	t_{CSWL4}	50	–	ns	
$\overline{CS}$ Width High	t_{CSWH4}	50	–	ns	
R/$\overline{W}$, RS1, RS0 Setup Time	t_{SU28}	6	–	ns	
R/$\overline{W}$, RS1, RS0 Setup Time	t_{SU29}	6	–	ns	
R/$\overline{W}$, RS1, RS0 Setup Time	t_{SU30}	6	–	ns	
RS2 Setup Time	t_{SU31}	6	–	ns	
RS2 Setup Time	t_{SU32}	6	–	ns	
RS2 Setup Time	t_{SU33}	6	–	ns	
Address Data Setup Time	t_{SU34}	6	–	ns	
R/$\overline{W}$, RS1, RS0 Hold Time	t_{H22}	6	–	ns	
R/$\overline{W}$, RS1, RS0 Hold Time	t_{H23}	6	–	ns	
RS2 Hold Time	t_{H24}	6	–	ns	
RS2 Hold Time	t_{H25}	6	–	ns	
Address Data Hold Time	t_{H26}	6	–	ns	
RED Output Delay Time	t_{d4}	–	75	ns	C_L = 50pF
GREEN Output Delay Time	t_{d5}	–	75	ns	C_L = 50pF
BLUE Output Delay Time	t_{d6}	–	75	ns	C_L = 50pF
RED Output Hold Time	t_{HZ4}	5	–	ns	
GREEN Output Hold Time	t_{HZ5}	5	–	ns	
BLUE Output Hold Time	t_{HZ6}	5	–	ns	
$\overline{CS}$ Cycle Time	t_{CSW22}	50 + 3 x t_{OCK}	–	ns	
$\overline{CS}$ Width Low	t_{CSWL22}	50	–	ns	
$\overline{CS}$ Width High	t_{CSWH22}	3 x t_{OCK}	–	ns	

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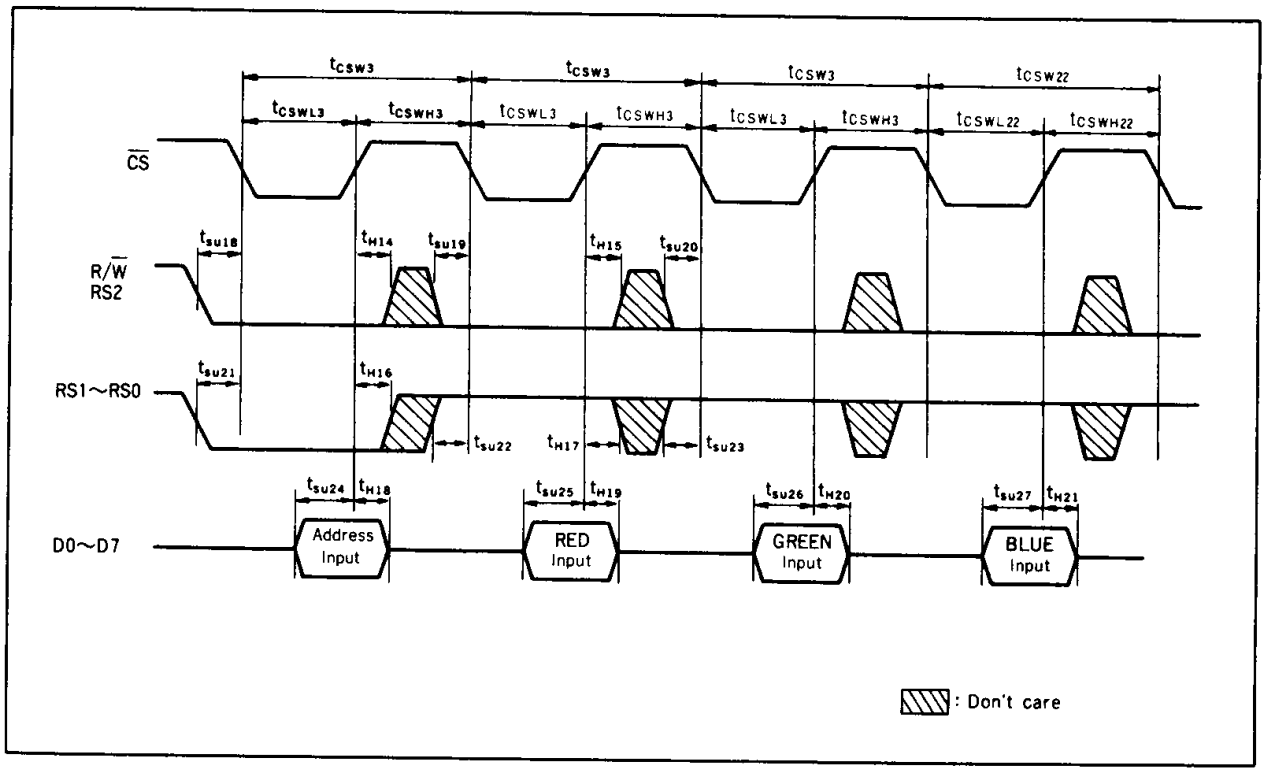
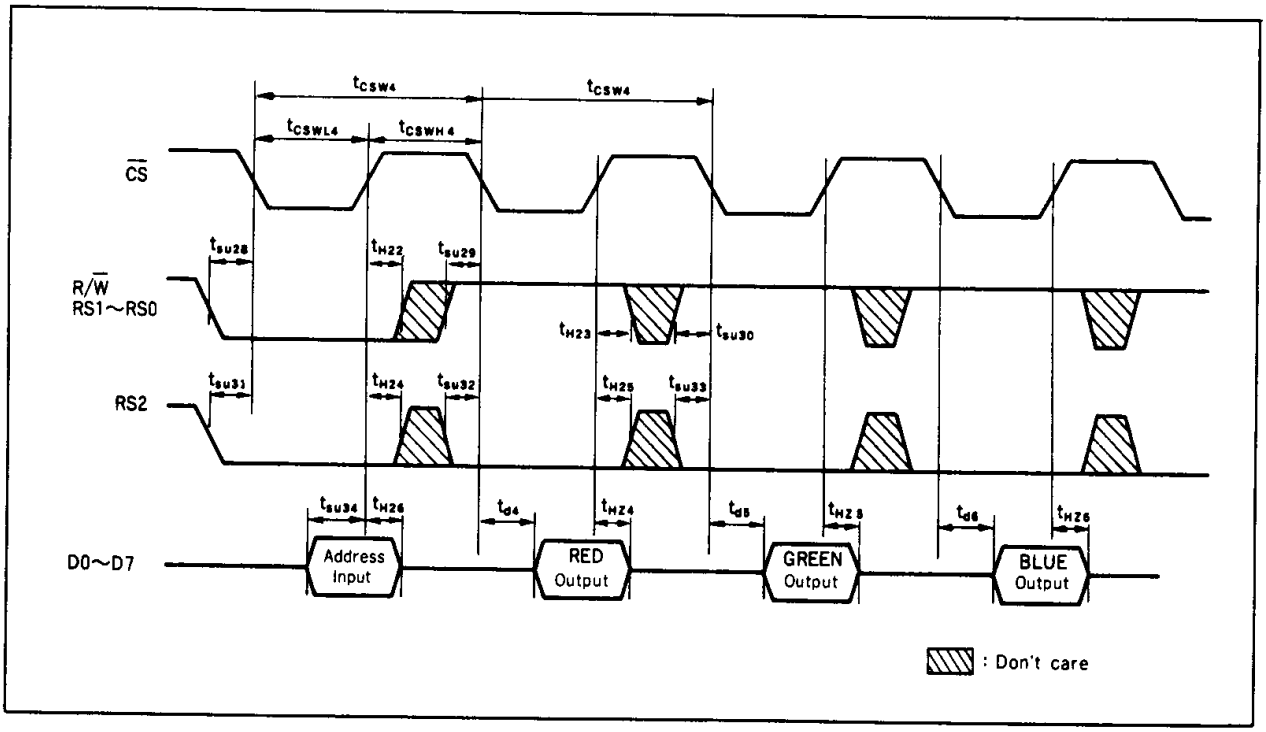
WRITE



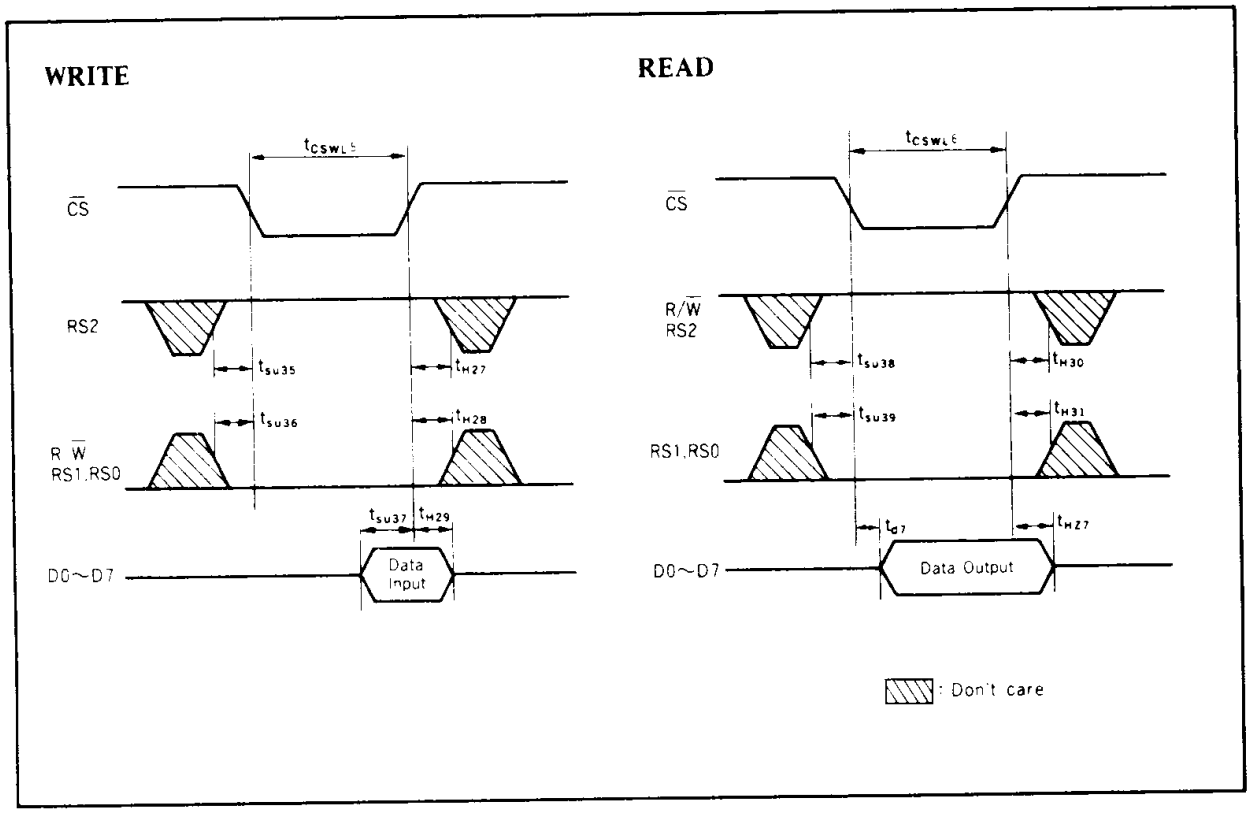
READ



READ MASK Register Access

(V_{CC} = 5V, Ta = 25°C)

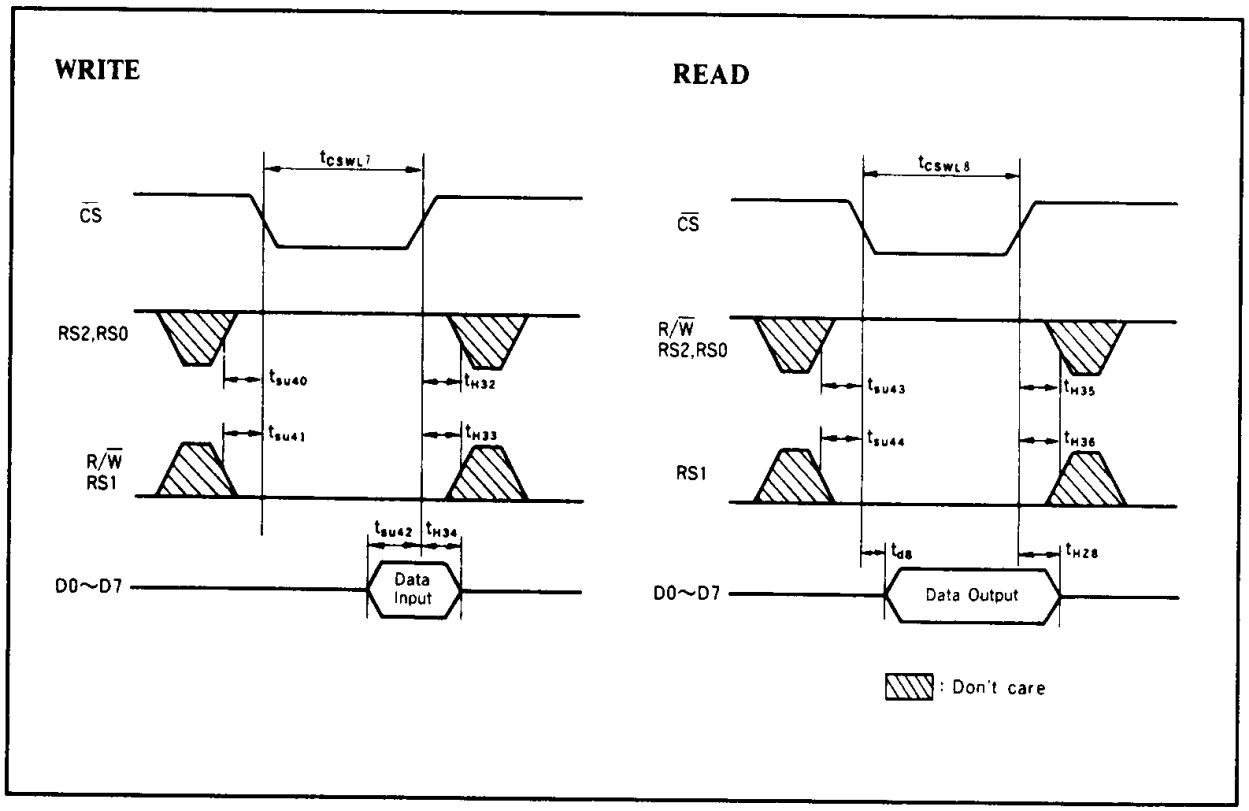
Item	Symbol	Min.	Max.	Unit	Test Condition
$\overline{CS}$ Width Low	t_{CSWL5}	50	–	ns	
RS2 Setup Time	t_{SU35}	6	–	ns	
R/$\overline{W}$, RS1, RS0 Setup Time	t_{SU36}	6	–	ns	
Input Data Setup Time	t_{SU37}	6	–	ns	
RS2 Hold Time	t_{H27}	6	–	ns	
R/$\overline{W}$, RS1, RS0 Hold Time	t_{H28}	6	–	ns	
Input Data Hold Time	t_{H29}	6	–	ns	
$\overline{CS}$ Width Low	t_{CSWL6}	50	–	ns	
R/$\overline{W}$, RS2 Setup Time	t_{SU38}	6	–	ns	
RS1, RS0 Setup Time	t_{SU39}	6	–	ns	
R/$\overline{W}$, RS2 Hold Time	t_{H30}	6	–	ns	
RS1, RS0 Hold Time	t_{H31}	6	–	ns	
READ MASK Register Output Delay	t_{d7}	–	75	ns	C_L = 50pF
READ MASK Register Output Hold Time	t_{HZ7}	5	–	ns	



BLINK MASK Register Access

(V_{CC} = 5V, Ta = 25°C)

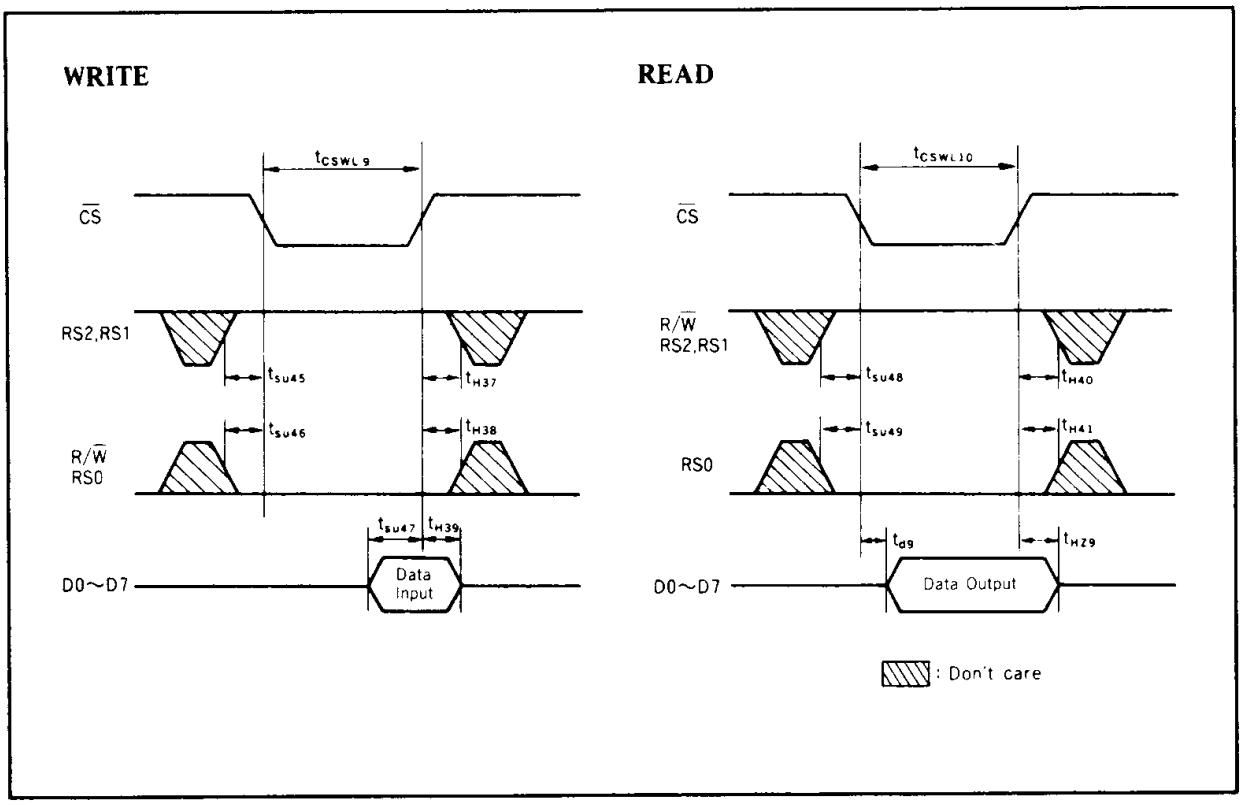
Item	Symbol	Min.	Max.	Unit	Test Condition
$\overline{CS}$ Width Low	t_{CSWL7}	50	–	ns	
RS2, RS0 Setup Time	t_{SU40}	6	–	ns	
R/$\overline{W}$, RS1 Setup Time	t_{SU41}	6	–	ns	
Input Data Setup Time	t_{SU42}	6	–	ns	
RS2, RS0 Hold Time	t_{H32}	6	–	ns	
R/$\overline{W}$, RS1 Hold Time	t_{H33}	6	–	ns	
Input Data Hold Time	t_{H34}	6	–	ns	
$\overline{CS}$ Width Low	t_{CSWL8}	50	–	ns	
R/$\overline{W}$, RS2, RS0 Setup Time	t_{SU43}	6	–	ns	
RS1 Setup Time	t_{SU44}	6	–	ns	
R/$\overline{W}$, RS2, RS0 Hold Time	t_{H35}	6	–	ns	
RS1 Hold Time	t_{H36}	6	–	ns	
BLINK MASK Register Output Delay	t_{d8}	–	75	ns	C_L = 50pF
BLINK MASK Register Output Hold Time	t_{HZ8}	5	–	ns	



OVERLAY CONTROL Register Access

(V_{CC} = 5V, Ta = 25°C)

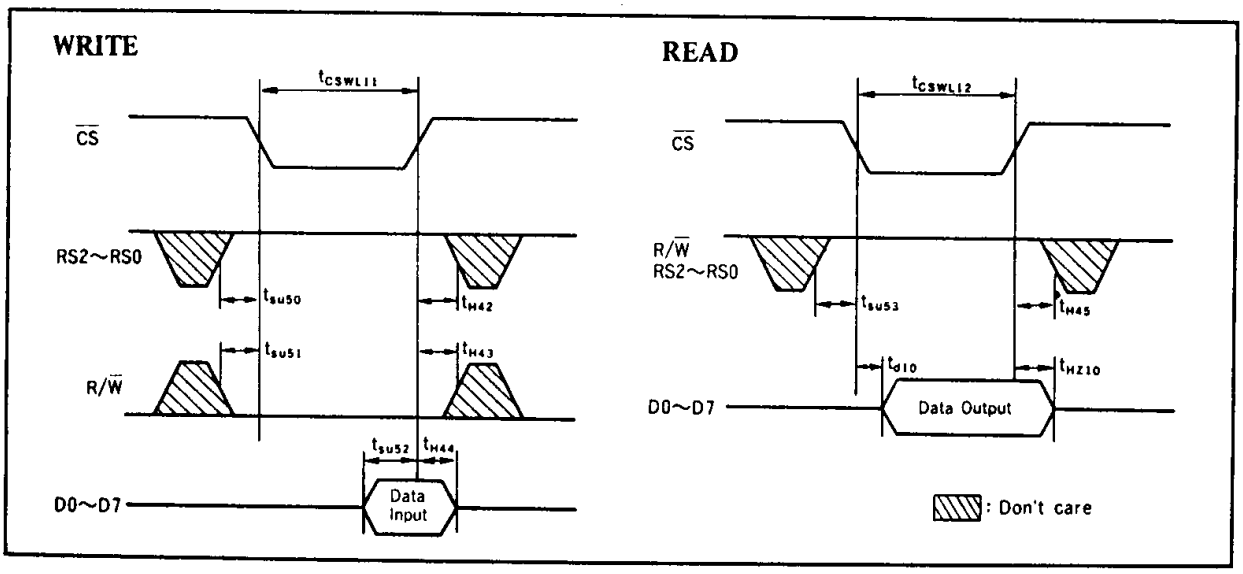
Item	Symbol	Min.	Max.	Unit	Test Condition
$\overline{CS}$ Width Low	t_{CSWL9}	50	–	ns	
RS2, RS1 Setup Time	t_{SU45}	6	–	ns	
R/$\overline{W}$, RS0 Setup Time	t_{SU46}	6	–	ns	
Input Data Setup Time	t_{SU47}	6	–	ns	
RS2, RS1 Hold Time	t_{H37}	6	–	ns	
R/$\overline{W}$, RS0 Hold Time	t_{H38}	6	–	ns	
Input Data Hold Time	t_{H39}	6	–	ns	
$\overline{CS}$ Width Low	t_{CSWL10}	50	–	ns	
R/$\overline{W}$, RS2, RS1 Setup Time	t_{SU48}	6	–	ns	
RS0 Setup Time	t_{SU49}	6	–	ns	
R/$\overline{W}$, RS2, RS1 Hold Time	t_{H40}	6	–	ns	
RS0 Hold Time	t_{H41}	6	–	ns	
OVERLAY CONTROL Register Output Delay	t_{d9}	–	75	ns	C_L = 50pF
OVERLAY CONTROL Register Output Hold Time	t_{HZ9}	5	–	ns	



BLINK TIMING Register Access

(V_{CC} = 5V, Ta = 25°C)

Item	Symbol	Min.	Max.	Unit	Test Condition
$\overline{CS}$ Width Low	t_{CSWL11}	50	–	ns	
RS2, RS1, RS0 Setup Time	t_{SU50}	6	–	ns	
R/$\overline{W}$ Setup Time	t_{SU51}	6	–	ns	
Input Data Setup Time	t_{SU52}	6	–	ns	
RS2, RS1, RS0 Hold Time	t_{H42}	6	–	ns	
R/$\overline{W}$ Hold Time	t_{H43}	6	–	ns	
Input Data Hold Time	t_{H44}	6	–	ns	
$\overline{CS}$ Width Low	t_{CSWL12}	50	–	ns	
R/$\overline{W}$, RS2, RS1, RS0 Setup Time	t_{SU53}	6	–	ns	
R/$\overline{W}$, RS2, RS1, RS0 Hold Time	t_{H45}	6	–	ns	
BLINK TIMING Register Output Delay	t_{d10}	–	75	ns	C_L = 50pF
BLINK TIMING Register Output Hold Time	t_{HZ10}	5	–	ns	



CRT Monitor Interface

R, G and B output (analog) waveform will be like Fig. 2 (a), (b) under the load condition in Fig. 1.

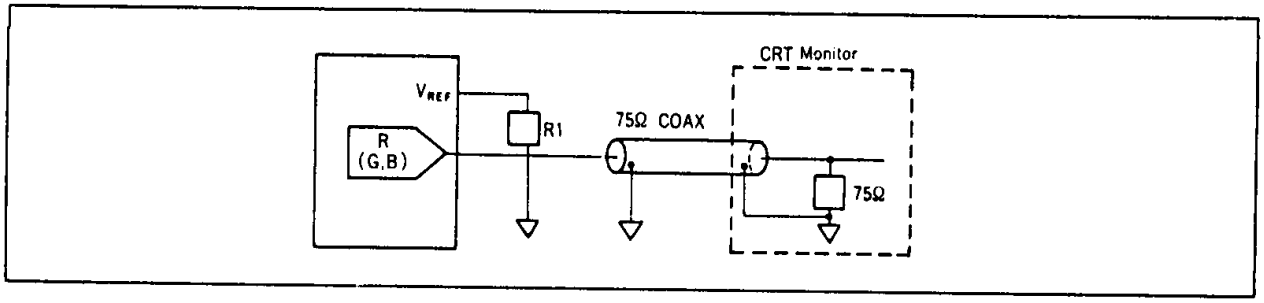


Fig. 1. CRT Monitor Interface

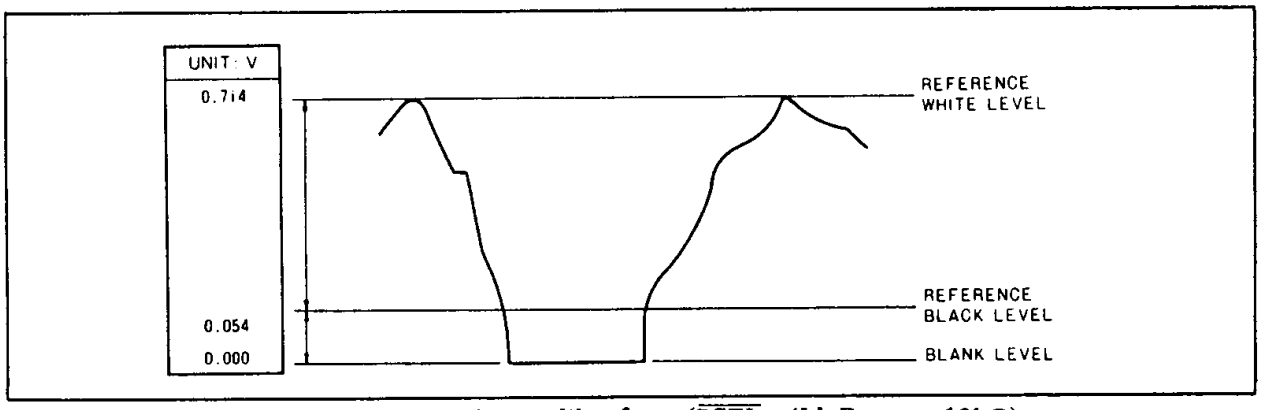


Fig. 2. (a) Video Output Waveform ($\overline{BSEL}$ = 'L', R_{REF} = 13kΩ)

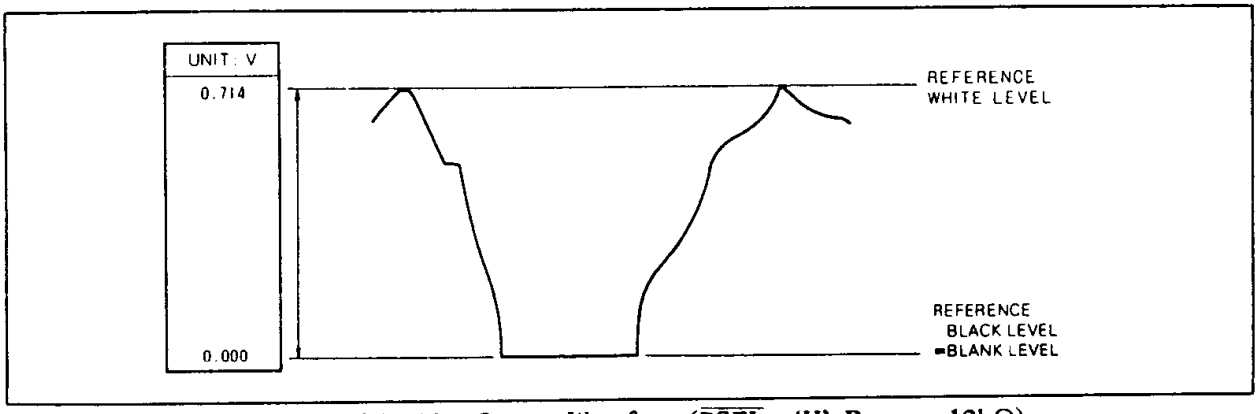


Fig. 2. (b) Video Output Waveform ($\overline{BSEL}$ = 'H', R_{REF} = 12kΩ)

Typical Connection Diagram