

Package Style: Module, 7.00mmx6.00mmx1.00mm

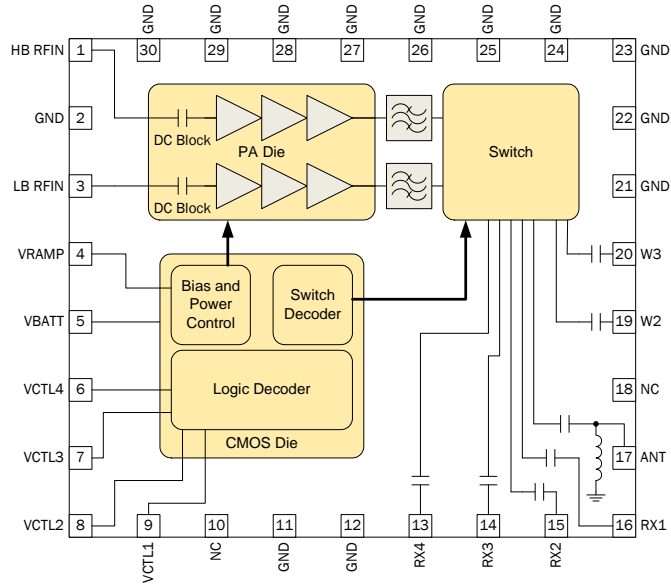


**Features**

- Two High Linearity, Low Loss, UMTS Switch Ports
- UMTS Port to Port Isolation >20dB
- Improved Power Flatness Into VSWR Through Integrated 2.5A Current Limiter
- Low Harmonics Into VSWR
- GSM850 Max PAE 43%
- EGSM900 Max PAE 39%
- DCS1800 Max PAE 40%
- PCS1900 Max PAE 42%
- Four Symmetrical RX Ports
- Two Symmetrical UMTS Ports
- 8kV ESD Protection at Antenna Port
- All RF Ports Have Internal DC Blocking
- Drive Level 0dBm to 6dBm
- Proven PowerStar® Architecture

**Applications**

- Battery Powered 3G Handsets
- GSM850/EGSM900/DCS/PCS Products
- Multislot Class 12 Products (4TX, 4RX Timeslots)



Functional Block Diagram

**Product Description**

The RF3230 is a high-power, high-efficiency transmit module with integrated power control, an integrated pHEMT front end switch, and harmonic filtering functionality. This device is self-contained with 50Ω input and output terminals and no external matching circuits required. The device is designed for use as the last portion of the transmit chain in GMSK architectures in GSM850, EGSM900, DCS, and PCS handheld digital cellular equipment where UMTS pass-through ports are needed. The RF3230 high performance transmit module offers mobile handset designers a compact, easy-to-use, front-end solution for multi-mode, multi-band systems.

**Ordering Information**

RF3230	Quad-Band GMSK TXM, 2 UMTS Switch Ports
RF3230 SB	5-Piece Module Sample Pack
RF3230PCBA-410	Fully Assembled Evaluation Board

**Optimum Technology Matching® Applied**

- |  |                                      |  |                                   |
|--|--------------------------------------|--|-----------------------------------|
| <input checked="" type="checkbox"/> GaAs HBT | <input type="checkbox"/> SiGe BiCMOS | <input checked="" type="checkbox"/> GaAs pHEMT | <input type="checkbox"/> GaN HEMT |
| <input type="checkbox"/> GaAs MESFET         | <input type="checkbox"/> Si BiCMOS   | <input checked="" type="checkbox"/> Si CMOS    | <input type="checkbox"/> RF MEMS  |
| <input type="checkbox"/> InGaP HBT           | <input type="checkbox"/> SiGe HBT    | <input type="checkbox"/> Si BJT                | <input type="checkbox"/> LDMS     |

RF MICRO DEVICES®, RFMD®, Optimum Technology Matching®, Enabling Wireless Connectivity™, PowerStar®, POLARIS™ TOTAL RADIO™ and UltimateBlue™ are trademarks of RFMD, LLC. BLUETOOTH is a trademark owned by Bluetooth SIG, Inc., U.S.A. and licensed for use by RFMD. All other trade names, trademarks and registered trademarks are the property of their respective owners. ©2006, RF Micro Devices, Inc.

## Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage in Standby Mode	-0.5 to +6.0	V
Supply Voltage in Idle Mode	-0.5 to +6.0	V
Supply Voltage in Operating Mode (Operation time less than 100ms; $V_{RAMP} \leq 1.6V$ )	-0.5 to +6.0	V
DC Continuous current during burst	2.8	A
VCTL 1 - 4	-0.5 to +3.0	V
Power Control Voltage ( $V_{RAMP}$ )	-0.5 to +1.8	V
Input RF Power	+12	dBm
Duty Cycle with power reduction per 3GPP Power Profile 2	50	%
Output Load VSWR (See Ruggedness Specification)	20:1	
Operating Temperature	-30 to +85	°C
Storage Temperature	-55 to +150	°C
ESD Antenna Port (IEC 61000-4-2)	8	kV



Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RoHS status based on EU Directive 2002/95/EC (at time of this document revision).

The information in this publication is believed to be accurate and reliable. However, no responsibility is assumed by RF Micro Devices, Inc. ("RFMD") for its use, nor for any infringement of patents, or other rights of third parties, resulting from its use. No license is granted by implication or otherwise under any patent or patent rights of RFMD. RFMD reserves the right to change component circuitry, recommended application circuitry and specifications at any time without prior notice.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
<b>General Operating Conditions</b>					
Operating Temperature	-20	25	85	°C	Specified operating range.
$V_{BATT}$ Supply Voltage	3.2	3.6	4.6	V	Specified operating range.
	3		4.8	V	Functional operating range.
$V_{BATT}$ Supply Current					
Off State		0.1	10	uA	Mode=Standby
Antenna Switch Active (RX path)		60	150	uA	Mode=RXn (n=1, 2, 3, 4)
Antenna Switch Active (W path)		60	150	uA	Mode=Wn (n=2, 3)
Transmit Mode with Current Limit		2300	2600	mA	Mode=TX LB, TX HB
$V_{RAMP}$ Input					
GMSK Operation	0.2		1.6	V	$V_{RAMP}$ voltage controls saturated power
Impedance	50k $\Omega$		10pF		
VCTL 1-4					Logic control voltages
Logic Low Voltage	0	0	0.5	V	
Logic High Voltage	1.3	2.0	3.0	V	
Logic High Current		0.1	10	uA	
RF Input and Output Impedance		50		$\Omega$	Pins 1, 3, 13, 14, 15, 16, 17, 19, 20

**Module Control Logic**

Mode	VCTL1	VCTL2	VCTL3	VCTL4
Standby	0	0	0	0
TX LB	0	0	0	1
TX HB	0	0	1	1
RX1	1	X	0	0
RX2	1	X	0	1
RX3	1	X	1	1
RX4	1	X	1	0
W2	0	1	0	0
W3	0	1	1	0

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
<b>GSM850 Band GMSK Parameters</b>					<b>Unless otherwise stated:</b> All unused RF ports terminated in 50Ω, Input and Output=50Ω, Temperature=25°C, V <sub>BATT</sub> =3.6V, Mode=TX LB, GSM timeslots≤2, P <sub>IN</sub> =3dBm, V <sub>RAMP</sub> =Max
Operating Frequency	824		849	MHz	
Input Power (P <sub>IN</sub> )	0	3	6	dBm	
Input VSWR			3:1	Ratio	V <sub>RAMP</sub> =0.25V to 1.6V
Maximum Output Power (Nominal)	32.7	33.7		dBm	Temp=+25°C, V <sub>BATT</sub> =3.6V
Maximum Output Power (Extreme)	30.7			dBm	Temp=+85°C, V <sub>BATT</sub> =3.2V
PAE (Max Power)	36	43		%	
PAE (Rated Power)	32	36		%	P <sub>OUT</sub> =32.7 dBm
Peak Supply Current (Rated Power)		1400	1650	mA	P <sub>OUT</sub> =32.7 dBm
Peak Supply Current (Low Power)		120		mA	P <sub>OUT</sub> =5 dBm
Receive Band Noise Power					P <sub>OUT</sub> ≤32.7 dBm, Bandwidth=100kHz
869MHz to 894MHz (CEL)		-88	-82	dBm	20MHz noise
1930MHz to 1990MHz (PCS)		-117	-90	dBm	Out of band noise
Harmonics					V <sub>RAMP</sub> =V <sub>RAMPRP</sub>
2F <sub>0</sub>			-33	dBm	
3F <sub>0</sub>			-33	dBm	
4F <sub>0</sub> to 12.75GHz			-33	dBm	
Stability Under Load Mismatch (Spurious Emissions)			-36	dBm	Output Load VSWR=15:1, All phase angles, Temp=-20°C to +85°C, V <sub>BATT</sub> =3.2V to 4.6V, V <sub>RAMP</sub> ≤V <sub>RAMPRP</sub>
Ruggedness Under Load Mismatch	No damage or permanent degradation to device				Output Load VSWR=20:1, All phase angles, Temp=-20°C to +85°C, V <sub>BATT</sub> =3.2V to 4.6V, V <sub>RAMP</sub> ≤V <sub>RAMPRP</sub>
Forward Isolation 1		-48	-40	dBm	Mode=Standby, P <sub>IN</sub> =Max, V <sub>RAMP</sub> =Min
Forward Isolation 2		-28	-20	dBm	Mode=TX LB, P <sub>IN</sub> =Max, V <sub>RAMP</sub> =Min
Transmit Power Control Accuracy					Temp=-20°C to +85°C, V <sub>BATT</sub> =3.2V to 4.6V
Rated Power (PCL 5)	-2		2	dB	V <sub>RAMP</sub> =V <sub>RAMPRP</sub>
27dBm (PCL 8)	-3		3	dB	V <sub>RAMP</sub> set for 27 dBm at nominal conditions
13dBm (PCL 15)	-3		3	dB	V <sub>RAMP</sub> set for 13dBm at nominal conditions
5dBm (PCL 19)	-5		5	dB	V <sub>RAMP</sub> set for 5dBm at nominal conditions

Notes:

V<sub>RAMPRP</sub> is defined as the V<sub>RAMP</sub> voltage required to achieve 32.7 dBm at V<sub>BATT</sub>=3.6V, Temperature=25°C, P<sub>IN</sub>=3dBm

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
<b>GSM900 Band GMSK Parameters</b>					<b>Unless otherwise stated:</b> All unused RF ports terminated in 50Ω, Input and Output=50Ω, Temperature = 25 °C, V <sub>BATT</sub> = 3.6V, Mode=TX LB, GSM timeslots≤2, P <sub>IN</sub> =3dBm, V <sub>RAMP</sub> =Max
Operating Frequency	880		915	MHz	
Input Power (P <sub>IN</sub> )	0	3	6	dBm	
Input VSWR			3:1	Ratio	V <sub>RAMP</sub> =0.25V to 1.6V
Maximum Output Power (Nominal)	32.7	33.2		dBm	Temp = +25 °C, V <sub>BATT</sub> = 3.6V
Maximum Output Power (Extreme)	30.7			dBm	Temp = +85 °C, V <sub>BATT</sub> = 3.2V
PAE (Max Power)	33	39		%	
PAE (Rated Power)	32	36		%	P <sub>OUT</sub> = 32.7 dBm
Peak Supply Current (Rated Power)		1400	1650	mA	P <sub>OUT</sub> = 32.7 dBm
Peak Supply Current (Low Power)		120		mA	P <sub>OUT</sub> = 5 dBm
Receive Band Noise Power					P <sub>OUT</sub> ≤ 32.7 dBm, Bandwidth = 100kHz
925 MHz to 935 MHz (EGSM)		-81	-78	dBm	10MHz noise
935 MHz to 960 MHz (EGSM)		-89	-83	dBm	20MHz noise
1805 MHz to 1880 MHz (DCS)		-117	-90	dBm	Out of band noise.
Harmonics					V <sub>RAMP</sub> = V <sub>RAMPRP</sub>
2F <sub>0</sub>			-33	dBm	
3F <sub>0</sub>			-33	dBm	
4F <sub>0</sub> to 12.75GHz			-33	dBm	
Stability Under Load Mismatch (Spurious Emissions)			-36	dBm	Output Load VSWR = 15:1, All phase angles, Temp = -20 °C to +85 °C, V <sub>BATT</sub> = 3.2V to 4.6V, V <sub>RAMP</sub> ≤ V <sub>RAMPRP</sub>
Ruggedness Under Load Mismatch	No damage or permanent degradation to device				Output Load VSWR = 20:1, All phase angles, Temp = -20 °C to +85 °C, V <sub>BATT</sub> = 3.2V to 4.6V, V <sub>RAMP</sub> ≤ V <sub>RAMPRP</sub>
Forward Isolation 1		-48	-40	dBm	Mode = Standby, P <sub>IN</sub> = Max, V <sub>RAMP</sub> = Min
Forward Isolation 2		-28	-20	dBm	Mode = TX LB, P <sub>IN</sub> = Max, V <sub>RAMP</sub> = Min
Transmit Power Control Accuracy					Temp = -20 °C to +85 °C, V <sub>BATT</sub> = 3.2V to 4.6V,
Rated Power (PCL 5)	-2		2	dB	V <sub>RAMP</sub> = V <sub>RAMPRP</sub>
27 dBm (PCL 8)	-3		3	dB	V <sub>RAMP</sub> set for 27 dBm at nominal conditions
13 dBm (PCL 15)	-3		3	dB	V <sub>RAMP</sub> set for 13 dBm at nominal conditions
5 dBm (PCL 19)	-5		5	dB	V <sub>RAMP</sub> set for 5 dBm at nominal conditions

**Notes:**

 V<sub>RAMPRP</sub> is defined as the V<sub>RAMP</sub> voltage required to achieve 32.7 dBm at V<sub>BATT</sub> = 3.6V, Temperature = 25 °C, P<sub>IN</sub> = 3dBm

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
<b>DCS1800 Band GMSK Parameters</b>					<b>Unless otherwise stated:</b> All unused RF ports terminated in 50Ω, Input and Output=50Ω, Temperature=25°C, V <sub>BATT</sub> =3.6V, Mode=TX HB, GSM timeslots≤2, P <sub>IN</sub> =3dBm, V <sub>RAMP</sub> =Max
Operating Frequency	1710		1785	MHz	
Input Power (P <sub>IN</sub> )	0	3	6	dBm	
Input VSWR			3:1	Ratio	V <sub>RAMP</sub> =0.25V to 1.6V
Maximum Output Power (Nominal)	30	31		dBm	Temp=+25°C, V <sub>BATT</sub> =3.6V
Maximum Output Power (Extreme)	28	29		dBm	Temp=+85°C, V <sub>BATT</sub> =3.2V
PAE (Max Power)	34	40		%	
PAE (Rated Power)	30	34		%	P <sub>OUT</sub> =30.0dBm
Peak Supply Current (Rated Power)		800	930	mA	P <sub>OUT</sub> =30.0dBm
Peak Supply Current (Low Power)		115		mA	P <sub>OUT</sub> =0dBm
Receive Band Noise Power					P <sub>OUT</sub> ≤33.0dBm, Bandwidth=100kHz
925MHz to 960MHz (EGSM)		-102	-90	dBm	Out of band noise
1805MHz to 1880MHz (DCS)		-90	-78	dBm	20MHz noise
Harmonics					V <sub>RAMP</sub> =V <sub>RAMPRP</sub>
2F <sub>0</sub>			-33	dBm	
3F <sub>0</sub>			-33	dBm	
6F <sub>0</sub> , 7F <sub>0</sub>		-32		dBm	
Other Harmonics, 4F <sub>0</sub> to 12.75GHz			-31	dBm	
Stability Under Load Mismatch (Spurious Emissions)			-36	dBm	Output Load VSWR=15:1, All phase angles, Temp=-20°C to +85°C, V <sub>BATT</sub> =3.2V to 4.6V, V <sub>RAMP</sub> ≤V <sub>RAMPRP</sub>
Ruggedness Under Load Mismatch	No damage or permanent degradation to device				Output Load VSWR=20:1, All phase angles, Temp=-20°C to +85°C, V <sub>BATT</sub> =3.2V to 4.6V, V <sub>RAMP</sub> ≤V <sub>RAMPRP</sub>
Forward Isolation 1		-58	-40	dBm	Mode=Standby, P <sub>IN</sub> =Max, V <sub>RAMP</sub> =Min
Forward Isolation 2		-25	-20	dBm	Mode=TX HB, P <sub>IN</sub> =Max, V <sub>RAMP</sub> =Min
Transmit Power Control Accuracy					Temp=-20°C to +85°C, V <sub>BATT</sub> =3.2V to 4.6V,
Rated Power (PCL 0)	-2		2	dB	V <sub>RAMP</sub> =V <sub>RAMPRP</sub>
14dBm (PCL 8)	-3		3	dB	V <sub>RAMP</sub> set for 14dBm at nominal conditions
4dBm (PCL 13)	-4		4	dB	V <sub>RAMP</sub> set for 4dBm at nominal conditions
0dBm (PCL 15)	-5		5	dB	V <sub>RAMP</sub> set for 0dBm at nominal conditions

Notes:

V<sub>RAMPRP</sub> is defined as the V<sub>RAMP</sub> voltage required to achieve 30.0dBm at V<sub>BATT</sub>=3.6V, Temperature=25°C, P<sub>IN</sub>=3dBm

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
<b>PCS1900 Band GMSK Parameters</b>					<b>Unless otherwise stated:</b> All unused RF ports terminated in 50Ω, Input and Output=50Ω, Temperature=25 °C, V <sub>BATT</sub> =3.6V, Mode=TX HB, GSM timeslots≤2, P <sub>IN</sub> =3dBm, V <sub>RAMP</sub> =Max
Operating Frequency	1850		1910	MHz	
Input Power (P <sub>IN</sub> )	0	3	6	dBm	
Input VSWR			3:1	Ratio	V <sub>RAMP</sub> =0.25V to 1.6V
Maximum Output Power (Nominal)	30	31		dBm	Temp=+25 °C, V <sub>BATT</sub> =3.6V
Maximum Output Power (Extreme)	28	29		dBm	Temp=+85 °C, V <sub>BATT</sub> =3.2V
PAE (Max Power)	37	42		%	
PAE (Rated Power)	30	35		%	P <sub>OUT</sub> =30.0dBm
Peak Supply Current (Rated Power)		760	930	mA	P <sub>OUT</sub> =30.0dBm
Peak Supply Current (Low Power)		115		mA	P <sub>OUT</sub> =0dBm
Receive Band Noise Power					P <sub>OUT</sub> ≤30.0dBm, Bandwidth=100kHz
869MHz to 894MHz (EGSM)		-106	-90	dBm	Out of band noise
1930MHz to 1990MHz (PCS)		-86	-78	dBm	20MHz noise
Harmonics					V <sub>RAMP</sub> =V <sub>RAMP</sub> RP
2F <sub>0</sub>			-33	dBm	
3F <sub>0</sub>			-33	dBm	
6F <sub>0</sub>		-32		dBm	
Other Harmonics, 4F <sub>0</sub> to 12.75GHz			-31	dBm	
Stability Under Load Mismatch (Spurious Emissions)			-36	dBm	Output Load VSWR=15:1, All phase angles, Temp=-20 °C to +85 °C, V <sub>BATT</sub> =3.2V to 4.6V, V <sub>RAMP</sub> ≤V <sub>RAMP</sub> RP
Ruggedness Under Load Mismatch	No damage or permanent degradation to device				Output Load VSWR=20:1, All phase angles, Temp=-20 °C to +85 °C, V <sub>BATT</sub> =3.2V to 4.6V, V <sub>RAMP</sub> ≤V <sub>RAMP</sub> RP
Forward Isolation 1		-58	-40	dBm	Mode=Standby, P <sub>IN</sub> =Max, V <sub>RAMP</sub> =Min
Forward Isolation 2		-25	-20	dBm	Mode=TX HB, P <sub>IN</sub> =Max, V <sub>RAMP</sub> =Min
Transmit Power Control Accuracy					Temp=-20 °C to +85 °C, V <sub>BATT</sub> =3.2V to 4.6V
Rated Power (PCL 0)	-2		2	dB	V <sub>RAMP</sub> =V <sub>RAMP</sub> RP
14dBm (PCL 8)	-3		3	dB	V <sub>RAMP</sub> set for 14dBm at nominal conditions
4dBm (PCL 13)	-4		4	dB	V <sub>RAMP</sub> set for 4dBm at nominal conditions
0dBm (PCL 15)	-5		5	dB	V <sub>RAMP</sub> set for 0dBm at nominal conditions

**Notes:**

 V<sub>RAMP</sub>RP is defined as the V<sub>RAMP</sub> voltage required to achieve 30.0dBm at V<sub>BATT</sub>=3.6V, Temperature=25 °C, P<sub>IN</sub>=3dBm

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
<b>Antenna Switch</b>					<b>Unless otherwise stated:</b> All unused RF ports terminated in 50Ω, Input and Output=50Ω, Temperature=25 °C, V <sub>BATT</sub> =3.6V, Mode=(See Module Control Logic), GSM timeslots≤2
Operating Frequency Range 1	824		960	MHz	
Operating Frequency Range 2	1710		1910	MHz	
Operating Frequency Range 3	1920		2170	MHz	
Input Power W2, W3			32	dBm	
Input Power RX1, RX2, RX3, RX4			13	dBm	
Input VSWR			1.6:1	Ratio	
Insertion Loss					Corrected for Evaluation Board loss
W2 - W3 ports (824MHz to 960MHz)		0.7	1.0	dB	Freq=960MHz
W2 - W3 ports (1710MHz to 1910MHz)		1.0	1.2	dB	Freq=1910MHz
W2 - W3 ports (1920MHz to 2170MHz)		1.1	1.3	dB	Freq=2170MHz
RX1 - RX4 ports (869MHz to 960MHz)		1.0	1.3	dB	Freq=960MHz
RX1 - RX4 ports (1805MHz to 1880MHz)		1.3	1.7	dB	Freq=1880MHz
RX1 - RX4 ports (1930MHz to 1990MHz)		1.4	1.7	dB	Freq=1990MHz
Isolation/Leakage					
Leakage LBTX to RX port			6	dBm	GMSK transmit at rated power
Leakage HBTX to RX port			10	dBm	GMSK transmit at rated power
Leakage LBTX to W port			12	dBm	GMSK transmit at rated power
Leakage HBTX to W port			12	dBm	GMSK transmit at rated power
Isolation LB W port to RX port	26	30		dB	Freq=824MHz to 915 MHz
Isolation HB W port to RX port	26	30		dB	Freq=1710MHz to 1980MHz
Isolation LB W port to W port	20	23		dB	Freq=824MHz to 915 MHz
Isolation HB W port to W port	20	21		dB	Freq=1710MHz to 1980MHz
Harmonics UMTS Ports					
Harmonics LB 2F <sub>0</sub>		-70	-60	dBm	P <sub>IN</sub> =28dBm CW, F <sub>0</sub> =824MHz to 915MHz
Harmonics LB 3F <sub>0</sub>		-60	-50	dBm	P <sub>IN</sub> =28dBm CW, F <sub>0</sub> =824MHz to 915MHz
Harmonics LB 4F <sub>0</sub> to 12.75GHz		-70	-60	dBm	P <sub>IN</sub> =28dBm CW, F <sub>0</sub> =824MHz to 915MHz
Harmonics HB 2F <sub>0</sub>		-60	-54	dBm	P <sub>IN</sub> =28dBm CW, F <sub>0</sub> =1710MHz to 1980MHz
Harmonics HB 3F <sub>0</sub>		-65	-58	dBm	P <sub>IN</sub> =28dBm CW, F <sub>0</sub> =1710MHz to 1980MHz
Harmonics HB 4F <sub>0</sub> to 12.75GHz		-65	-60	dBm	P <sub>IN</sub> =28dBm CW, F <sub>0</sub> =1710MHz to 1980MHz

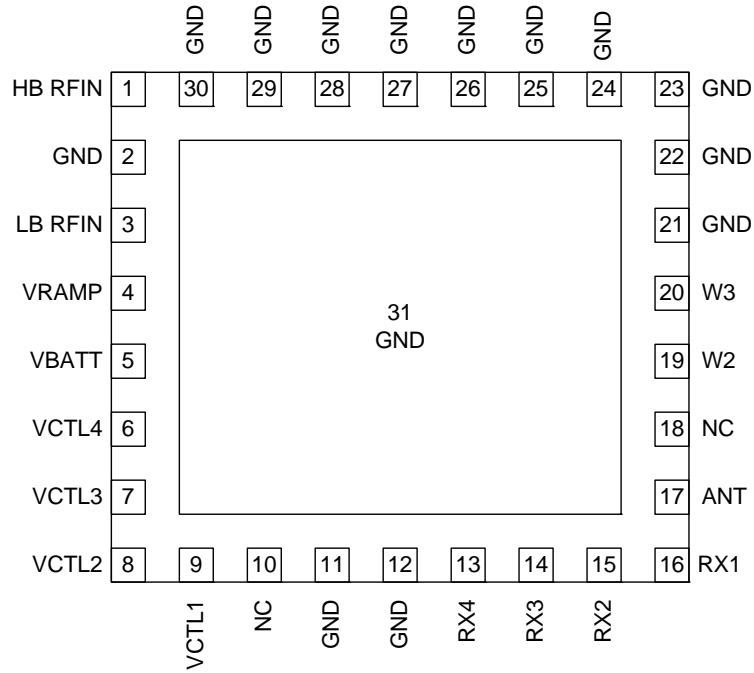


Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Antenna Switch, cont.					<b>Unless otherwise stated:</b> All unused RF ports terminated in 50Ω, Input and Output=50Ω, Temperature=25 °C, V <sub>BATT</sub> =3.6V, Mode=(See Module Control Logic), GSM timeslots ≤2
Intermodulation Products (Linearity) UMTS Ports					F <sub>0</sub> =20dBm signal on UMTS port, F <sub>INT</sub> =-15dBm signal on ANT port, frequency=(F <sub>IM</sub> -m*F <sub>0</sub> )/n, F <sub>IM</sub> =Spur signal within RX band, created by intermod product, measured at UMTS port
IMD2 (F <sub>0</sub> =824MHz to 915MHz)		-110	-101	dBm	F <sub>0</sub> =824MHz to 915MHz, F <sub>INT</sub> =(F <sub>IM</sub> -1*F <sub>0</sub> )/1, (F <sub>IM</sub> -(-1)*F <sub>0</sub> )/1
IMD3 (F <sub>0</sub> =824MHz to 915MHz)		-115	-101	dBm	F <sub>0</sub> =824MHz to 915MHz, F <sub>INT</sub> =(F <sub>IM</sub> -2*F <sub>0</sub> )/-1, (F <sub>IM</sub> -(-2)*F <sub>0</sub> )/1
IMD2 (F <sub>0</sub> =1710MHz to 1980MHz)		-115	-101	dBm	F <sub>0</sub> =1710MHz to 1980MHz, F <sub>INT</sub> =(F <sub>IM</sub> -1*F <sub>0</sub> )/1, (F <sub>IM</sub> -(-1)*F <sub>0</sub> )/1
IMD3 (F <sub>0</sub> =1710MHz to 1980MHz)		-108	-101	dBm	F <sub>0</sub> =1710MHz to 1980MHz, F <sub>INT</sub> =(F <sub>IM</sub> -2*F <sub>0</sub> )/-1, (F <sub>IM</sub> -(-2)*F <sub>0</sub> )/1

Pin	Function	Description
1	HB RF IN	RF input to the high band power amplifier. DC blocked inside the module.
2	GND	Ground.
3	LB RF IN	RF input to the low band power amplifier. DC blocked inside the module.
4	VRAMP	The voltage on this pin controls the output power by varying the internally regulated collector voltage on the amplifiers. This is a high bandwidth input so filter considerations for performance must be addressed externally.
5	VBATT	Main DC power supply for all circuitry in the module. Traces to this pin will have high current pulses during transmit operation. Proper decoupling and routing to handle this condition should be observed.
6	VCTL4	Digital Control Signal. Binary logic on VCTL1-4 sets module operating state.
7	VCTL3	Digital Control Signal. Binary logic on VCTL1-4 sets module operating state.
8	VCTL2	Digital Control Signal. Binary logic on VCTL1-4 sets module operating state.
9	VCTL1	Digital Control Signal. Binary logic on VCTL1-4 sets module operating state.
10	NC	No internal connection defined. Pin can be grounded on PCB.
11	GND	Ground.
12	GND	Ground.
13	RX4	Receive port 4. GSM receive port. DC blocked inside the module.
14	RX3	Receive port 3. GSM receive port. DC blocked inside the module.
15	RX2	Receive port 2. GSM receive port. DC blocked inside the module.
16	RX1	Receive port 1. GSM receive port. DC blocked inside the module.
17	ANT	Antenna Port. 50Ω matched input/output port for RF signals going to or from the antenna.
18	NC	No internal connection defined. Pin can be grounded on PCB.
19	W2	UMTS Transmit and Receive port 2. DC blocked inside the module.
20	W3	UMTS Transmit and Receive port 3. DC blocked inside the module.
21	GND	Ground.
22	GND	Ground.
23	GND	Ground.
24	GND	Ground.
25	GND	Ground.
26	GND	Ground.
27	GND	Ground.
28	GND	Ground.
29	GND	Ground.
30	GND	Ground.
31	GND	Ground. Main thermal heat sink for module.

**Pin Out**

Top Down View



## Theory of Operation

### Overview

The RF3230 is designed for use as the final portion of the transmit section in mobile phones covering the GSM850, EGSM900, DCS1800, and PCS1900MHz frequency bands in architectures where UMTS pass through ports are required. The RF3230 is a high power, saturated transmit module containing RFMD's patented PowerStar® Architecture. The module includes a multi function CMOS controller, GaAs HBT power amplifier, and pHEMT front end antenna switch. The integrated power control loop allows a single analog voltage to control output power for GSM PCLs and ramping. This analog voltage can be driven directly from the transceiver DAC to provide very predictable power control, enabling handset manufacturers to achieve simple and efficient phone calibration in production.

### Additional Features

#### Current Limiter

During normal use, a mobile phone antenna will be subjected to a variety of conditions that can affect its designed resonant frequency. This shift in frequency appears as a varying impedance to a power amplifier connected to the antenna. As the impedance presented to the power amplifier varies, so does the output power and current consumption. If left uncontrolled, power amplifier current can reach levels that can starve other circuitry, connected to the same supply, of the required voltage to operate. This can result in a reset or shutdown of the mobile phone. The RF3230 contains an active circuit that monitors the current and adjusts the internal power control loop to prevent peak current from going above 2.6A. While this current limiter can limit transmitted power under situations where the antenna is operating at very low efficiency, it is typically more acceptable for users to have a dropped call than a phone reset.

#### GMSK Operation

GMSK modulation is a constant RF envelope modulation scheme which encodes information in the phase of the signal and any amplitude variation is suppressed. Since no information is included in the amplitude of the signal, GMSK transmit is not sensitive to amplitude non-linearity of the power amplifier, allowing the amplifier to operate in deep class AB or class C saturation for optimum efficiency. The power envelope can be controlled by any one of a number of power control schemes.

During GMSK transmit RF3230 operates as a traditional PowerStar® module. The basic circuit diagram is shown in Figure 1. The PowerStar® control circuit receives an analog voltage ( $V_{RAMP}$ ) which sets the amplifier output power. The PowerStar® I architecture is essentially a closed loop method of power control that is invisible to the user. The  $V_{RAMP}$  voltage is used as a reference to a high speed linear voltage regulator which supplies the collector voltage to all stages of the amplifier. The base bias is fixed at a point that maintains deep class AB or class C transistor saturation. Because the amplifier remains in saturation at any power level, performance sensitivity to temperature, frequency, voltage and input drive level is essentially eliminated, ensuring robust performance within the ETSI power vs time mask.

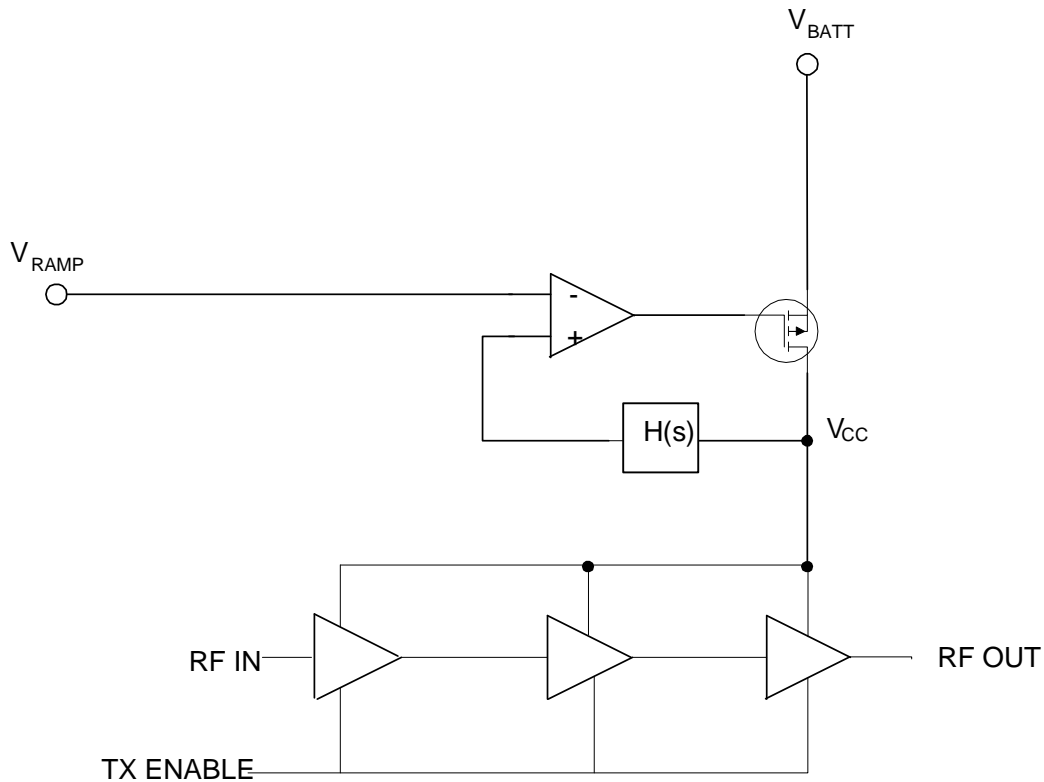


Figure 1: Basic PowerStar® Circuit Diagram

The PowerStar® power control relationship is described in Equation 1 where  $V_{CC}$  is the voltage from the linear regulator and the other variables are constants for a given amplifier design and load. The equation shows that load impedance affects output power, but to a lesser degree than  $V_{CC}$  supply variations. Since the architecture regulates  $V_{CC}$ , the dominant cause of power variation is eliminated. Another important result is that the equation provides a very linear relationship between  $V_{RAMP}$  and  $P_{OUT}$  expressed as  $V_{RMS}$ .

$$P_{dBm} = 10 \cdot \log \left[ \frac{(2 \cdot V_{CC} - V_{SAT})^2}{8 \cdot R_{LOAD} \cdot 10^{-3}} \right]$$

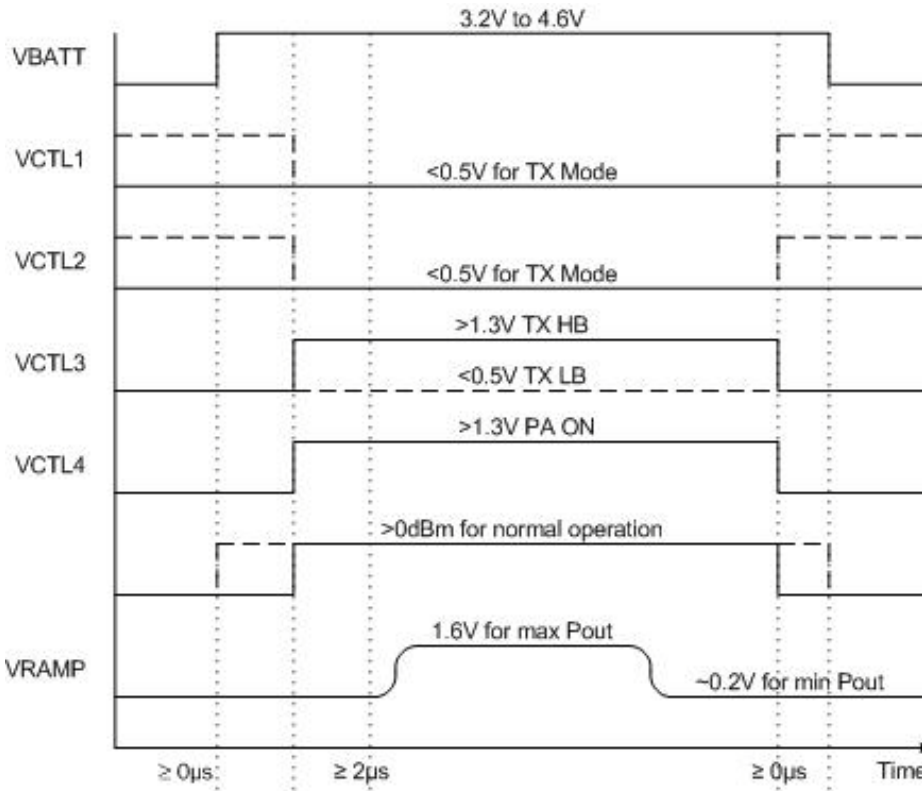
Equation 1: Output Power versus Voltage Relationship

The RF signal applied at  $RFIN$  of the amplifier must be a constant amplitude signal and should be high enough to saturate the amplifier. The input power ( $P_{IN}$ ) range is indicated in the specifications. Power levels below this range will result in reduced maximum output power and the potential for more variation of output power over extreme conditions. Higher input power is unnecessary and will require more current in the circuitry driving the power amplifier. A higher input power may also couple to the output and will increase the minimum output power level.

## Module Control Timing

In the Power-On Sequence, there are some important set-up times associated with the control signals of the TxM. Refer to the logic table for control signal functions. One of the critical relationships is the settling time between selecting TX mode and when  $V_{RAMP}$  can begin to increase. This time is often referred to as the “pedestal” and is required so that the internal power control loop and bias circuitry can settle after being turned on. The PowerStar® architecture usually requires approximately 1  $\mu$ s to 2  $\mu$ s for proper settling of the power control loop.

## GMSK Power On/Off Sequence



### Power On Sequence:

1. Apply VBATT
2. Apply minimum VRAMP (~-0.25V)
3. Apply RFIN
4. Apply VCTL1-4
5. Ramp VRAMP for desired output power

RFIN can be applied at any time. For good transient response it must be applied before power ramp begins.

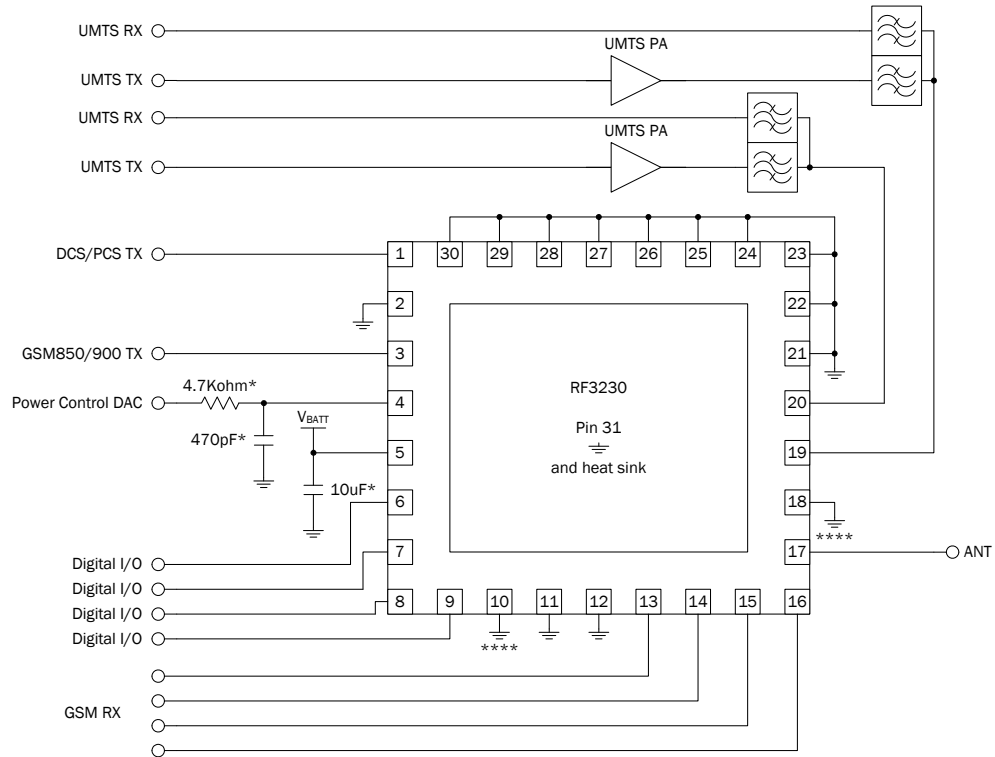
The Power Down Sequence is the reverse order of the Power On Sequence.

## Power Ramping

The  $V_{RAMP}$  waveform must be created such that the output power falls into the ETSI power versus time mask. The ability to ramp the RF output power to meet ETSI switching transient and time mask requirements partially depends upon the predictability of output power versus  $V_{RAMP}$  response of the power amplifier. The PowerStar® control loop is very capable of meeting switching transient requirements with the proper raised cosine waveform applied to the  $V_{RAMP}$  input. Ramp times between 10  $\mu$ s and 14  $\mu$ s can be optimized to provide excellent switching transients at high power levels. Shorter ramps will have a higher rate of change which will produce higher transients. Longer ramps may have difficulty meeting the time mask. Optimization needs to include all power levels as the time mask requirements change with  $P_{OUT}$  levels.

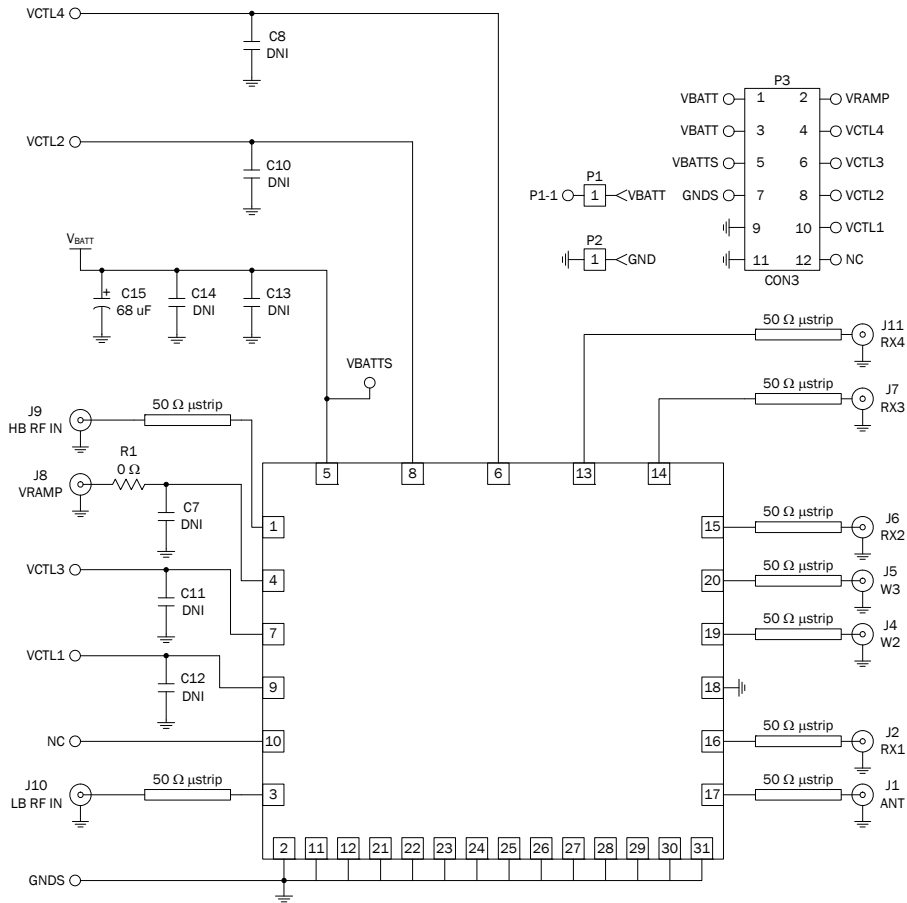
The RF3230 does not include a power control loop detection/correction circuit such as the  $V_{BATT}$  tracking circuit found in some PowerStar modules. If  $V_{RAMP}$  is set to a voltage where the FET pass-device in the linear regulator saturates, the response time of the regulated voltage ( $V_{CC}$ ) slows significantly. Upon ramp-down, the saturated linear regulator does not react immediately, and the output power does not follow the desired ramp-down curve. The result is a discontinuity in the output power ramp and degraded switching transients. To prevent this from happening,  $V_{RAMP}$  must be limited as the supply voltage is reduced. By maintaining  $V_{RAMP} \leq 0.345 \cdot V_{BATT} + 0.26$ , the linear regulator will avoid deep saturation and serious switching transient degradation will be avoided.

**Application Schematic**



- Notes:
- \* Suggested values only. Actual requirements will vary with application.
  - \*\*All RF paths should be designed as 50ohm microstrip or stripline.
  - \*\*\*Harmonic power from the high band amplifier near 11GHz is influenced by board layout and antenna impedance. Any matching components applied to the ANT port should be configured as a low pass filter to attenuate frequencies well above the normal GSM and UMTS transmit and receive signals.
  - \*\*\*\*NC pins on this module can be connected to ground.

## Evaluation Board Schematic

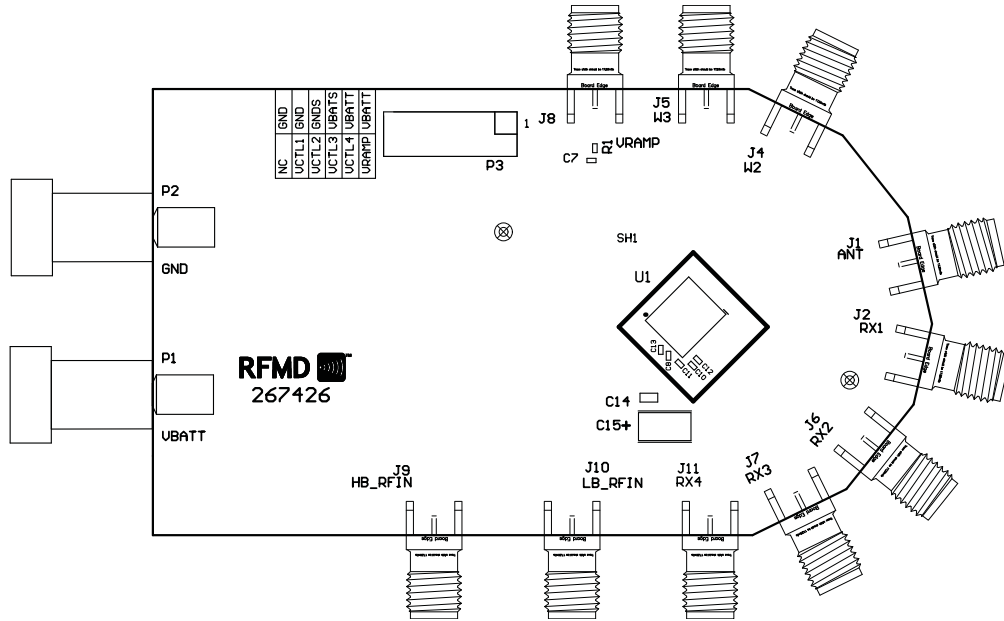




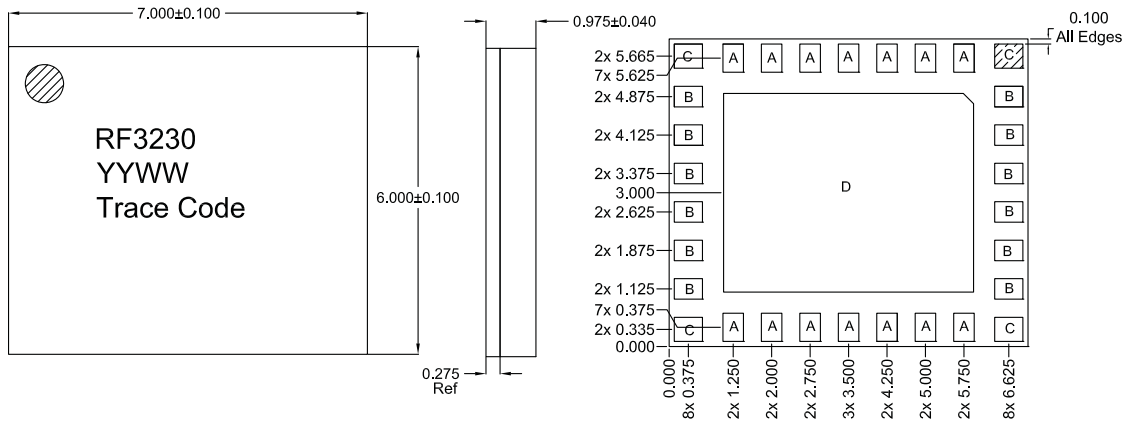
**Evaluation Board Layout**

Board Size 3.5" x 2.0"

Board Thickness 0.042", Board Material R04003 Top Layer, FR-4 Core and Bottom Layer



**Package Drawing**



A = 0.400 x 0.550 mm Typ  
 B = 0.550 x 0.400 mm Typ  
 C = 0.550 x 0.470 mm  
 D = 4.875 x 3.875 mm

**Notes:**

1. Shaded area represents Pin 1 location
2. Defining I/O Pad Center:  
 To define center of the I/O pad opening, draw a right triangle in one corner of the I/O pad  
 Then take the center of the hypotenuse to determine center of I/O pad



## PCB Design Requirements

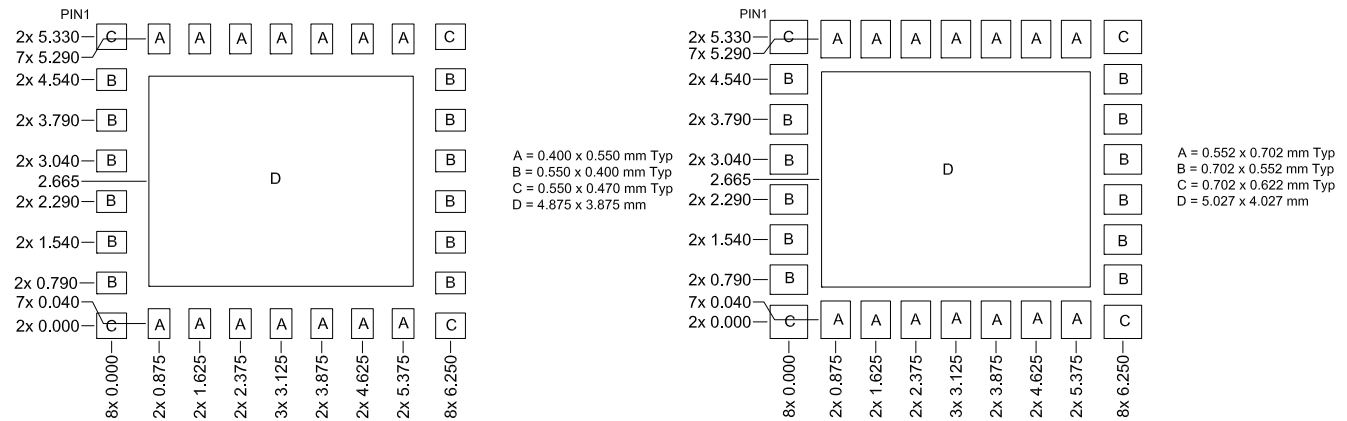
### PCB Surface Finish

The PCB surface finish used for RFMD's qualification process is electroless nickel, immersion gold. Typical thickness is 2 µinch to 5 µinch gold over 180 µinch nickel.

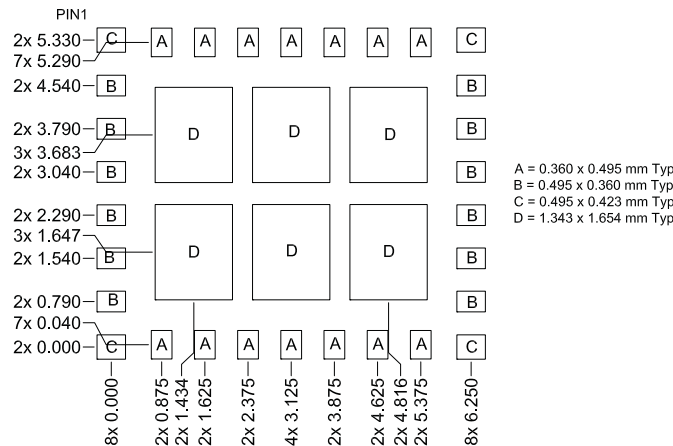
### PCB Land Pattern Recommendation

PCB land patterns for RFMD components are based on IPC-7351 standards and RFMD empirical data. The pad pattern shown has been developed and tested for optimized assembly at RFMD. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.

### PCB Metal Land and Solder Mask Pattern



### PCB Stencil Pattern



### Tape and Reel

Carrier tape basic dimensions are based on EIA 481. The pocket is designed to hold the part for shipping and loading onto SMT manufacturing equipment, while protecting the body and the solder terminals from damaging stresses. The individual pocket design can vary from vendor to vendor, but width and pitch will be consistent.

Carrier tape is wound or placed onto a shipping reel either 330mm (13 inches) in diameter or 178mm (7 inches) in diameter. The center hub design is large enough to ensure the radius formed by the carrier tape around it does not put unnecessary stress on the parts.

Prior to shipping, moisture sensitive parts (MSL level 2a-5a) are baked and placed into the pockets of the carrier tape. A cover tape is sealed over the top of the entire length of the carrier tape. The reel is sealed in a moisture barrier ESD bag with the appropriate units of desiccant and a humidity indicator card, which is placed in a cardboard shipping box. It is important to note that unused moisture sensitive parts need to be resealed in the moisture barrier bag. If the reels exceed the exposure limit and need to be rebaked, most carrier tape and shipping reels are not rated as bakeable at 125 °C. If baking is required, devices may be baked according to section 4, table 4-1, of Joint Industry Standard IPC/JEDEC J-STD-033.

The table below provides information for carrier tape and reels used for shipping the devices described in this document.

#### Tape and Reel

RFMD Part Number	Reel Diameter Inch (mm)	Hub Diameter Inch (mm)	Width (mm)	Pocket Pitch (mm)	Feed	Units per Reel
<b>RF3230TR13</b>	13 (330)	4 (102)	16	8	Single	2500
<b>RF3230TR7</b>	7 (178)	2.4 (61)	16	8	Single	750

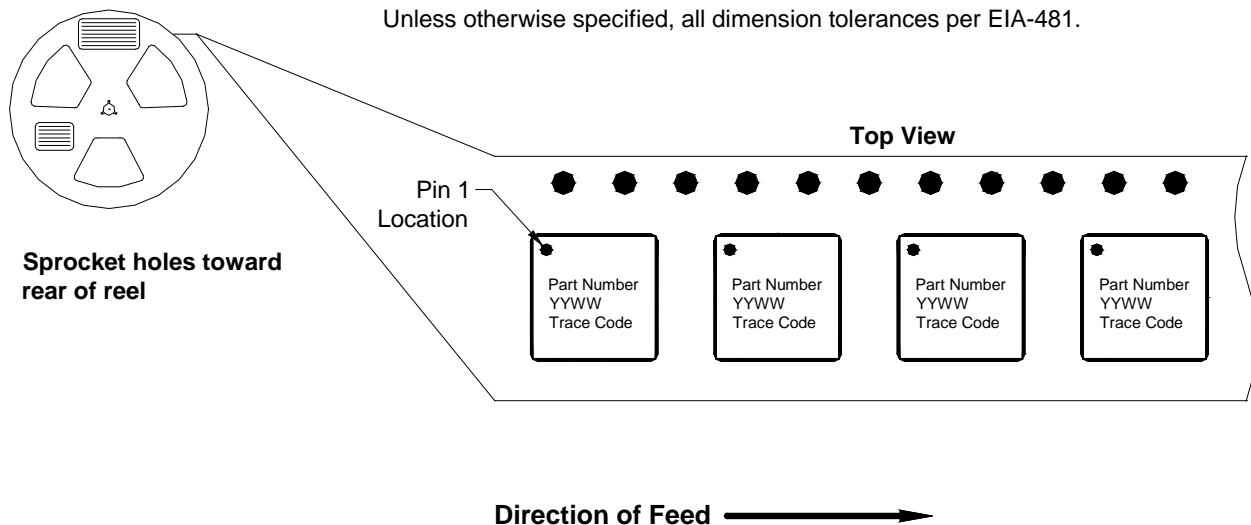


Figure 2. 7 mmx6mm (Carrier Tape Drawing with Part Orientation)

**RF3230**

