SC1486A
Dual Synchronous Buck DDR and DDR2 Power Supply Controller

POWER MANAGEMENT

Description

The SC1486A is a dual output constant on-time synchronous buck PWM controller optimized for cost effective mobile DDR and DDR2 applications. Features include high efficiency, a fast dynamic response with no minimum on time, a REFIN input and a buffered REFOUT pin capable of sourcing 3mA. The excellent transient response means that SC1486A based solutions will require less output capacitance than competing fixed frequency converters.

The output voltage of the first controller can be adjusted from 0.5V to VCCA. In DDR applications, this voltage is set to 2.5 volts, and in DDR2, 1.8V. A resistor divider from this supply is used to drive the REFIN pin of the second controller. A unity gain buffer drives the REFOUT pin to the same potential as REFIN. The second controller regulates its output to REFOUT. Two frequency setting resistors set the on-time for each buck controller. The frequency can thus be tailored to minimize crosstalk. The integrated gate drivers feature adaptive shoot-through protection and soft switching, requiring no gate resistors for the top MOSFET. Additional features include cycle-by-cycle current limit, digital soft-start, over-voltage and under-voltage protection, and a Power Good output for each controller.

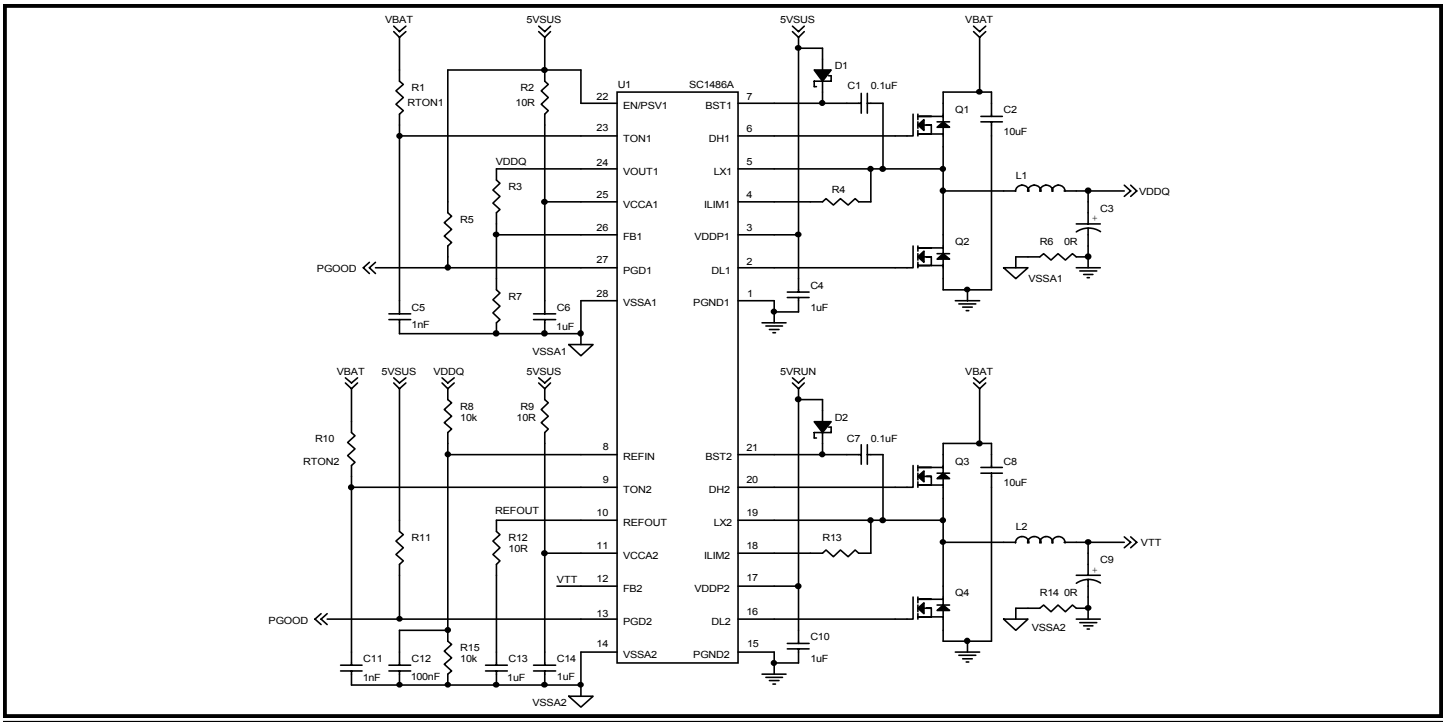
Features

- 1% DC accuracy
- Compatible with DDR & DDR2 memory power requirements
- Constant on-time for fast dynamic response
- VIN range = 1.8V – 25V
- DC current sense using low-side RDS(ON) sensing or sense resistor
- Integrated reference buffer for VTT
- Low power S3 state with high-Z VTT
- Resistor programmable on-time
- Cycle-by-cycle current limit
- Digital soft-start
- PSAVE option for VDDQ
- Over-voltage/under-voltage fault protection
- <20µA shutdown current
- Low quiescent power dissipation
- Two Power Good indicators
- Separate enable for each switcher
- Integrated gate drivers with soft switching - no gate resistors required
- Efficiency >90%
- 28 Lead TSSOP (lead free available)

Applications

- Notebook computers
- CPU I/O supplies
- Handheld terminals and PDAs

Typical Application Circuit



Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

Parameter	Symbol	Maximum	Units
TON1 to VSSA1, TON2 to VSSA2		-0.3 to +25.0	V
DH1, BST1 to PGND1 and DH2, BST2 to PGND2		-0.3 to +30.0	V
LX1 to PGND1 and LX2 to PGND2		-2.0 to +25.0	V
VSSA1 to PGND1, and VSSA2 to PGND2		-0.3 to +0.3	V
BST1 to LX1 and BST2 to LX2		-0.3 to +6.0	V
DL1, ILIM1, VDDP1 to PGND1 and DL2, ILIM2, VDDP2 to PGND2		-0.3 to +6.0	V
EN/PSV1, FB1, PGOOD1, VCCA1, VOUT1 to VSSA1		-0.3 to +6.0	V
FB2, PGOOD2, VCCA2, REFIN, REFOUT to VSSA2		-0.3 to +6.0	V
VCCA1 to EN/PSV1, FB1, PGOOD1, VOUT1		-0.3 to +6.0	V
VCCA2 to FB2, PGOOD2, REFIN, REFOUT		-0.3 to +6.0	V
Thermal Resistance Junction to Ambient(5)	θ_{JA}	37	°C/W
Operating Junction Temperature Range	T_J	-40 to +125	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C
Lead Temperature (Soldering) 10 Sec.	T_{LEAD}	300	°C

Electrical Characteristics

Test Conditions: V_{BAT} = 15V, EN/PSV1 = 5V, REFIN=1.25V, VCCA1 = VDDP1 = VCCA2 =VDDP2= 5.0V, V_{VDDQ} = 2.5, V_{VTT} = 1.25, R_{TON1} = 1M, R_{TON2} = 1M

Parameter	Conditions	25°C			-40°C to 125°C		Units
		Min	Typ	Max	Min	Max	
Input Supplies							
VCCA1, VCCA2			5.0		4.5	5.5	V
VDDP1, VDDP2			5.0		4.5	5.5	V
VDDP2 Undervoltage Threshold	VDDP2 falling		3.5				V
VDDP2 Undervoltage Hysteresis			250				mV
VDDP1, VDDP2 Operating Current	FB > regulation point, I_{LOAD} = 0A		70			150	µA
VCCA1, VCCA2 Operating Current	FB > regulation point, I_{LOAD} = 0A		700			1100	µA
VCCA2 Standby Current	VDDP2 < VDDP2 UV threshold, no load on REFOUT		125				µA
TON1, TON2 Operating Current	R_{TON} = 1M		15				µA
REFIN Bias Current	REFIN = 1.25					1	µA

Electrical Characteristics (Cont.)

Test Conditions: V_{BAT} = 15V, EN/PSV1 = 5V, REFIN=1.25V, VCCA1 = VDDP1 = VCCA2 =VDDP2= 5.0V, V_{VDDQ} = 2.5, V_{VTT} = 1.25, R_{TON1} = 1M, R_{TON2} = 1M

Parameter	Conditions	25°C			-40°C to 125°C		Units
		Min	Typ	Max	Min	Max	
Input Supplies (Cont.)							
Shutdown Current	EN/PSV1 = 0V		-5			-10	µA
	VCCA1, VCCA2		5			10	µA
	TON1, TON2, VDDP1		0			1	µA
Controller							
Error Comparator Threshold (FB1 Turn ON Threshold)	VCCA = 4.5V to 5.5V		0.500		-1%	+1%	V
VDDQ Output Voltage Range					0.5	VCCA	V
REFOUT Source Capability					3		mA
REFOUT DC Accuracy	no load, REFIN = 1.25	1.24		1.26	1.238	1.262	V
Error Comparator Threshold (FB2 Turn ON Threshold)	VCCA = 4.5V to 5.5V		REFOUT		REFOUT -10mV	REFOUT +10mV	V
On-Time, VBAT = 2.5V	R_{TON} = 1M Ω, V_{OUT} = 1.25V		1660		1411	1909	ns
	R_{TON} = 500kΩ, V_{OUT} = 1.25V		913		776	1050	ns
Minimum Off Time			400			550	ns
VOUT Input Resistance (VDDQ Controller)			500				kΩ
FB1 Input Bias Current					-1.0	+1.0	µA
FB2 Input Bias Current			2.5				µA
Over-Current Sensing							
ILIM Source Current	DL High		10		9	11	µA
Current Comparator Offset	PGND - ILIM				-10	+10	mV
PSAVE							
Zero-Crossing Threshold	PGND - LX EN/PSV1 = 5V		5				mV
Fault Protection							
Current Limit (Positive) (2) (PGND-LX)	R_{ILIM} = 5kΩ		50		35	65	mV
	R_{ILIM} = 10kΩ		100		80	120	mV
	R_{ILIM} = 20kΩ		200		170	230	mV
Current Limit (Negative) (PGND-LX)			-125		-160	-90	mV

Electrical Characteristics (Cont.)

Test Conditions: V_{BAT} = 15V, EN/PSV1 = 5V, REFIN=1.25V, VCCA1 = VDDP1 = VCCA2 =VDDP2= 5.0V, V_{VDDQ} = 2.5, V_{VTT} = 1.25, R_{TON1} = 1M, R_{TON2} = 1M

Parameter	Conditions	25°C			-40°C to 125°C		Units
		Min	Typ	Max	Min	Max	
Fault Protection (Cont.)							
VDDQ - Output Under-Voltage Fault	With respect to internal ref.		-30		-40	-25	%
VTT - Output Under-Voltage Fault	With respect to REFOUT		-20		-28	-15	%
VDDQ/VTT Output Over-Voltage Fault	VDDQ with respect to internal reference, VTT with respect to REFOUT		+10		+8	+12	%
Over-Voltage Fault Delay	FB forced above OV threshold		5				µs
PGD Low Output Voltage	Sink 1mA					0.4	V
PGD Leakage Current	FB in regulation, PGD = 5V					1	µA
PGD UV Threshold	With respect to internal reference for VDDQ and REFOUT for VTT		-10		-15	-8	%
PGD Fault Delay	FB forced outside PGD window		5				µs
VCCA1,VCCA2 Under Voltage	Falling (100mV hysteresis)		4.0		3.7	4.3	V
Over Temperature Lockout	10°C Hysteresis		165				°C
Inputs/Outputs							
Logic Input Low Voltage	EN/PSV1 low					1.2	V
Logic Input High Voltage	EN High, PSV low (Floating)		2.0		1.2	2.4	V
Logic Input High Voltage	EN/PSV1 high				2.4		V
REFIN EN Threshold	REFIN rising		0.50			0.60	V
REFIN EN Hysteresis			30				mV
EN/PSV1 Input Resistance	R pullup to VCCA1		1.5				MΩ
	R pulldown to VSSA1		1.0				
Soft Start							
Soft-Start Ramp Time	EN/PSV1 high to PGD1 high, REFIN high to PGD2 high		440				clks(3)
Under-Voltage Blank Time	EN/PSV1 high to UV high, REFIN high to UV high		440				clks(3)

Electrical Characteristics (Cont.)

Test Conditions: V_{BAT} = 15V, EN/PSV1 = 5V, REFIN=1.25V, VCCA1 = VDDP1 = VCCA2 =VDDP2= 5.0V, V_{VDDQ} = 2.5, V_{VTT} = 1.25, R_{TON1} = 1M, R_{TON2} = 1M

Parameter	Conditions	25°C			-40°C to 125°C		Units
		Min	Typ	Max	Min	Max	
Gate Drivers							
Shoot-Through Delay (4)	DH or DL rising		30				ns
DL Pull-Down Resistance	DL low		0.8			1.6	Ω
DL Sink Current	DL = 2.5V		3.1				A
DL Pull-Up Resistance	DL high		2			4	Ω
DL Source Current	DL = 2.5V		1.3				A
DH Pull-Down Resistance	DH low, BST - LX = 5V		2			4	Ω
DH Pull-Up Resistance	DH high, BST - LX = 5V		2			4	Ω
DH Sink/Source Current	DL = 2.5V		1.3				A

Notes:

(1) The output voltage will have a DC regulation level higher than the error-comparator threshold by 50% of the ripple voltage.

(2) Using a current sense resistor, this measurement relates to PGND minus the voltage of the source on the low-side MOSFET.

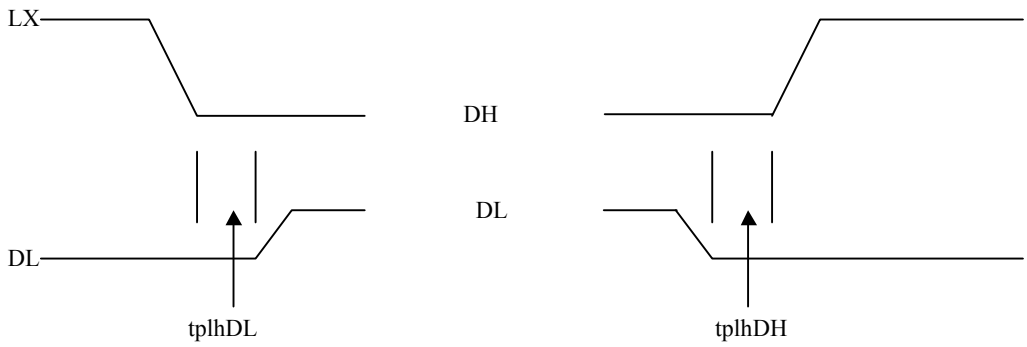
(3) clks = switching cycles.

(4) Guaranteed by design. See Shoot-Through Delay Timing Diagram below.

(5) Measured in accordance with JESD51-1, JESD51-2 and JESD51-7.

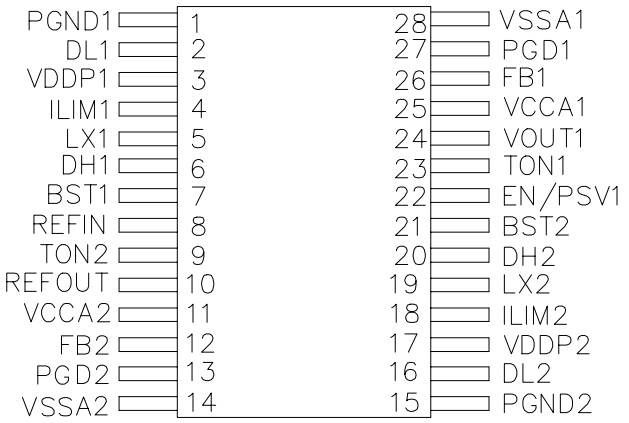
(6) This device is ESD sensitive. Use of standard ESD handling precautions is required.

Shoot-Through Delay Timing Diagram



Pin Configuration

Top View



(TSSOP-28)

Ordering Information

DEVICE	PACKAGE(1)
SC1486AITSTR	TSSOP-28
SC1486AITSTRT(2)	TSSOP-28
SC1486AEVB(3)	Evaluation Board

Notes:
(1) Only available in tape and reel packaging. A reel contains 2500 devices.
(2) Lead free option.
(3) Specify DDR or DDR2.

Pin Descriptions

Pin #	Pin Name	Pin Function
1	PGND1	Power ground.
2	DL1	Gate drive output for the low side MOSFET switch.
3	VDDP1	+5V supply voltage input for the gate drivers. Decouple this pin with a 1µF ceramic capacitor to PGND1.
4	ILIM1	Current limit input pin. Connect to drain of low-side MOSFET for RDS(ON) sensing or the source for resistor sensing through a threshold sensing resistor.
5	LX1	Phase node (junction of top and bottom MOSFETs and the output inductor) connection.
6	DH1	Gate drive output for the high side MOSFET switch.
7	BST1	Boost capacitor connection for the high side gate drive.
8	REFIN	Reference input. A 10kOhm + 10kOhm resistor divider from VDDQ to VSSA2 sets this voltage. A 0.1µF input filter capacitor is recommended.
9	TON2	This pin is used to sense VBAT through a pullup resistor, RTON2, and to set the top MOSFET on-time. Bypass this pin with a 1nF ceramic capacitor to VSSA2.
10	REFOUT	Buffered REFIN output. The second controller regulates to this voltage. Connect a series 10 Ohm and 1µF from this pin to VSSA2.
11	VCCA2	Supply voltage input for the analog supply. Use a 10 Ohm/1µF RC filter from 5VSUS to VSSA2.
12	FB2	Feedback input for output 2. Connect to the output at the output capacitor.
13	PGD2	Power Good open drain NMOS output. Goes high after a fixed clock cycle delay (440 cycles) following power up.
14	VSSA2	Ground reference for analog circuitry for output 2. Connect to bottom of output capacitor for output 2.

Pin Descriptions (Cont)

15	PGND2	Power ground.
16	DL2	Gate drive output for the low side MOSFET switch.
17	VDDP2	+5V supply voltage input for the gate drivers. Decouple this pin with a 1µF ceramic capacitor to PGND2.
18	ILIM2	Current limit input pin. Connect to drain of low-side MOSFET for RDS(ON) sensing or the source for resistor sensing through a threshold sensing resistor.
19	LX2	Phase node (junction of top and bottom MOSFETs and the output inductor) connection.
20	DH2	Gate drive output for the high side MOSFET switch.
21	BST2	Boost capacitor connection for the high side gate drive.
22	EN/PSV1	Enable/Power Save input pin. Pull down to VSSA1 to shut down this output. Pull up to enable this output and activate PSAVE mode. Float to enable this output and activate continuous conduction mode (CCM). If floated, bypass to VSSA1 with a 10nF ceramic capacitor.
23	TON1	This pin is used to sense VBAT through a pullup resistor, RTON1, and to set the top MOSFET on-time. Bypass this pin with a 1nF ceramic capacitor to VSSA1.
24	VOUT1	Output voltage sense input for output 1. Connect to the output at the output capacitor.
25	VCCA1	Supply voltage input for the analog supply. Use a 10Ohm/ 1µF RC filter from 5VSUS to VSSA1.
26	FB1	Feedback input. Connect to a resistor divider located at the IC from VOUT1 to VSSA1 to set the output voltage from 0.5V to VCCA1.
27	PGD1	Power Good open drain NMOS output. Goes high after a fixed clock cycle delay (440 cycles) following power up.
28	VSSA1	Ground reference for analog circuitry for output 1. Connect to bottom of output capacitor for output 1.

Block Diagram

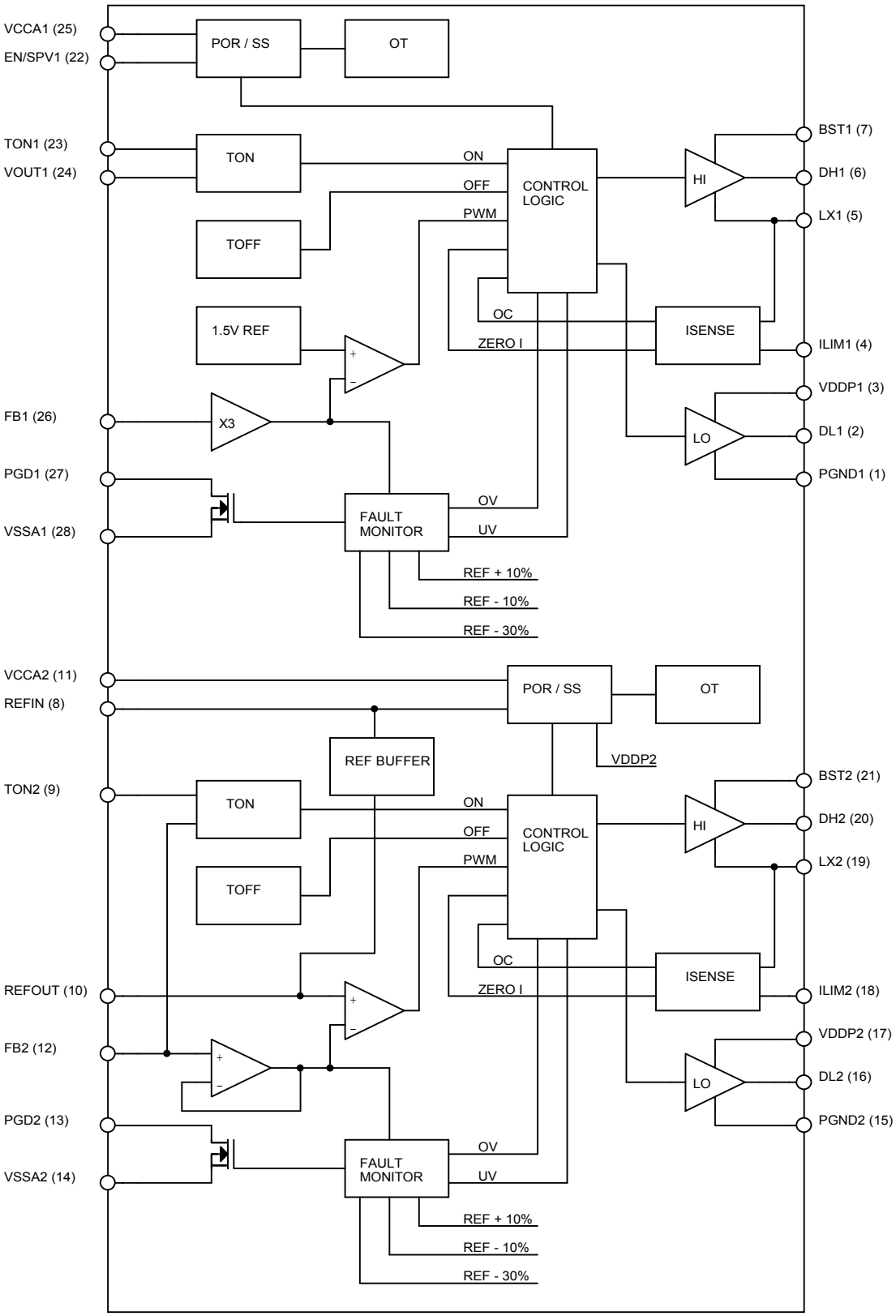


FIGURE 1 - SC1486A Block Diagram

Application Information

+5V Bias Supplies

The SC1486A requires an external +5V bias supply in addition to the battery. If stand-alone capability is required, the +5V supply can be generated with an external linear regulator such as the Semtech LP2951. To minimize channel to channel crosstalk, each controller has 4 supply pins, VDDP, PGND, VCCA and VSSA.

To avoid interference between outputs, each controller has its own ground reference, VSSA, which should be tied by a single trace to PGND at the negative terminal of that controller's output capacitor (see Layout Guidelines). All external components referenced to VSSA in the schematic should be connected to the appropriate VSSA trace. The supply decoupling capacitor for controller 1 should be tied between VCCA1 and VSSA1. Likewise, the supply decoupling capacitor for controller 2 should be tied between VCCA2 and VSSA2. A 10Ω resistor should be used to decouple each VCCA supply from the main VDDP supplies. PGND can then be a separate plane which is not used for routing traces. All PGND connections are connected directly to the ground plane with special attention given to avoiding indirect connections which may create ground loops. As mentioned above, VSSA1 and VSSA2 must be connected to the PGND plane at the negative terminal of their respective output capacitors only. The VDDP1 and VDDP2 inputs provide power to the upper and lower gate drivers. A decoupling capacitor for each supply is required. No series resistor between VDDP and 5V is required. See layout guidelines for more details.

Pseudo-fixed Frequency Constant On-Time PWM Controller

The PWM control architecture consists of a constant on-time, pseudo fixed frequency PWM controller (see Figure 1, SC1486A Block Diagram). The output ripple voltage developed across the output filter capacitor's ESR provides the PWM ramp signal eliminating the need for a current sense resistor. The high-side switch on-time is determined by a one-shot whose period is directly proportional to output voltage and inversely proportional to input voltage. A second one-shot sets the minimum off-time which is typically 400ns.

On-Time One-Shot (t_{ON})

The on-time one-shot comparator has two inputs. One input looks at the output voltage, while the other input samples the input voltage and converts it to a current. This input voltage-proportional current is used to charge an internal on-time capacitor. The on-time is the time required for the voltage on this capacitor to charge from zero volts to VOUT, thereby making the on-time of the high-side switch directly proportional to output voltage and inversely proportional to input voltage. This implementation results in a nearly constant switching frequency without the need for a clock generator.
For VOUT < 3.3V:

$$t_{ON} = 3.3x10^{-12} \bullet (R_{TON} + 37x10^{3}) \bullet \left(\frac{V_{OUT}}{V_{IN}} \right) + 50ns$$

For 3.3V ≤ VOUT ≤ 5V:

$$t_{ON} = 0.85 \bullet 3.3x10^{-12} \bullet (R_{TON} + 37x10^{3}) \bullet \left(\frac{V_{OUT}}{V_{IN}} \right) + 50ns$$

R_{TON} is a resistor connected from the input supply to the TON pin. Due to the high impedance of this resistor, the TON pin should always be bypassed to VSSA using a 1nF ceramic capacitor.

Enable & Psave

The EN/PSV pin enables the VDDQ (2.5V or 1.8V) supply. REFIN and VDDP2 enable the VTT (1.25V or 0.9V) supply. The VTT and VDDQ supplies may be enabled independently, however it is usual to use a resistor divider from VDDQ to generate REFIN, so if VDDQ is not present, VTT will not be present.
When EN/PSV1 is tied to VCCA the VDDQ controller is enabled and power save will also be enabled. When the EN/PSV pin is tri-stated, an internal pull-up will activate the VDDQ controller and power save will be disabled. If PSAVE is enabled, the SC1486A PSAVE comparator will look for the inductor current to cross zero on eight consecutive switching cycles by comparing the phase node (LX) to PGND. Once observed, the controller will enter power save and turn off the low side MOSFET when the current crosses zero. To improve light-load efficiency and add hysteresis, the on-time is increased by 50% in power save. The efficiency improvement at light-loads more than offsets the disadvantage of slightly higher output ripple. If the inductor current does not cross zero on any switching cycle, the controller will immediately exit power save. Since the controller counts zero crossings, the converter can sink current as long as the current does not cross zero on eight consecutive cycles. This allows the output voltage to recover quickly in response to negative load steps even when psave is enabled.

Application Information (Cont.)

OUT1 Output Voltage Selection

The output voltage is set by the feedback resistors R10 & R13 of Figure 2 below. The internal reference is 1.5V, so the voltage at the feedback pin is multiplied by three to match the 1.5V reference. Therefore the output can be set to a minimum of 0.5V. The equation for setting the output voltage is:

$$VOUT = \left(1 + \frac{R10}{R13}\right) \bullet 0.5$$

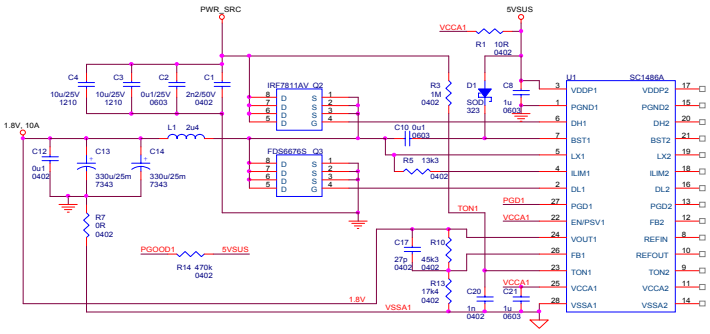
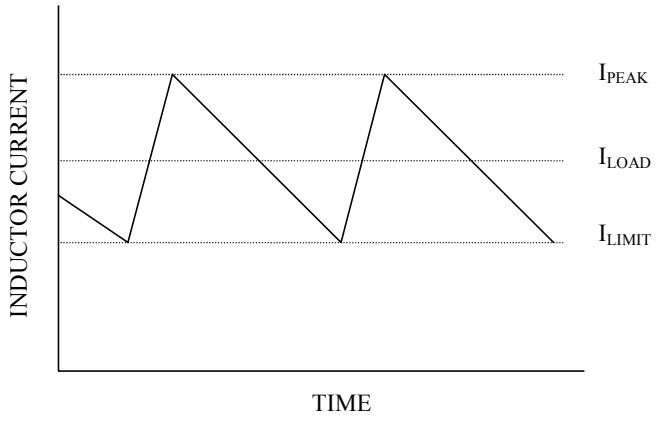


Figure 2: Setting VDDQ Output Voltage

Current Limit Circuit

Current limiting of the SC1486A can be accomplished in two ways. The on-state resistance of the low-side MOSFETs can be used as the current sensing element or sense resistors in series with the low-side sources can be used if greater accuracy is desired. $R_{DS(ON)}$ sensing is more efficient and less expensive. In both cases, the R_{ILIM} resistors between the ILIM pin and LX pin set the over current threshold. This resistor R_{ILIM} is connected to a 10µA current source within the SC1486A which is turned on when the low side MOSFET turns on. When the voltage drop across the sense resistor or low side MOSFET equals the voltage across the RILIM resisor, positive current limit will activate. The high side MOSFET will not be turned on until the voltage drop across the sense element (resistor or MOSFET) falls below the voltage across the R_{ILIM} resistor. In an extreme over-current situation, the top MOSFET will never turn back on and eventually the part will latch off due to output undervoltage (see Output Undervoltage Protection).

The current sensing circuit actually regulates the inductor valley current (see Figure 3). This means that if the current limit is set to 10A, the peak current through the inductor would be 10A plus the peak ripple current, and the average current through the inductor would be 10A plus 1/2 the peak-to-peak ripple current. The equations for setting the valley current and calculating the average current through the inductor are shown below:



Valley Current-Limit Threshold Point

Figure 3: Valley Current Limiting

The equation for the current limit threshold is as follows:

$$I_{LIMIT} = 10e^{-6} \bullet \frac{R_{ILIM}}{R_{SENSE}} A$$

Where (referring to Figure 2) R_{ILIM} is R5 and R_{SENSE} is the $R_{DS(ON)}$ of Q3.

For resistor sensing, a sense resistor is placed between the source of Q3 and PGND. The current through the source sense resistor develops a voltage that opposes the voltage developed across R_{ILIM}. When the voltage developed across the R_{SENSE} resistor reaches the voltage drop across R_{ILIM}, a positive over-current exists and the high side MOSFET will not be allowed to turn on. When using an external sense resistor R_{SENSE} is the resistance of the sense resistor.

The current limit circuitry also protects against negative over-current (i.e. when the current is flowing from the load to PGND through the inductor and bottom MOSFET). In this case, when the bottom MOSFET is turned on, the phase node, LX, will be higher than PGND initially. The SC1486A monitors the voltage at LX, and if it is greater than a set threshold voltage of 140mV (nom.) the bottom MOSFET is turned off. The device then waits for approximately 2µs and then DL goes high for 300ns (typ.) once more to sense the current. This repeats until either the over-current condition goes away or the part

Application Information (Cont.)

Current Limit Circuit (Cont.)
latches off due to output overvoltage (see Output Overvoltage Protection).

Power Good Output
Each controller has its own power good output. Power good is an open-drain output and requires a pull-up resistor. When the output voltage is 10% above or below its set voltage, PGD gets pulled low. It is held low until the output voltage returns to within 10% of the output set voltage. PGD is also held low during start-up and will not be allowed to transition high until soft start is over (440 switching cycles) and the output reaches 90% of its set voltage. There is a 5µs delay built into the PGD circuitry to prevent false transitions.

Output Overvoltage Protection
When the output exceeds 10% of the its set voltage the low-side MOSFET is latched on. It stays latched on and the controller is latched off until reset (see below). There is a 5µs delay built into the OV protection circuit to prevent false transitions. An OV fault in either controller will not cause the other one to shutdown. Note: to reset VDDQ from any fault, VCCA1 or EN/PSV1 must be toggled. To reset VTT from a fault, VCCA2 or REFIN must be toggled.

Output Undervoltage Protection
When the output is 30% below its set voltage the output is latched in a tri-stated condition. It stays latched and the controller is latched off until reset (see below). There is a 5µs delay built into the UV protection circuit to prevent false transitions. An UV fault in either controller will not cause the other one to shutdown. Note: to reset VDDQ from any fault, VCCA1 or EN/PSV1 must be toggled. To reset VTT from a fault, VCCA2 or REFIN must be toggled.

POR, UVLO and Softstart
An internal power-on reset (POR) occurs when VCCA1 and VCCA2 exceed 3V, resetting the fault latch and soft-start counter, and preparing the PWM for switching. VCCA undervoltage lockout (UVLO) circuitry inhibits switching and forces the DL gate driver high until VCCA rises above 4.2V. At this time the circuit will come out of UVLO and begin switching, and with the softstart circuit enabled, will progressively limit the output current (by limiting the current out of the ILIM pin) over a predetermined time period of 440 switching cycles.

The ramp occurs in four steps:
1) 110 cycles at 25% ILIM with double minimum off-time
2) 110 cycles at 50% ILIM with normal minimum off-time
3) 110 cycles at 75% ILIM with normal minimum off-time
4) 110 cycles at 100% ILIM with normal minimum off-time. At this point the output undervoltage and power good circuitry is enabled.

There is 100mV of hysteresis built into the UVLO circuit and when VCCA falls to 4.1V (nom.) the output drivers are shut down and tristated.

MOSFET Gate Drivers
The DH and DL drivers are optimized for driving moderate-sized high-side, and larger low-side power MOSFETs. An adaptive dead-time circuit monitors the DL output and prevents the high-side MOSFET from turning on until DL is fully off (below ~1V). Conversely, it monitors the phase node, LX, to determine the state of the high side MOSFET, and prevents the low-side MOSFET from turning on until DH is fully off (LX below ~1V). Be sure there is low resistance and low inductance between the DH and DL outputs to the gate of each MOSFET.

DDR Reference Buffer
The reference buffer is capable of driving 3mA and sinking 25µA. Since the output is class A, if additional sinking is required an external pulldown resistor can be added. Make sure that the ground side of this pulldown is tied to VSSA2. As with most opamps, a small resistor is required when driving a capacitive load. To ensure stability use either a 10Ω resistor in series with a 1µF capacitor or a 100Ω resistor in series with a 0.1µF capacitor from REFOUT to AGND2.

Since it is possible to have as much as 10µF to 20µF of capacitance at the memory socket or on-board the DIMMs, it is recommended that a 0Ω resistor is placed between REFOUT and the DIMM sockets. This allows the addition of extra resistance between REFOUT and the DIMMs to avoid spurious OVP at startup, which can occur if REFOUT rises really slowly and VTT overshoots it. The extra resistance allows REFOUT to rise faster, avoiding this issue.

REFIN should also be filtered so that VDDQ ripple does not appear at the REFIN pin. If a resistor divider is used to create REFIN from VDDQ, then a 0.1µF capacitor from REFIN to VSSA2 will provide adequate filtering.

Application Information (Cont.)

Dropout Performance

The output voltage adjust range for continuous-conduction operation is limited by the fixed 550ns (maximum) minimum off-time one-shot. For best dropout performance, use the slowest on-time setting of 200kHz. When working with low input voltages, the duty-factor limit must be calculated using worst-case values for on and off times. The IC duty-factor limitation is given by:

$$DUTY = \frac{t_{ON(MIN)}}{t_{ON(MIN)} + t_{OFF(MAX)}}$$

Be sure to include inductor resistance and MOSFET on-state voltage drops when performing worst-case dropout duty-factor calculations.

SC1486A System DC Accuracy (VTT Controller)

Two IC parameters effect system DC accuracy, the error comparator offset voltage, and the switching frequency variation with line and load. The SC1486A regulates to the REFOUT voltage not the REFIN voltage. Since DDR specifications are written with respect to REFOUT, the offset of the reference buffer does not create a regulation error.

The error comparator offset does not drift significantly with supply and temperature. Thus, the error comparator contributes 1% or less to DC system inaccuracy.

The on pulse in the SC1486A is calculated to give a pseudo fixed frequency. Nevertheless, some frequency variation with line and load can be expected. This variation changes the output ripple voltage. Because constant on regulators regulate to the valley of the output ripple, ½ of the output ripple appears as a DC regulation error. For example, if REFOUT=1.25V, then the valley of the output ripple will be 1.25V. If the ripple is 20mV with VIN = 6V, then the DC output voltage will be 1.26V. If the ripple is 40mV with VIN = 25V, then the DC output voltage will be 1.27V.

1486 System DC Accuracy (VDDQ Controller)

Two IC parameters affect system DC accuracy, the error comparator threshold voltage variation and the switching frequency variation with line and load.

The error comparator threshold does not drift significantly with supply and temperature. Thus, the error comparator contributes 1% or less to DC system inaccuracy.

Board components and layout also influence DC accuracy. The use of 1% feedback resistors contribute 1%. If tighter DC accuracy is required use 0.1% feedback resistors.

The on pulse in the SC1486A is calculated to give a pseudo fixed frequency. Nevertheless, some frequency variation with line and load can be expected. This variation changes the output ripple voltage. Because constant on regulators regulate to the valley of the output ripple, ½ of the output ripple appears as a DC regulation error. For example, if the feedback resistors are chosen to divide down the output by a factor of five, the valley of the output ripple will be 2.5V. If the ripple is 50mV with VIN = 6V, then the measured DC output will be 2.525V. If the ripple increases to 80mV with VIN = 25V, then the measured DC output will be 2.540V.

The output inductor value may change with current. This will change the output ripple and thus the DC output voltage. It will not change the frequency.

Switching frequency variation with load can be minimized by choosing MOSFETs with lower $R_{DS(ON)}$. High $R_{DS(ON)}$ MOSFETs will cause the switching frequency to increase as the load current increases. This will reduce the ripple and thus the DC output voltage.

DDR Supply Selection

The SC1486A can be configured so that VTT and VDDQ are generated directly from the battery. Alternatively, the VTT supply can be generated from the VDDQ supply. Since the battery configuration generally yields better efficiency and performance, the evaluation board is configured to generate both supplies from the battery.

Application Information (Cont.)

Design Procedure

Prior to designing an output and making component selections, it is necessary to determine the input voltage range and the output voltage specifications. For purposes of demonstrating the procedure the VDDQ output for the schematic on page 17 will be designed.

The maximum input voltage ($V_{IN(MAX)}$) is determined by the highest AC adaptor voltage. The minimum input voltage ($V_{IN(MIN)}$) is determined by the lowest battery voltage after accounting for voltage drops due to connectors, fuses and battery selector switches. For the purposes of this design example we will use a V_{IN} range of 7.5V to 20.5V.

Four parameters are needed for the output:
1) nominal output voltage, V_{OUT} (for DDR2 this is 1.8V)
2) static (or DC) tolerance, TOL_{ST} (for DDR2 this is +/-0.1V)
3) transient tolerance, TOL_{TR} and size of transient (for DDR2 this is undefined, so assume +/-8% for purposes of this demonstration).
4) maximum output current, I_{OUT} (we will design for 10A)

Switching frequency determines the trade-off between size and efficiency. Increased frequency increases the switching losses in the MOSFETs, since losses are a function of VIN^2. Knowing the maximum input voltage and budget for MOSFET switches usually dictates where the design ends up. It is recommended that the two outputs are designed to operate at frequencies approximately 25% apart to avoid any possible interaction. It is also recommended that the higher frequency output is the lower output voltage output, since this will tend to have lower output ripple and tighter specifications. The default R_{tON} values of 1MΩ and 649kΩ are suggested as a starting point, but these are not set in stone. The first thing to do is to calculate the on-time, t_{ON}, at $V_{IN(MIN)}$ and $V_{IN(MAX)}$, since this depends only upon V_{IN}, V_{OUT} and R_{tON}. For V_{OUT} < 3.3V:

$$t_{ON\_VIN(MIN)} = \left[3.3 \bullet 10^{-12} \bullet \left(R_{tON} + 37 \bullet 10^{3}\right) \bullet \frac{V_{OUT}}{V_{IN(MIN)}}\right] + 50 \bullet 10^{-9} s$$

and

$$t_{ON\_VIN(MAX)} = \left[3.3 \bullet 10^{-12} \bullet \left(R_{tON} + 37 \bullet 10^{3}\right) \bullet \frac{V_{OUT}}{V_{IN(MAX)}}\right] + 50 \bullet 10^{-9} s$$

From these values of t_{ON} we can calculate the nominal switching frequency as follows:

$$f_{SW\_VIN(MIN)} = \frac{V_{OUT}}{\left(V_{IN(MIN)} \bullet t_{ON\_VIN(MIN)}\right)} Hz$$

and

$$f_{SW\_VIN(MAX)} = \frac{V_{OUT}}{\left(V_{IN(MAX)} \bullet t_{ON\_VIN(MAX)}\right)} Hz$$

t_{ON} is generated by a one-shot comparator that samples V_{IN} via R_{tON}, converting this to a current. This current is used to charge an internal 3.3pF capacitor to V_{OUT}. The equations above reflect this along with any internal components or delays that influence t_{ON}. For our DDR2 VDDQ example we select R_{tON} = 1MΩ:

$t_{ON\_VIN(MIN)}$ = 871ns and $t_{ON\_VIN(MAX)}$ = 350ns

$f_{SW\_VIN(MIN)}$ = 275kHz and $f_{SW\_VIN(MAX)}$ = 251kHz

Now that we know t_{ON} we can calculate suitable values for the inductor. To do this we select an acceptable inductor ripple current. The calculations below assume 50% of I_{OUT} which will give us a starting place.

$$L_{VIN(MIN)} = \left(V_{IN(MIN)} - V_{OUT}\right) \bullet \frac{t_{ON\_VIN(MIN)}}{\left(0.5 \bullet I_{OUT}\right)} H$$

and

$$L_{VIN(MAX)} = \left(V_{IN(MAX)} - V_{OUT}\right) \bullet \frac{t_{ON\_VIN(MAX)}}{\left(0.5 \bullet I_{OUT}\right)} H$$

For our DDR2 VDDQ example:

$L_{VIN(MIN)}$ = 1µH and $L_{VIN(MAX)}$ = 1.3µH

We will select an inductor value of 2.4µH to reduce the ripple current, which can be calculated as follows:

$$I_{RIPPLE\_VIN(MIN)} = \left(V_{IN(MIN)} - V_{OUT}\right) \bullet \frac{t_{ON\_VIN(MIN)}}{L} A_{P-P}$$

and

$$I_{RIPPLE\_VIN(MAX)} = \left(V_{IN(MAX)} - V_{OUT}\right) \bullet \frac{t_{ON\_VIN(MAX)}}{L} A_{P-P}$$

Application Information (Cont.)

Design Procedure (Cont.)

For our DDR2 VDDQ example:

$I_{RIPPLE\_VIN(MIN)}$ = 2.07A_{P-P} and $I_{RIPPLE\_VIN(MAX)}$ = 2.73A_{P-P}

From this we can calculate the minimum inductor current rating for normal operation:

$$I_{INDUCTOR(MIN)} = I_{OUT(MAX)} + \frac{I_{RIPPLE\_VIN(MAX)}}{2} A_{(MIN)}$$

For our DDR2 VDDQ example:

$I_{INDUCTOR(MIN)}$ = 11.4$A_{(MIN)}$

Next we will calculate the maximum output capacitor equivalent series resistance (ESR). This is determined by calculating the remaining static and transient tolerance allowances. Then the maximum ESR is the smaller of the calculated static ESR ($R_{ESR\_ST(MAX)}$) and transient ESR ($R_{ESR\_TR(MAX)}$):

$$R_{ESR\_ST(MAX)} = \frac{(ERR_{ST} - ERR_{DC}) \bullet 2}{I_{RIPPLE\_VIN(MAX)}} Ohms$$

Where ERR_{ST} is the static output tolerance and ERR_{DC} is the DC error. The DC error will be 1% plus the tolerance of the feedback resistors, thus 2% total for 1% feedback resistors.

For our DDR2 VDDQ example:

ERR_{ST} = 100mV and ERR_{DC} = 36mV, therefore

$R_{ESR\_ST(MAX)}$ = 47mΩ

$$R_{ESR\_TR(MAX)} = \frac{(ERR_{TR} - ERR_{DC})}{\left(I_{OUT} + \frac{I_{RIPPLE\_VIN(MAX)}}{2}\right)} Ohms$$

Where ERR_{TR} is the transient output tolerance. Note that this calculation assumes that the worst case load transient is full load. For half of full load, divide the I_{OUT} term by 2.

For our DDR2 VDDQ example:

ERR_{TR} = 144mV and ERR_{DC} = 36mV, therefore

$R_{ESR\_TR(MAX)}$ = 9.5mΩ for a full 10A load transient

We will select a value of 12.5mΩ maximum for our design, which would be achieved by using two 25mΩ output capacitors in parallel.

Note that for constant-on converters there is a minimum ESR requirement for stability which can be calculated as follows:

$$R_{ESR(MIN)} = \frac{3}{2 \bullet \pi \bullet C_{OUT} \bullet f_{SW}}$$

This criteria should be checked once the output capacitance has been determined.

Now that we know the output ESR we can calculate the output ripple voltage:

$$V_{RIPPLE\_VIN(MAX)} = R_{ESR} \bullet I_{RIPPLE\_VIN(MAX)} V_{P-P}$$

and

$$V_{RIPPLE\_VIN(MIN)} = R_{ESR} \bullet I_{RIPPLE\_VIN(MIN)} V_{P-P}$$

For our DDR2 VDDQ example:

$V_{RIPPLE\_VIN(MAX)}$ = 34mV_{P-P} and $V_{RIPPLE\_VIN(MIN)}$ = 26mV_{P-P}

Note that in order for the device to regulate in a controlled manner, the ripple content at the feedback pin, V_{FB}, should be approximately 15mV_{P-P} at minimum V_{IN}, and worst case no smaller than 10mV_{P-P}. If $V_{RIPPLE\_VIN(MIN)}$ is less than 15mV_{P-P} the above component values should be revisited in order to improve this. Quite often a small capacitor, C_{TOP}, is required in parallel with the top feedback resistor, R_{TOP}, in order to ensure that V_{FB} is large enough. C_{TOP} should not be greater than 100pF. The value of C_{TOP} can be calculated as follows, where R_{BOT} is the bottom feedback resistor. Firstly calculating the value of Z_{TOP} required:

$$Z_{TOP} = \frac{R_{BOT}}{0.015} \bullet (V_{RIPPLE\_VIN(MIN)} - 0.015) Ohms$$

Secondly calculating the value of C_{TOP} required to achieve this:

Application Information (Cont.)

Design Procedure (Cont.)

$$C_{TOP} = \frac{\left(\frac{1}{Z_{TOP}} - \frac{1}{R_{TOP}}\right)}{2 \bullet \pi \bullet f_{SW\_VIN(MIN)}} F$$

For our DDR2 VDDQ example we will use R_{TOP} = 45.3kΩ and R_{BOT} = 17.4kΩ, therefore:

Z_{TOP} = 12.8kΩ and C_{TOP} = 32pF

We will select a value of C_{TOP} = 27pF. Calculating the value of V_{FB} based upon the selected C_{TOP}:

$$V_{FB\_VIN(MIN)} = V_{RIPPLE\_VIN(MIN)} \bullet \left(\frac{\frac{R_{BOT}}{1}}{R_{BOT} + \frac{1}{\frac{1}{R_{TOp}} + 2 \bullet \pi \bullet f_{SW\_VIN(MIN)} \bullet C_{TOP}}} \right) V_{P-P}$$

For our DDR2 VDDQ example:

$V_{FB\_VIN(MIN)}$ = 14.2mV_{P-P} - good

Next we need to calculate the minimum output capacitance required to ensure that the output voltage does not exceed the transient maximum limit, $POSLIM_{TR}$, starting from the actual static maximum, $V_{OUT\_ST\_POS}$, when a load release occurs:

$$V_{OUT\_ST\_POS} = V_{OUT} + ERR_{DC}\ V$$

For our DDR2 VDDQ example:

$V_{OUT\_ST\_POS}$ = 1.836V

$$POSLIM_{TR} = V_{OUT} \bullet TOL_{TR}\ V$$

Where TOL_{TR} is the transient tolerance. For our DDR2 VDDQ example:

$POSLIM_{TR}$ = 1.944V

The minimum output capacitance is calculated as follows:

$$C_{OUT(MIN)} = L \bullet \frac{\left(I_{OUT} + \frac{I_{RIPPLE\_VIN(MAX)}}{2}\right)^2}{\left(POSLIM_{TR}^{\ 2} - V_{OUT\_ST\_POS}^{\ 2}\right)} F$$

This calculation assumes the absolute worst case condition of a full-load to no load step transient occurring when the inductor current is at its highest. The capacitance required for smaller transient steps my be calculated by substituting the desired current for the I_{OUT} term.

For our DDR2 VDDQ example:

$C_{OUT(MIN)}$ = 760µF.

We will select 660µF, using two 330µF, 25mΩ capacitors in parallel.

Next we calculate the RMS input ripple current, which is largest at the minimum battery voltage:

$$I_{IN(RMS)} = \sqrt{V_{OUT} \bullet \left(V_{IN(MIN)} - V_{OUT}\right)} \bullet \frac{I_{OUT}}{V_{IN\_MIN}} A_{RMS}$$

For our DDR2 VDDQ example:

$I_{IN(RMS)}$ = 4.27A_{RMS}

Input capacitors should be selected with sufficient ripple current rating for this RMS current, for example a 10µF, 1210 size, 25V ceramic capacitor can handle a little more than 2A_{RMS}. Refer to manufacturer's data sheets.

Finally, we calculate the current limit resistor value. As described in the current limit section, the current limit looks at the "valley current", which is the average output current minus half the ripple current. We use the maximum room temperature specification for MOSFET $R_{DS(ON)}$ at V_{GS} = 4.5V for purposes of this calculation:

$$I_{VALLEY} = I_{OUT} - \frac{I_{RIPPLE\_VIN(MIN)}}{2} A$$

The ripple at low battery voltage is used because we want to make sure that current limit does not occur under normal operating conditions.

Application Information (Cont.)

Design Procedure (Cont.)

$$R_{ILIM} = (I_{VALLEY} \bullet 1.2) \bullet \frac{R_{DS(ON)} \bullet 1.4}{10 \bullet 10^{-6}} \text{ Ohms}$$

For our DDR2 VDDQ example:

I_{VALLEY} = 8.97A and R_{ILIM} = 13.6kΩ

We select the next lowest 1% resistor value: 13.3kΩ

Thermal Considerations

The junction temperature of the device may be calculated as follows:

$$T_J = T_A + P_D \bullet \theta_{JA} \quad °C$$

Where:
T_A = ambient temperature (°C)
P_D = power dissipation in (W)
θ_{JA} = thermal impedance junction to ambient from absolute maximum ratings (°C/W)

The power dissipation may be calculated as follows:

$$P_D = 2 \bullet (VCCA \bullet I_{VCCA} + V_g \bullet Q_g \bullet f) \quad W$$

Where:
VCCA = chip supply voltage (V)
I_{VCCA} = operating current (A)
V_g = gate drive voltage, typically 5V (V)
Q_g = FET gate charge, from the FET datasheet (C)
f = switching frequency (kHz)

Inserting the following values as an example:
T_A = 85°C
θ_{JA} = 37°C/W
VCCA = 5V
I_{VCCA} = 1100µA (data sheet maximum)
V_g = 5V
Q_g = 60nC
f = 300kHz (enter the higher of the two set frequencies here)
gives us:

$$T_J = 85 + 2 \bullet (5 \bullet 1100 \bullet 10^{-6} + 5 \bullet 60 \bullet 10^{-9} \bullet 300 \bullet 10^{3}) \bullet 37 = 92 \quad °C$$

As can be seen, the heating effects due to internal power dissipation are practically negligible, thus requiring no special consideration thermally during layout.

Application Information (Cont.)

Layout Guidelines

One (or more) ground planes is/are recommended to minimize the effect of switching noise and copper losses, and maximize heat dissipation. The IC ground references, VSSA1 and VSSA2, should be kept separate from power ground. All components that are referenced to them should connect to them locally at the chip. VSSA1 and VSSA2 should connect to power ground at their respective output capacitors only.

Feedback traces must be kept far away from noise sources such as switching nodes, inductors and gate drives. Route feedback traces with their respective VSSAs as a differential pair from the output capacitor back to the chip. Run them in a “quiet layer” if possible.

Chip decoupling capacitors (VDDP, VCCA) should be located next to the pins and connected directly to them on the same side.

Power sections should connect directly to the ground plane(s) using multiple vias as required for current handling (including the chip power ground connections). Power components should be placed to minimize loops and reduce losses. Make all the connections on one side of the PCB using wide copper filled areas if possible. Do not use “minimum” land patterns for power components. Minimize trace lengths between the gate drivers and the gates of the MOSFETs to reduce parasitic impedances (and MOSFET switching losses), the low-side MOSFET is most critical. Maintain a length to width ratio of <20:1 for gate drive signals. Use multiple vias as required by current handling requirement (and to reduce parasitics) if routed on more than one layer

Current sense connections must always be made using Kelvin connections to ensure an accurate signal.

We will examine the SC1486A DDR2 reference design used in the Design Procedure section while explaining the layout guidelines in more detail.

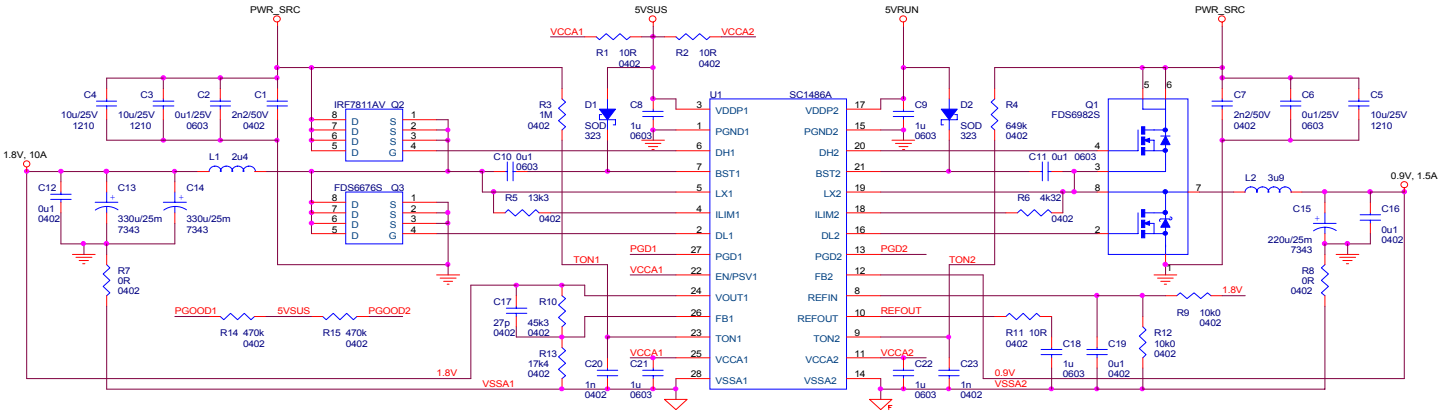


Figure 4: DDR2 Reference Design and Layout Example

Sample DDR2 Design Using SC1486A
PWR_SRC = 7.5V to 20.5V

VDDQ = 1.8V @ 10A
VTT = 0.9V @ 1.5A
Schematic is drawn to emphasize required grounding scheme

Layout Guidelines (Cont.)

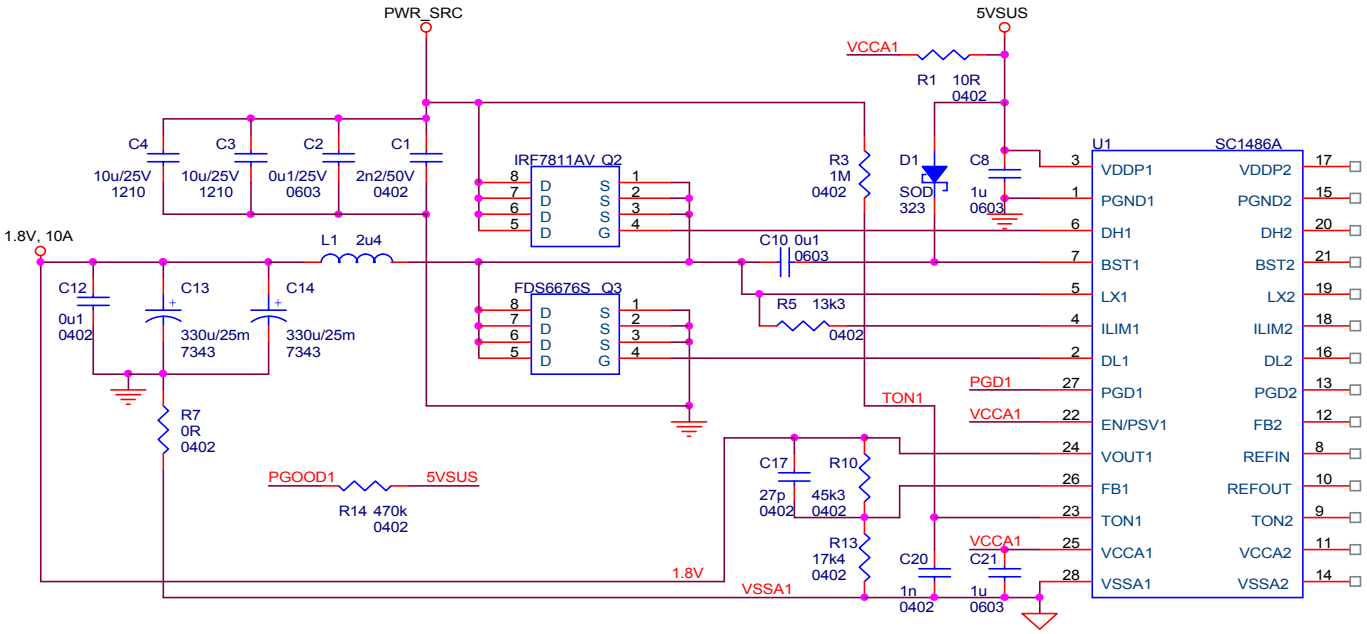


Figure 5: VDDQ Side Detail

Note R7 is present to facilitate isolation of power ground and VSSA1 during layout

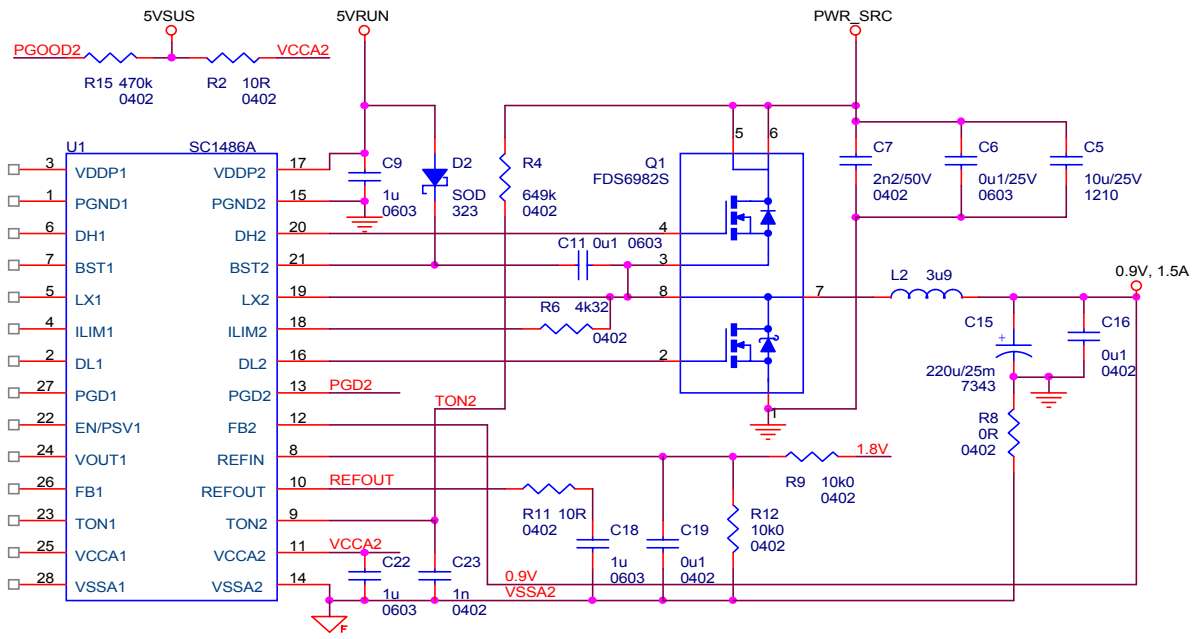


Figure 6: VTT Side Detail

Note R8 is present to facilitate isolation of power ground and VSSA2 during layout

Layout Guidelines (Cont.)

The layout can be considered in two parts, the control section referenced to VSSA1/2 and the power section. Looking at the control section first, locate all components referenced to VSSA1/2 on the schematic and place these components at the chip. Connect VSSA1 and VSSA2 using either a wide (>0.020") trace or a copper pour if room allows. Very little current flows in the chip ground therefore large areas of copper are not needed.

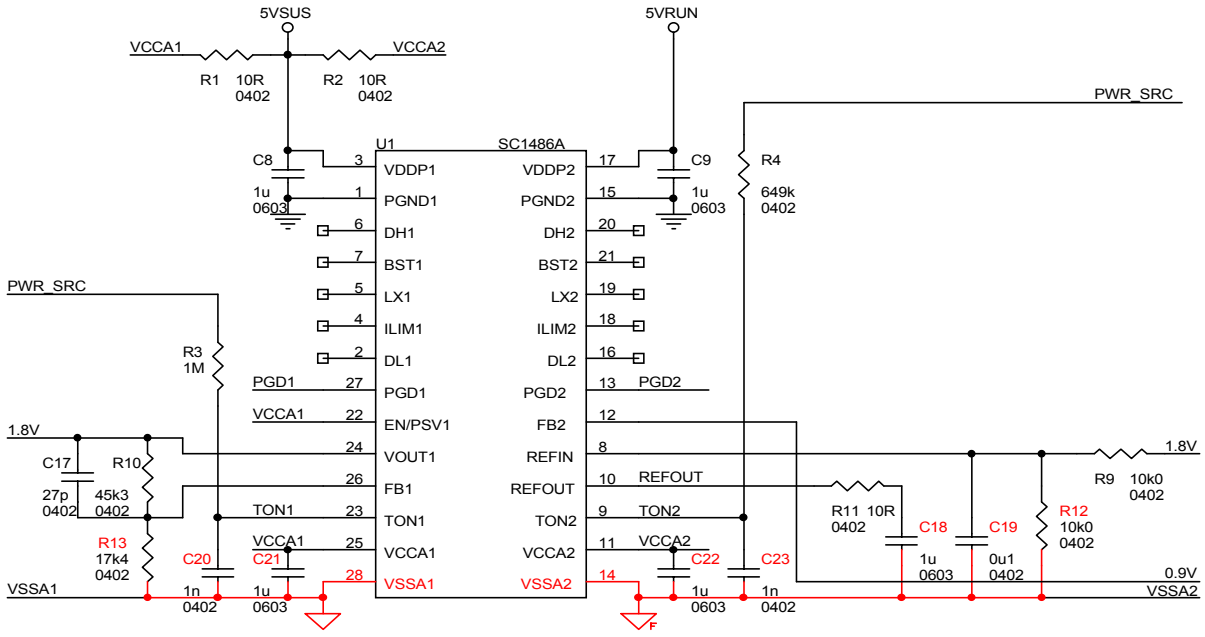


Figure 7: Components Connected to VSSA1 and VSSA2

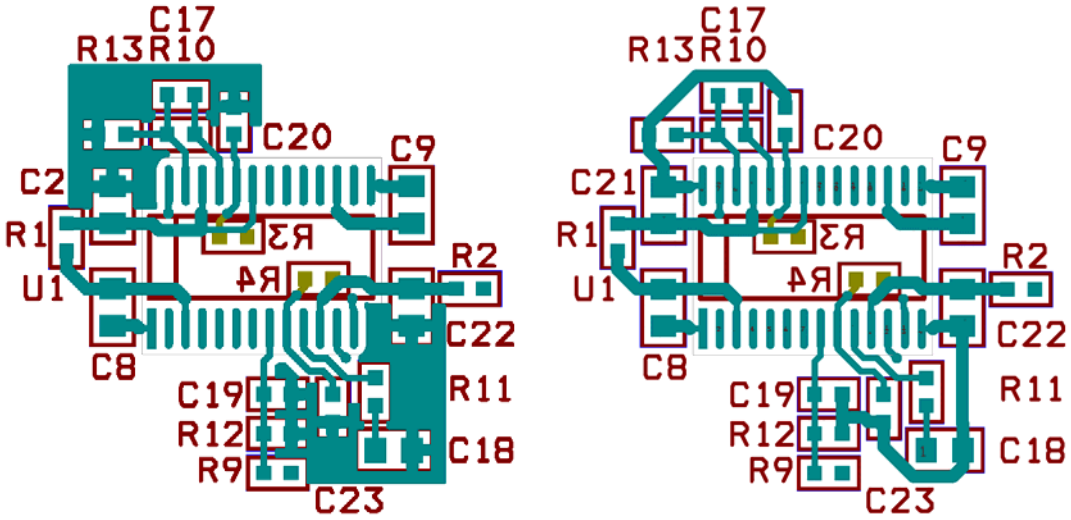


Figure 8: ExampleVSSA Copper Pours (Left) and 0.020" Traces (Right)

Application Information (Cont.)

Layout Guidelines (Cont.)

In Figure 8 on Page 19, all components referenced to VSSA1 and VSSA2 have been placed and have been connected using copper pours (left) or 0.020" traces (right). Note that there are two separate copper pours or traces, one for VSSA1 and one for VSSA2. Decoupling capacitors C2 and C22 are as close as possible to their pins, as are VDDP decoupling capacitors C8 and C9. C8 and C9 should connect to the ground plane using two vias each.

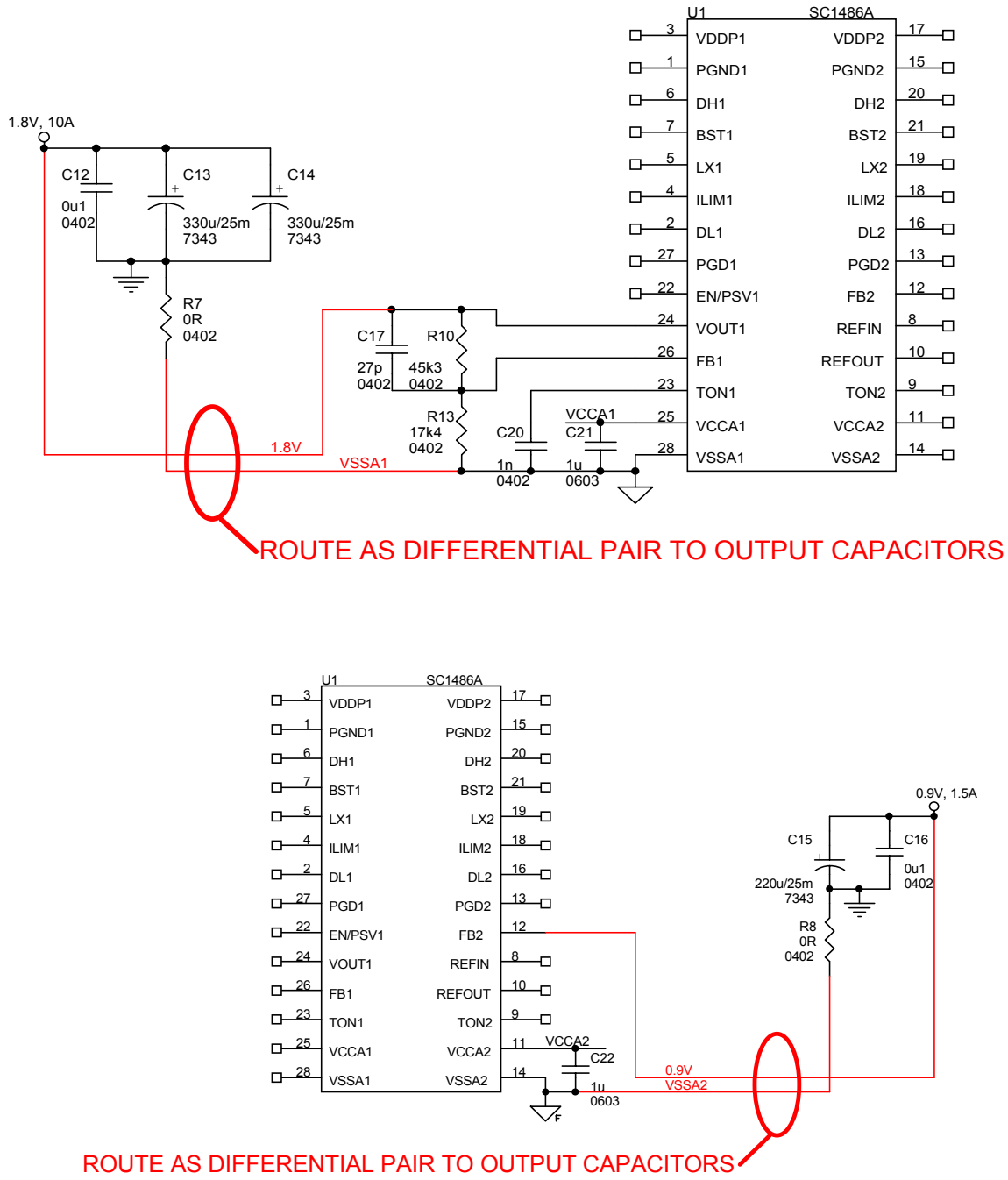


Figure 9: Differential Routing of Feedback and Ground Reference Traces

Application Information (Cont.)

Layout Guidelines (Cont.)

Next, looking at the power section, the schematics in Figures 10 and 11 below show the power sections for VDDQ and VTT:

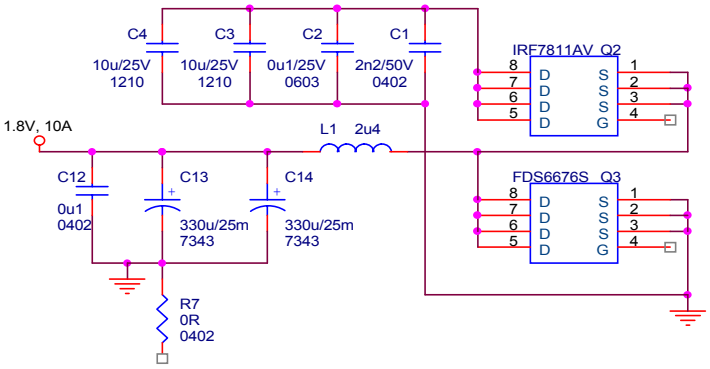


Figure 10: VDDQ Power Section

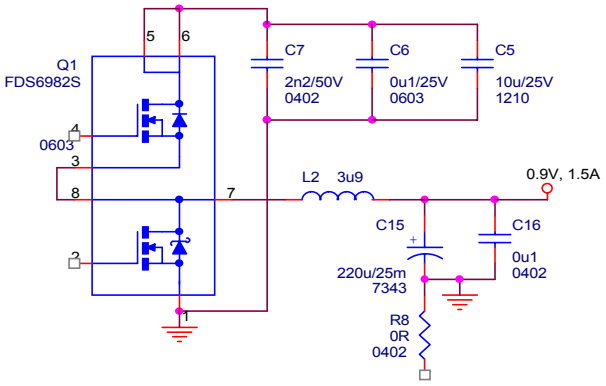


Figure 11: VTT Power Section

The highest di/dts occur in the input loops (see Figures 12 and 13 below) and thus these should be kept as small as possible.

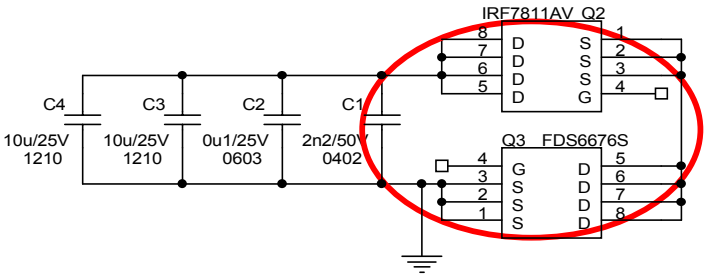


Figure 12: VDDQ Input Loop

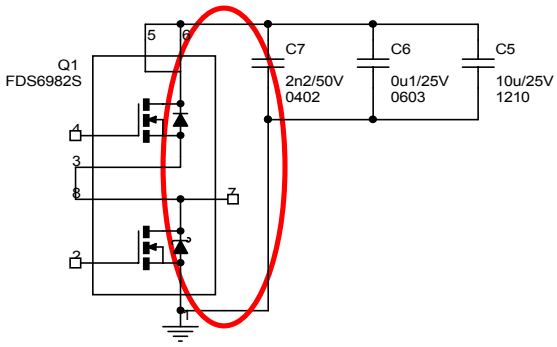


Figure 13: VTT Input Loop

The input capacitors should be placed with the highest frequency capacitors closest to the loop to reduce EMI. Use large copper pours to minimize losses and parasitics. See Figures 14 and 15 below for examples.

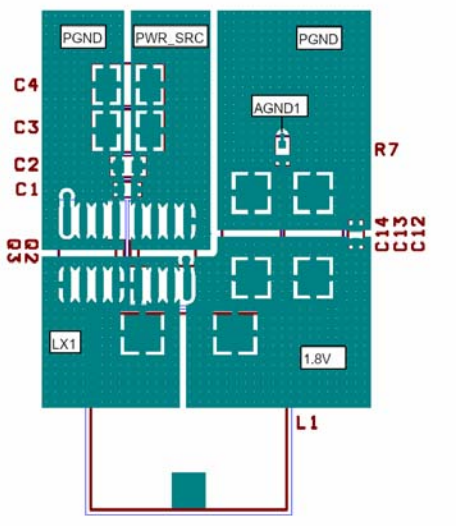


Figure 14: VDDQ Power Component Placement And Copper Pours

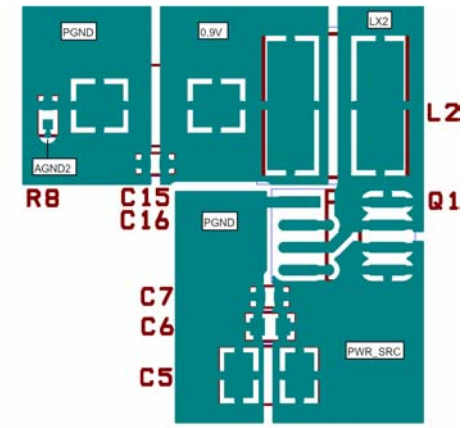


Figure 15: VTT Power Component Placement And Copper Pours

Application Information (Cont.)

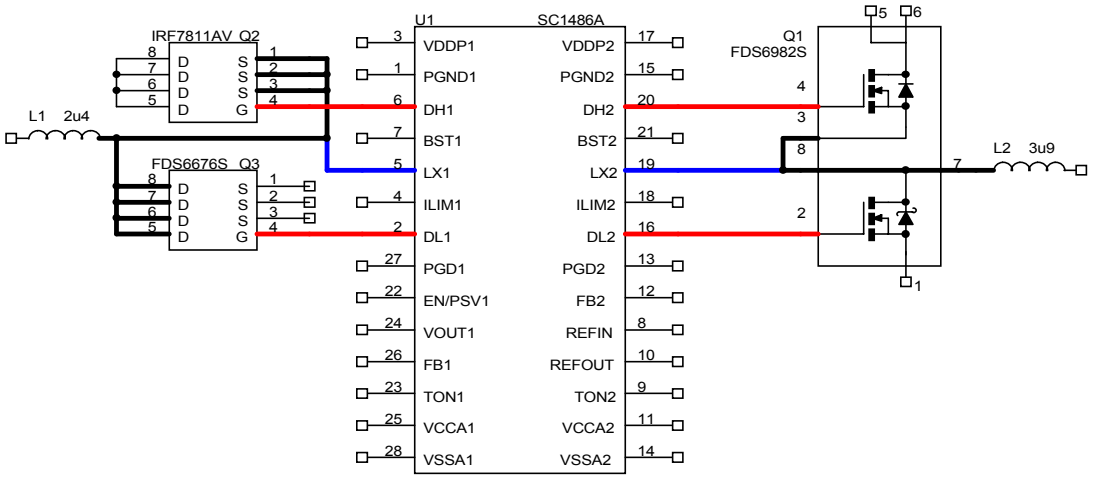
Layout Guidelines (Cont.)

Key points for the power section:

1) there should be a very small input loop, well decoupled.
2) the phase node should be a large copper pour, but compact since this is the noisiest node.
3) input power ground and output power ground should not connect directly, but through the ground planes instead.
4) The two outputs should not share their input capacitors, and these should have separate PWR_SRC and PGND (component-side) copper pours.
5) The two output inductors should not be placed adjacent to each other to avoid crosstalk.
6) Notice in Figures 10 and 11 on the previous page placement of 0Ω resistor at the bottom of the output capacitor to connect to VSSA1/2 for each output.

Connecting the control and power sections should be accomplished as follows (see Figure 16 below):

1) Route VSSA1/2 and their related feedback traces as differential pairs routed in a “quiet” layer away from noise sources.
2) Route DL, DH and LX (low side FET gate drive, high side FET gate drive and phase node) to chip using wide traces with multiple vias if using more than one layer. These connections to be as short as possible for loop minimization, with a length to width ratio less than 20:1 to minimize impedance. DL is the most critical gate drive, with power ground as its return path. LX is the noisiest node in the circuit, switching between PWR_SRC and ground at high frequencies, thus should be kept as short as practical. DH has LX as its return path.
3) BST is also a noisy node and should be kept as short as possible.
4) Connect PGND pins on the chip directly to the VDDP decoupling capacitor and then drop vias directly to the ground plane.



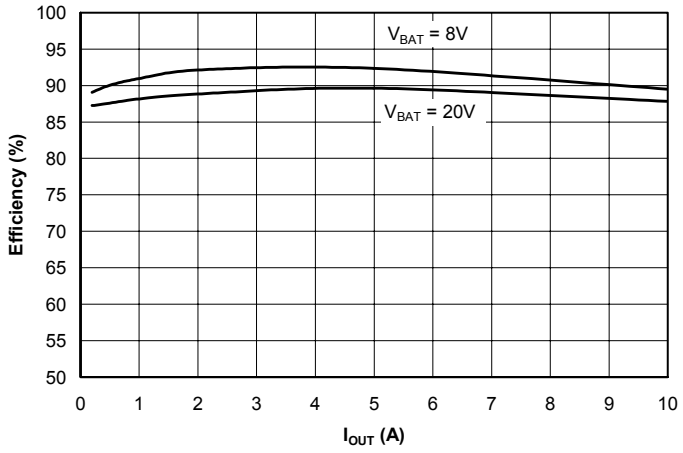
PHASE NODES (BLACK) TO BE COPPER ISLANDS (PREFERRED) OR WIDE COPPER TR

GATE DRIVE TRACES (RED) AND PHASE NODE TRACES (BLUE) TO BE WIDE COPPER TRACES (L:W < 20:1) AND AS SHORT AS POSSIBLE, WITH DL THE MOST CRITICAL

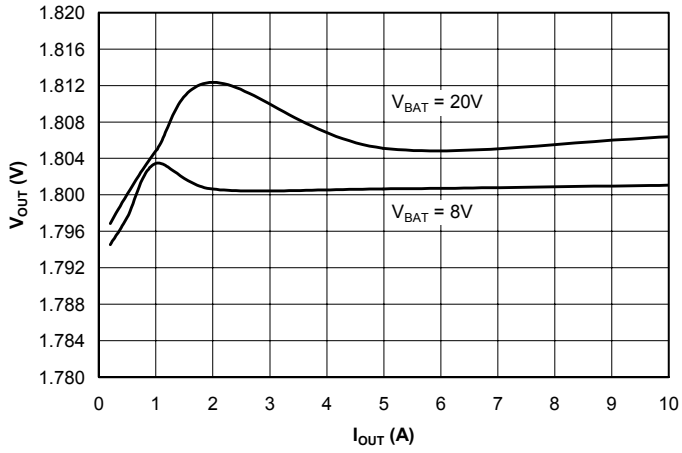
Figure 16: Connecting Control and Power Sections

Typical Characteristics

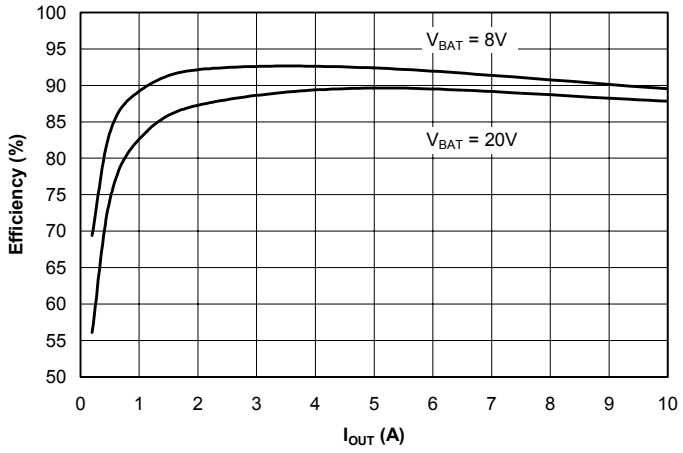
VDDQ Efficiency (Power Save Mode) vs. Output Current vs. Input Voltage



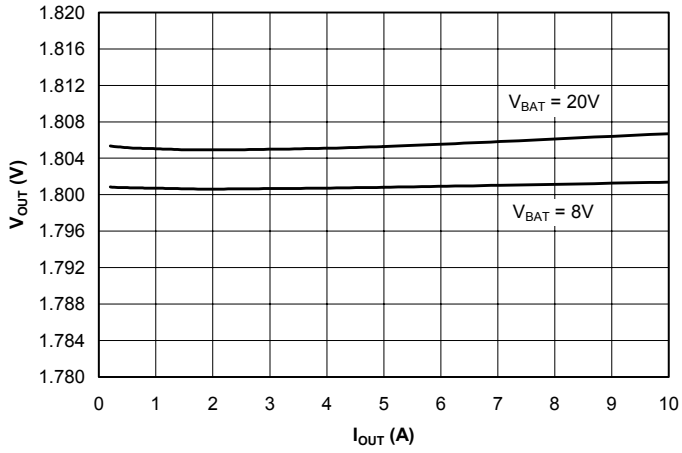
VDDQ Output Voltage (Power Save Mode) vs. Output Current vs. Input Voltage



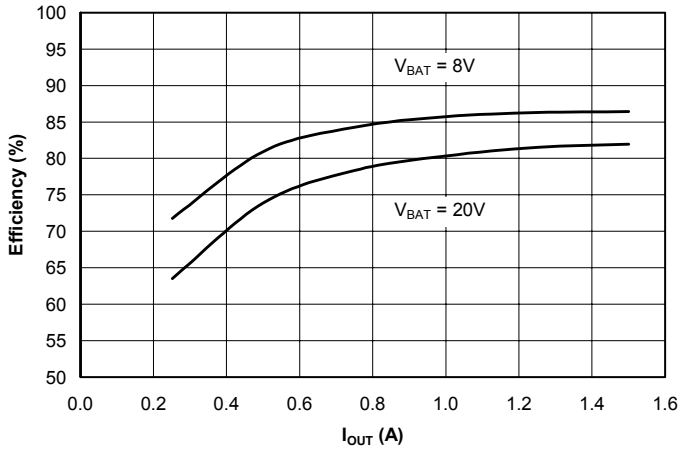
VDDQ Efficiency (Continuous Conduction Mode) vs. Output Current vs. Input Voltage



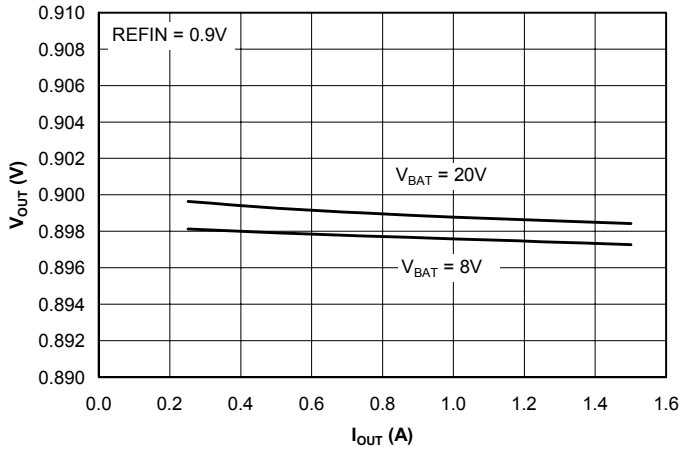
VDDQ Output Voltage (Continuous Conduction Mode) vs. Output Current vs. Input Voltage



VTT Efficiency vs. Output Current vs. Input Voltage



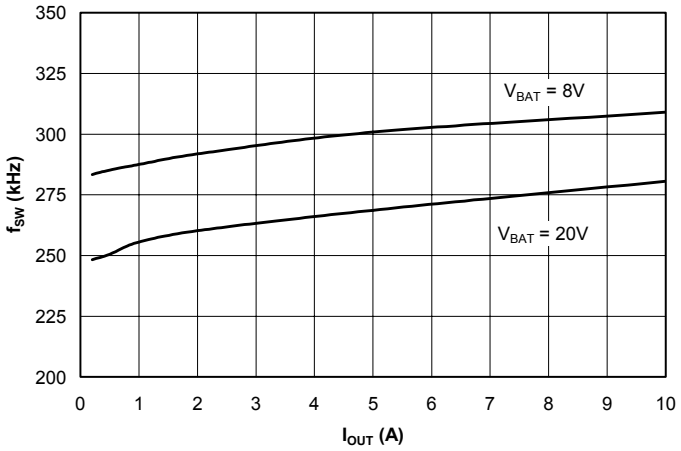
VTT Output Voltage vs. Output Current vs. Input Voltage



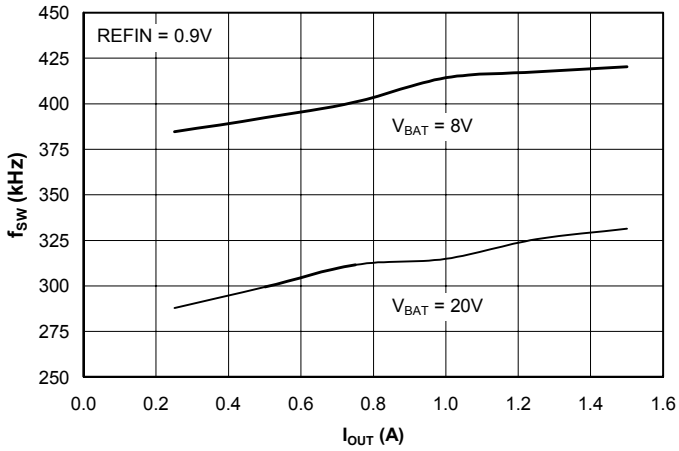
Please refer to Figure 4 on Page 17 for test schematic

Typical Characteristics (Cont.)

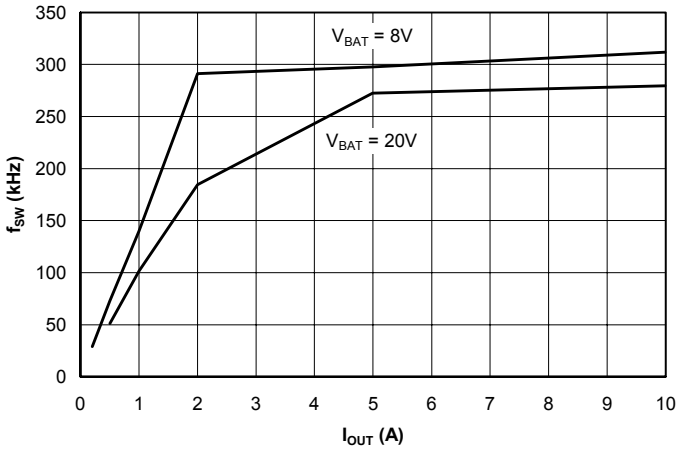
VDDQ Switching Frequency (Continuous Conduction Mode) vs. Output Current vs. Input Voltage



VTT Switching Frequency (Continuous Conduction Mode) vs. Output Current vs. Input Voltage



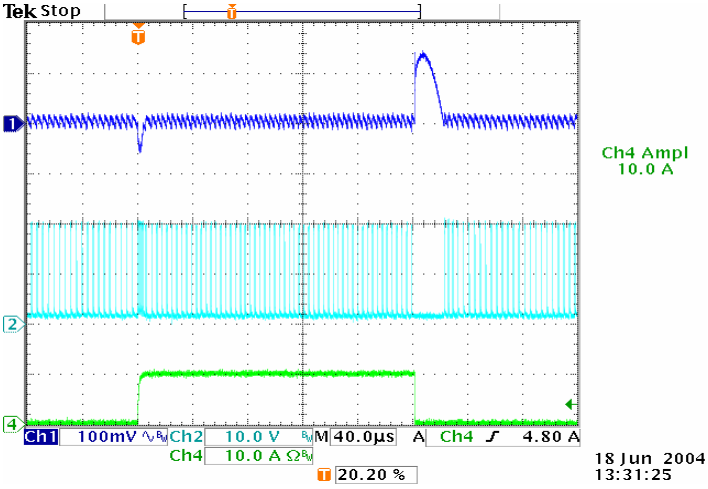
VDDQ Switching Frequency (Power Save Mode) vs. Output Current vs. Input Voltage



Please refer to Figure 4 on Page 17 for test schematic

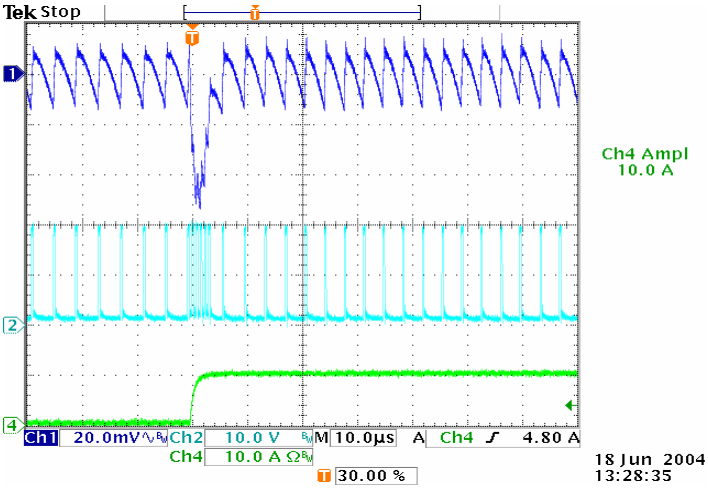
Typical Characteristics (Cont.)

**VDDQ Load Transient Response,
Continuous Conduction Mode, 0A to 10A to 0A**



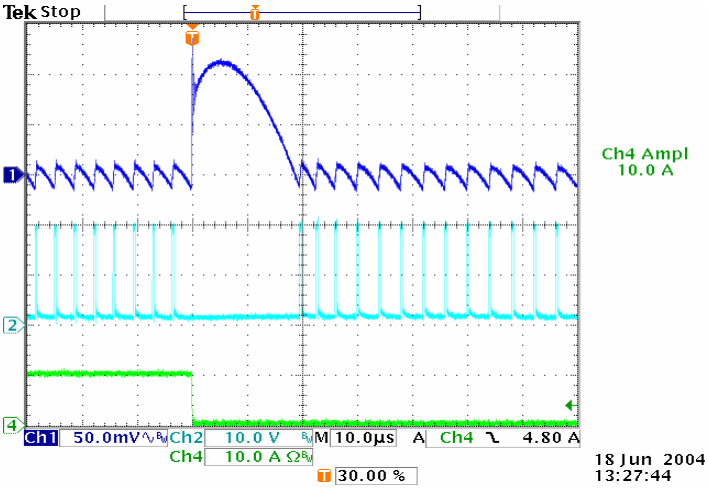
Trace 1: VDDQ, 100mV/div., AC coupled
Trace 2: LX, 10V/div
Trace 3: not connected
Trace 4: load current, 10A/div
Timebase: 40µs/div.

**VDDQ Load Transient Response,
Continuous Conduction Mode, 0A to 10A Zoomed**



Trace 1: VDDQ, 20mV/div., AC coupled
Trace 2: LX, 10V/div
Trace 3: not connected
Trace 4: load current, 10A/div
Timebase: 10µs/div.

**VDDQ Load Transient Response,
Continuous Conduction Mode, 10A to 0A Zoomed**

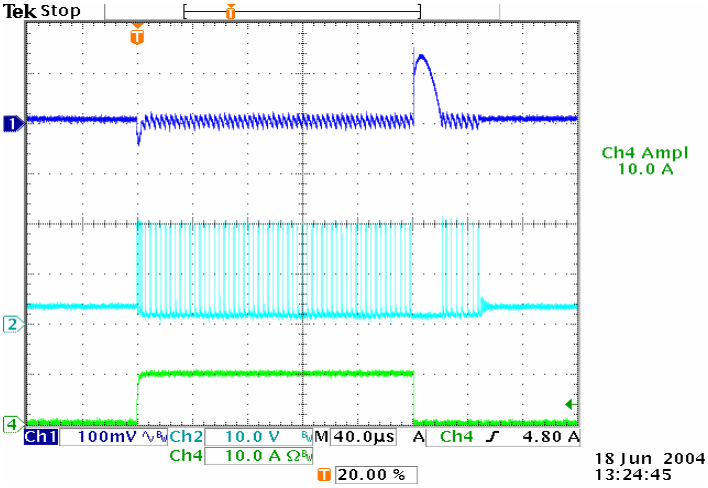


Trace 1: VDDQ, 50mV/div., AC coupled
Trace 2: LX, 10V/div
Trace 3: not connected
Trace 4: load current, 10A/div
Timebase: 10µs/div.

Please refer to Figure 4 on Page 17 for test schematic

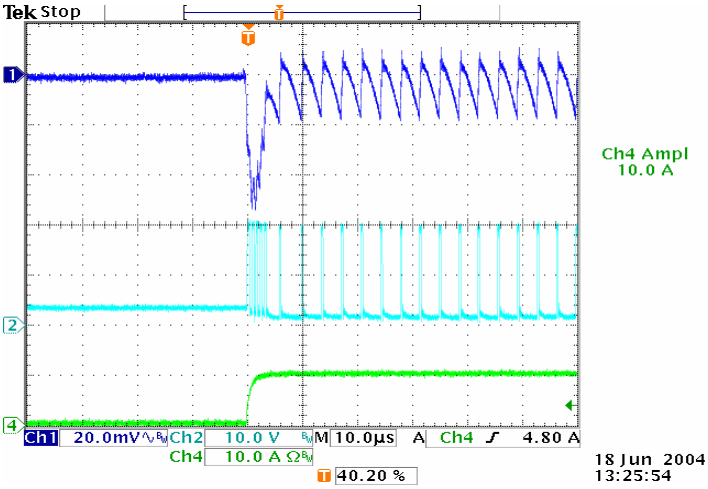
Typical Characteristics (Cont.)

VDDQ Load Transient Response, Power Save Mode, 0A to 10A to 0A



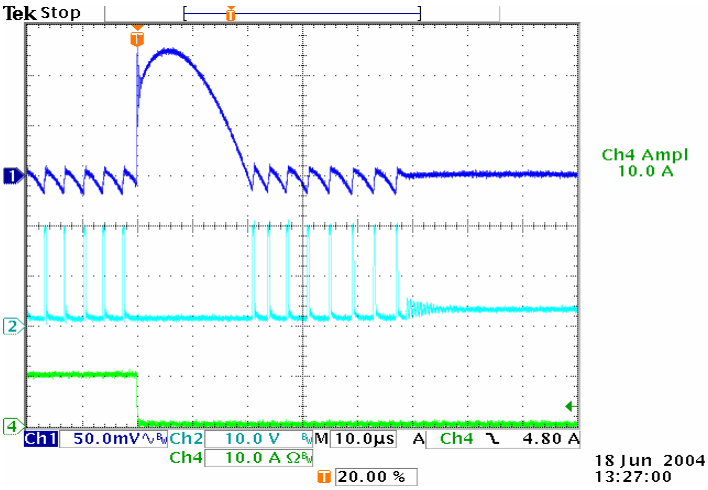
Trace 1: VDDQ, 100mV/div., AC coupled
Trace 2: LX, 10V/div
Trace 3: not connected
Trace 4: load current, 10A/div
Timebase: 40µs/div.

VDDQ Load Transient Response, Power Save Mode, 0A to 10A Zoomed



Trace 1: VDDQ, 20mV/div., AC coupled
Trace 2: LX, 10V/div
Trace 3: not connected
Trace 4: load current, 10A/div
Timebase: 10µs/div.

VDDQ Load Transient Response, Power Save Mode, 10A to 0A Zoomed

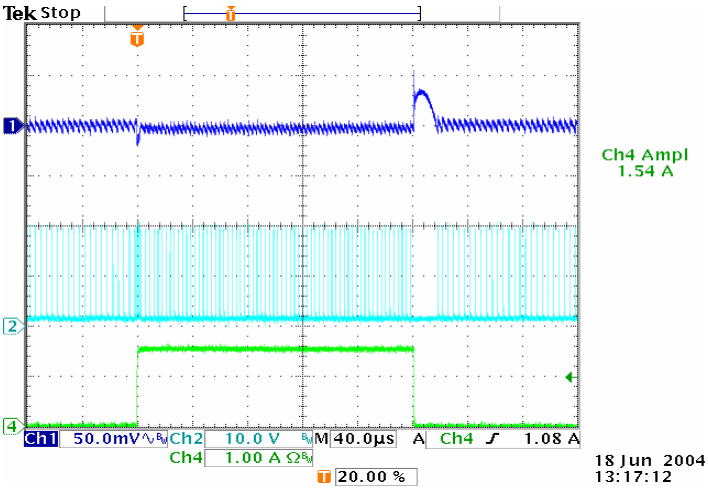


Trace 1: VDDQ, 50mV/div., AC coupled
Trace 2: LX, 10V/div
Trace 3: not connected
Trace 4: load current, 10A/div
Timebase: 10µs/div.

Please refer to Figure 4 on Page 17 for test schematic

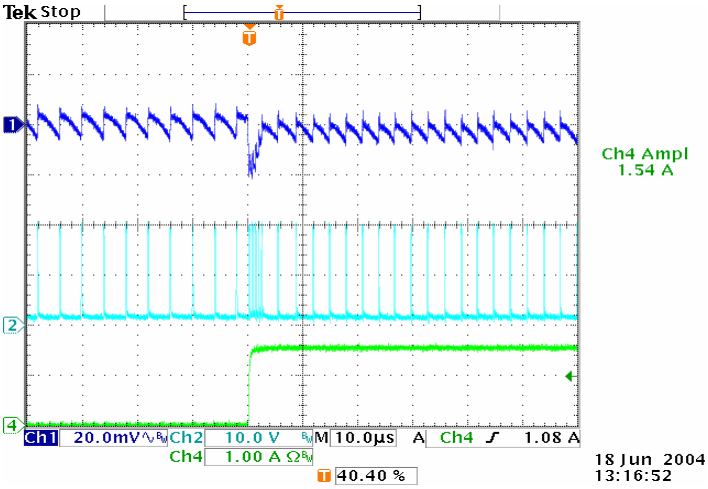
Typical Characteristics (Cont.)

VTT Load Transient Response, 0A to 1.5A to 0A



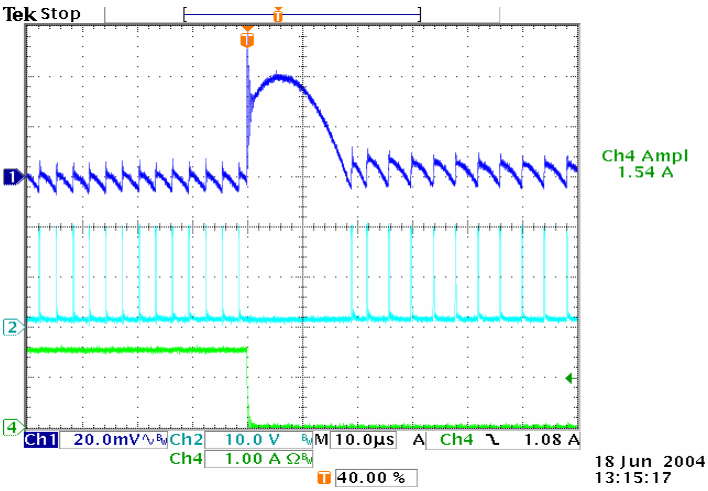
Trace 1: VTT, 50mV/div., AC coupled
Trace 2: LX, 10V/div
Trace 3: not connected
Trace 4: load current, 1A/div
Timebase: 40µs/div.

VTT Load Transient Response, 0A to 1.5A Zoomed



Trace 1: VTT, 20mV/div., AC coupled
Trace 2: LX, 10V/div
Trace 3: not connected
Trace 4: load current, 1A/div
Timebase: 10µs/div.

VTT Load Transient Response, 1.5A to 0A Zoomed

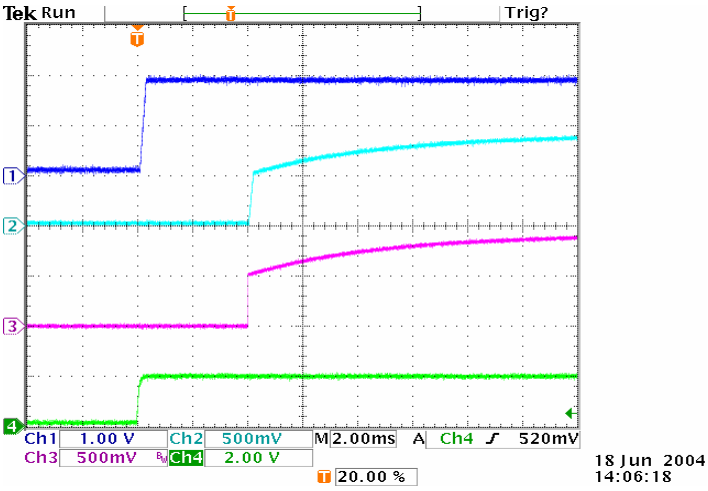


Trace 1: VTT, 20mV/div., AC coupled
Trace 2: LX, 10V/div
Trace 3: not connected
Trace 4: load current, 1A/div
Timebase: 10µs/div.

Please refer to Figure 4 on Page 17 for test schematic

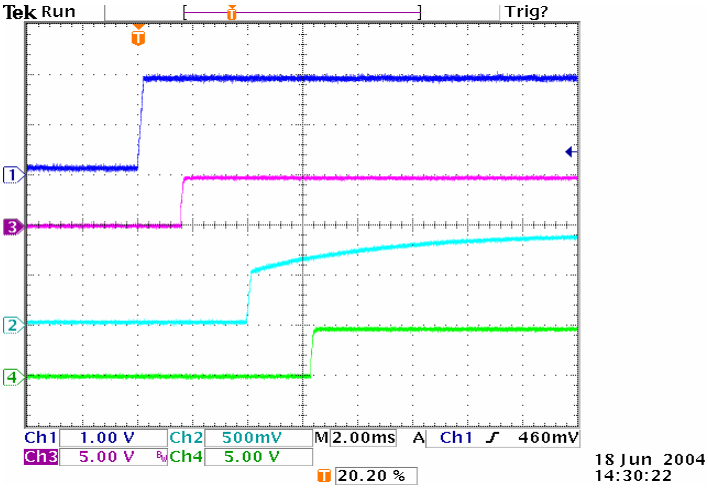
Typical Characteristics (Cont.)

Startup (CCM), EN/PSV1 Going 0V to Floating



Trace 1: VDDQ, 1V/div.
Trace 2: VTT, 0.5V/div
Trace 3: REFOUT, 0.5V/div
Trace 4: En/PSV1, 2V/div.
Timebase: 2ms/div.

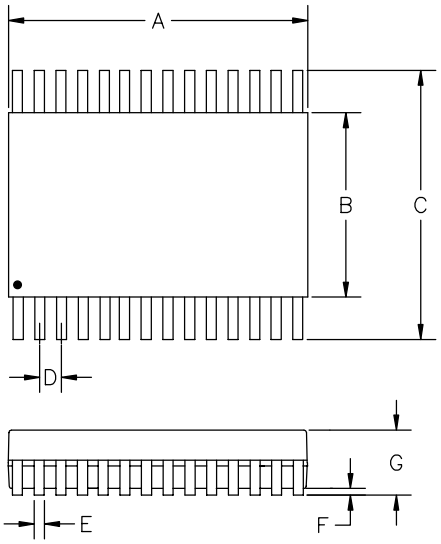
Startup (CCM) Showing PGD1 and PGD2



Trace 1: VDDQ, 1V/div.
Trace 2: VTT, 0.5V/div.
Trace 3: PGD1, 5V/div.
Trace 4: PGD2, 5V/div
Timebase: 2ms/div.

Please refer to Figure 4 on Page 17 for test schematic

Outline Drawing - TSSOP-28



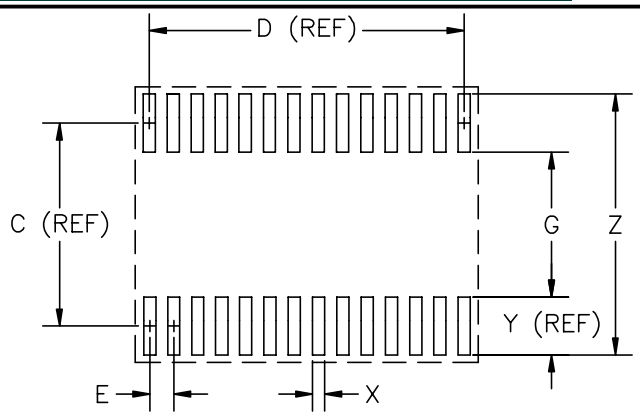
DIMENSIONS [1]					
DIM	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	.3779	.3858	9.60	9.80	[2]
B	.169	.177	4.30	4.50	[2]
C	.252 BSC		6.40 BSC		—
D	.026 BSC		.65 BSC		—
E	.007	.012	.19	.30	—
F	.0020	.0060	.05	.15	—
G		.047		1.20	—
J	.0035	.0079	.09	.20	—
K	0°	8°	0°	8°	—
L	.018	.030	.45	.75	—

JEDEC MO-153AE

[2] DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSIONS.

[1] CONTROLLING DIMENSIONS: MILLIMETERS.

Land Pattern - TSSOP-28



DIMENSIONS [1]					
DIM	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
C	—	.218	—	5.53	REF
D	—	.333	—	8.45	REF
E	—	.026	—	0.65	BSC
G	.155	—	3.947	—	—
X	—	.013	—	0.323	—
Y	—	.062	—	1.583	REF
Z	—	.280	—	7.113	—

[2] GRID PLACEMENT COURTYARD IS 18 X 15 ELEMENTS (9mm X 7.5mm) IN ACCORDANCE WITH THE INTERNATIONAL GRID DETAILED IN THE IEC PUBLICATION 97.

[1] CONTROLLING DIMENSIONS: MILLIMETERS.

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