

**POWER MANAGEMENT****Description**

The SC1214 is a high speed, Combi-Sense™, two-phase driver designed to drive high-side and low-side MOSFETs in two synchronous Buck converters. The driver combined with Combi-Sense PWM controllers, such as Semtech SC2643VX or SC2643, provides a cost effective two-phase voltage regulator for advanced micro-processors

The Combi-Sense™ is a technique to sense the inductor current for peak current mode control of voltage regulator without using sensing resistor. It provides the following advantages:

- No costly precision sensing resistor
- Lossless current sensing
- High level noise free signal
- Fast response
- Suitable for wide range of duty cycle

The detailed explanation of the technique can be found in the Applications Information section.

A 30ns max propagation delay from input transition to the gate of the power FET's guarantees operation at high switching frequencies. Internal overlap protection circuit prevents shoot-through from Vin to PGND in the main and synchronous MOSFETs. The adaptive overlap protection circuit ensures the bottom FET does not turn on until the top FET source has reached 1V, to prevent cross-conduction.

High current drive capability allows fast switching, thus reducing switching losses at high (up to 1.5MHz) frequencies without causing thermal stress on the driver.

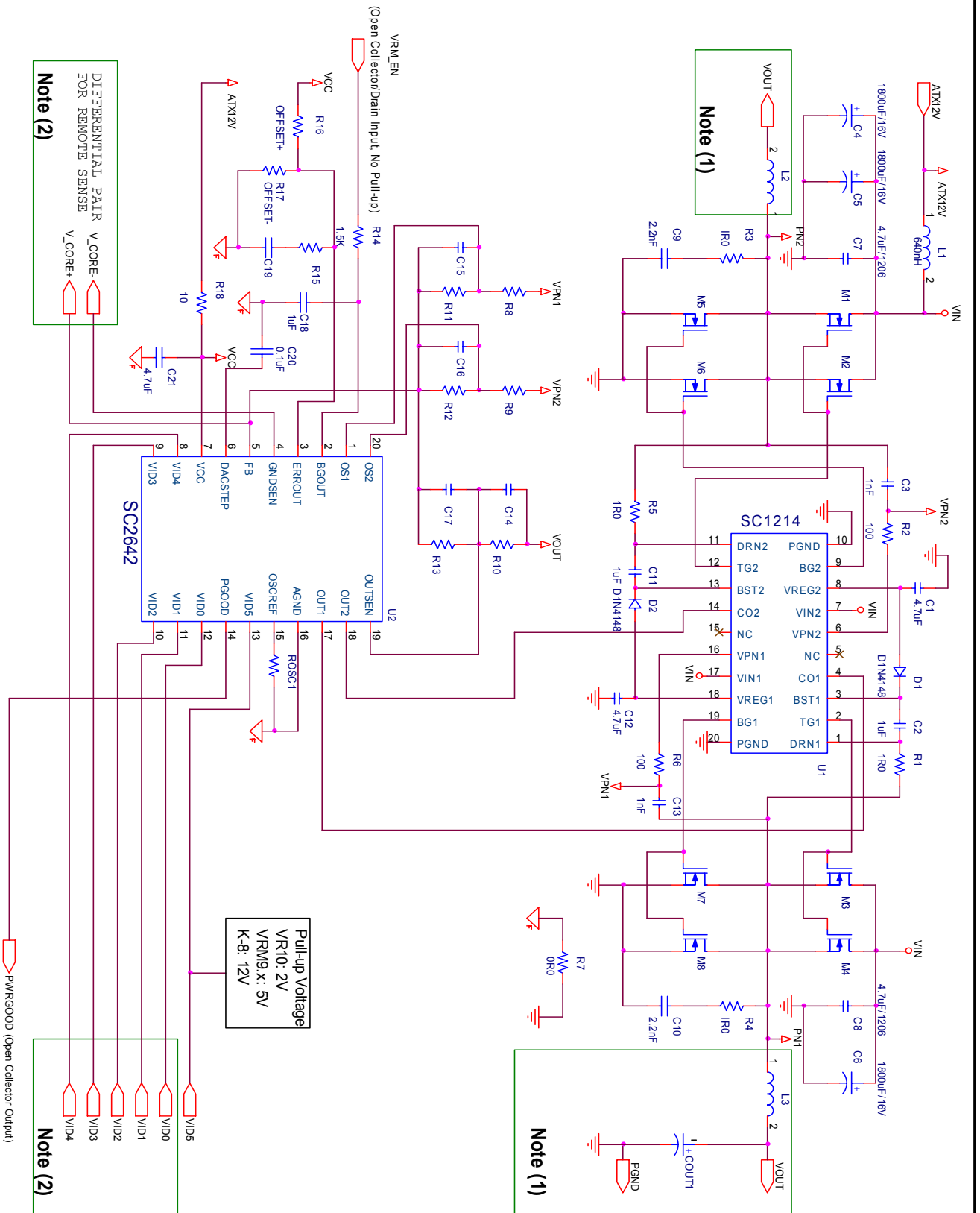
Under-voltage-lockout and over-temperature shutdown features are included for proper and safe operation. Timed latches and improved robustness are built into the housekeeping functions such as the Under Voltage Lockout and adaptive Shoot-through protection circuitry to prevent false triggering and to assure safe operation. The SC1214 is offered in a TSSOP-20 package.

**Features**

- ◆ High efficiency
- ◆ +12V gate drive voltage
- ◆ High peak drive current
- ◆ Adaptive non-overlapping gate drives provide shoot-through protection
- ◆ Support Combi-Sense™ and VID-on-fly operations
- ◆ Fast rise and fall times (15ns typical with 3000pf load)
- ◆ Ultra-low (<30ns) propagation delay (BG going low)
- ◆ Floating top gate drive
- ◆ Crowbar function for over voltage protection
- ◆ High frequency (to 1.5 MHz) operation allows use of small inductors and low cost ceramic capacitors
- ◆ Under-voltage-lockout
- ◆ Low quiescent current

**Applications**

- ◆ Intel Pentium® processor power supplies
- ◆ AMD Athlon™ and AMD-K8™ processor power supplies
- ◆ High current low voltage DC-DC converters

**POWER MANAGEMENT**[www.DataSheet4U.com](http://www.DataSheet4U.com)**Typical Application Circuit**

- Notes:
- (1) Output filter design: Please follow guidelines issued by Intel and AMD.
  - (2) Please follow the guidelines issued by Intel and AMD.

**Note (2)**

DIFFERENTIAL PAIR FOR REMOTE SENSE

V\_CORE+  
V\_CORE-  
V\_CORE+

**Note (2)**

VID5  
VID0  
VID1  
VID2  
VID3  
VID4

**Note (1)**

PGND  
L1  
COUT1  
VOUT

**Pull-up Voltage**

VR10: 2V  
VRM9: 5V  
K-8: 12V

**POWER MANAGEMENT**
**Absolute Maximum Ratings**

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

Parameter	Symbol	Conditions	Maximum	Units
V <sub>IN</sub> Supply Voltage	V <sub>IN</sub>		16	V
BST, TG to DRN	V <sub>BST-DRN</sub> , V <sub>TG-DRN</sub>		11	V
BST to PGND	V <sub>BST-PGND</sub>		40	V
BST to PGND Pulse	V <sub>BST-PULSE</sub>	t <sub>PULSE</sub> < 100ns	45	V
DRN to PGND	V <sub>DRN-PGND</sub>		-2 to 30	V
DRN to PGND Pulse	V <sub>DRN-PULSE</sub>	t <sub>PULSE</sub> < 200ns	-5 to 35	V
BG to PGND	V <sub>BG-PGND</sub>		11	V
VREG to PGND	V <sub>REG-PGND</sub>		11	V
VPN to PGND	V <sub>PN</sub>		16	V
VPN to PGND Pulse	V <sub>PN-PULSE</sub>	t <sub>PULSE</sub> < 100ns	20	V
PWM Input	CO		-0.3 to 8.5	V
Continuous Power Dissipation	P <sub>D</sub>	T <sub>A</sub> = 25°C, T <sub>J</sub> = 125°C	1.76	W
Thermal Resistance Junction to Case			17	°C/W
Operating Junction Temperature Range	T <sub>J</sub>		0 to +150	°C
Storage Temperature Range	T <sub>STG</sub>		-65 to +150	°C
Lead Temperature (Soldering) 10 Sec.	T <sub>LEAD</sub>		300	°C

NOTE:

(1) This device is ESD sensitive. Use of standard ESD handling precautions is required.

**Electrical Characteristics**

Unless specified: T<sub>A</sub> = 25°C; V<sub>IN</sub> = 12V; V<sub>REG</sub> = 8.5V

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Power Supply</b>						
Supply Voltage	V <sub>IN</sub>		9	12	15	V
Quiescent Current, Operating	I <sub>q_op</sub>			3.0		mA
<b>Under Voltage Lockout</b>						
Start Threshold of V <sub>REG</sub> Voltage	V <sub>REG_START</sub>			4	4.3	V
Hysteresis	V <sub>hys_UVLO</sub>			160		mV
<b>Internal LDO</b>						
LDO Output	V <sub>REG</sub>	V <sub>IN</sub> = 9V to 15V		8.5		V
Drop Out Voltage	V <sub>DROP</sub>	V <sub>IN</sub> = 5V to 8.8V		0.3		V

**POWER MANAGEMENT**
**Electrical Characteristics (Cont.)**

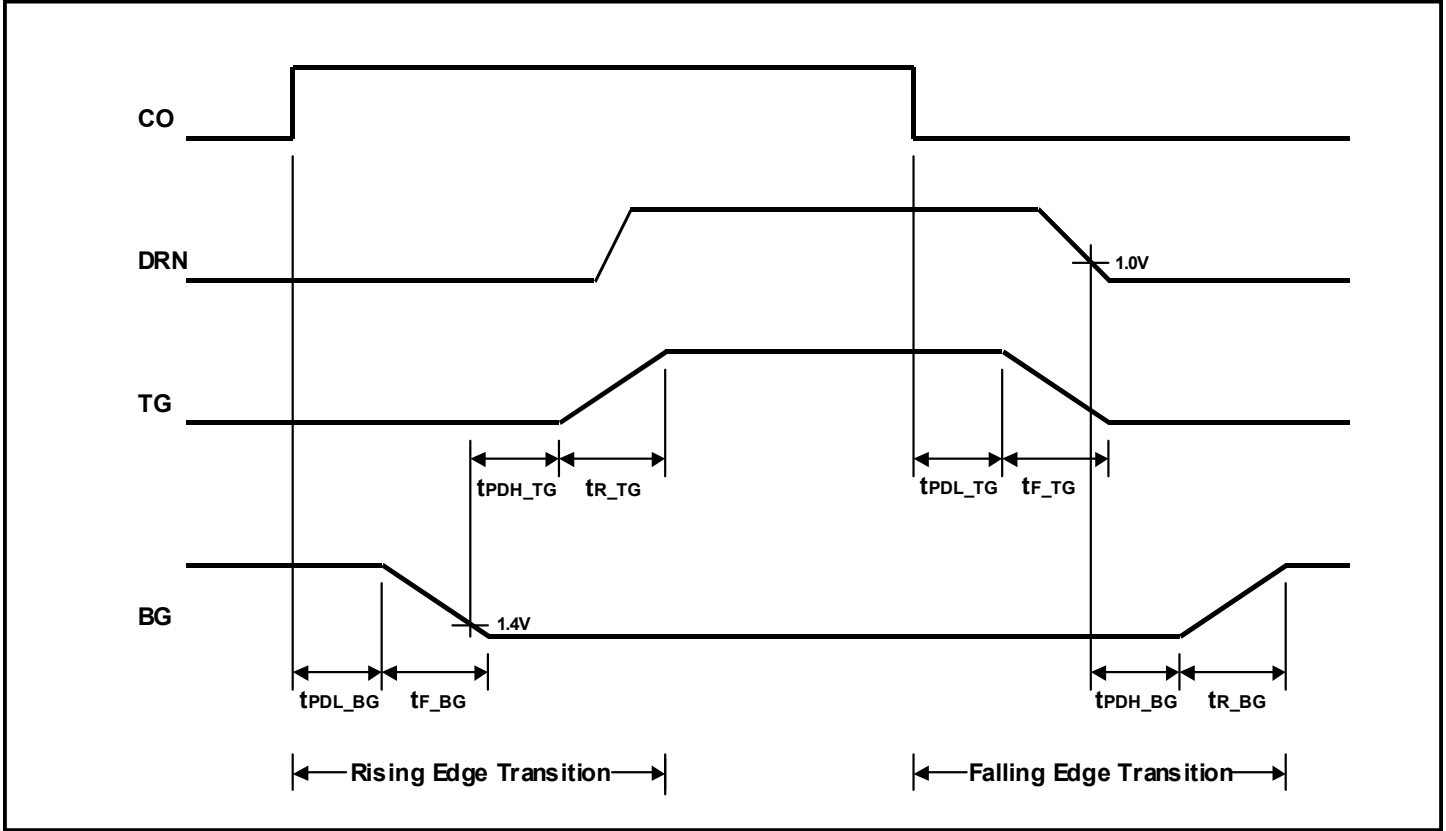
 Unless specified:  $T_A = 25^\circ\text{C}$ ;  $V_{IN} = 12\text{V}$ ;  $V_{REG} = 8.5\text{V}$ 

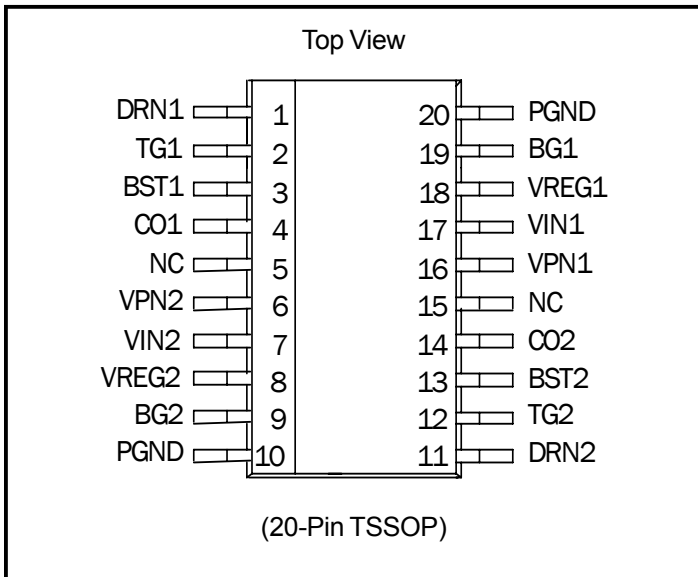
Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>CO1, CO2</b>						
Logic High Input Voltage	$V_{CO\_H}$		2.0			V
Logic Low Input Voltage	$V_{CO\_L}$				0.8	V
<b>Thermal Shutdown</b>						
Over Temperature Trip Point	$T_{OTP}$			155		$^\circ\text{C}$
Hysteresis	$T_{HYST}$			10		$^\circ\text{C}$
<b>High Side Driver (TG1, TG2)</b>						
Output Impedance	$R_{SRC\_TG}$	$V_{BST} - V_{DRN} = 8.5\text{V}$		1.5	3.0	Ohm
	$R_{SINK\_TG}$			1.0	2.0	
Rise Time	$t_{R\_TG}$	$CL = 3.3\text{nF}, V_{BST} - V_{DRN} = 8.5\text{V}$		15		ns
Fall Time	$t_{F\_TG}$	$CL = 3.3\text{nF}, V_{BST} - V_{DRN} = 8.5\text{V}$		10		ns
Propagation Delay, TG Going High	$t_{PDH\_TG}$	$V_{BST} - V_{DRN} = 8.5\text{V}$		37		ns
Propagation Delay, TG Going Low	$t_{PDL\_TG}$	$V_{BST} - V_{DRN} = 8.5\text{V}$		30		ns
<b>Low-Side Driver (BG1, BG2)</b>						
Output Impedance	$R_{SRC\_BG}$	$V_{REG} = 8.5\text{V}$		1.5	3.0	Ohm
	$R_{SINK\_BG}$			1.5	3.0	
Rise Time	$t_{R\_BG}$	$CL = 3.3\text{nF}, V_{REG} = 8.5\text{V}$		10		ns
Fall Time	$t_{F\_BG}$	$CL = 3.3\text{nF}, V_{REG} = 8.5\text{V}$		10		ns
Propagation Delay, BG Going High	$t_{PDH\_BG}$	$V_{REG} = 8.5\text{V}$		20		ns
Propagation Delay, BG Going Low	$t_{PDL\_BG}$	$V_{REG} = 8.5\text{V}$		27		ns
BG1, BG2 Minimum Off-time <sup>(1)</sup>	$t_{OFF\_BG}$			75		ns
<b>Under-Voltage-Lockout Time Delay</b>						
$V_{REG}$ ramping up	$t_{PDH\_UVLO}$			2		$\mu\text{s}$
$V_{REG}$ ramping down	$t_{PDL\_UVLO}$			2		$\mu\text{s}$

NOTE:

(1) Guaranteed by design.

**Timing Diagrams**



**POWER MANAGEMENT**
**Pin Configurations**

**Ordering Information**

Device	Package	Temp. Range( T <sub>j</sub> )
SC1214TSTR <sup>(1)</sup>	TSSOP-20	0 - 125°C
SC1214TSTRT <sup>(1)(2)</sup>	TSSOP-20	0 - 125°C

**Note:**

(1) Only available in tape and reel packaging. A reel contains 2500 devices.

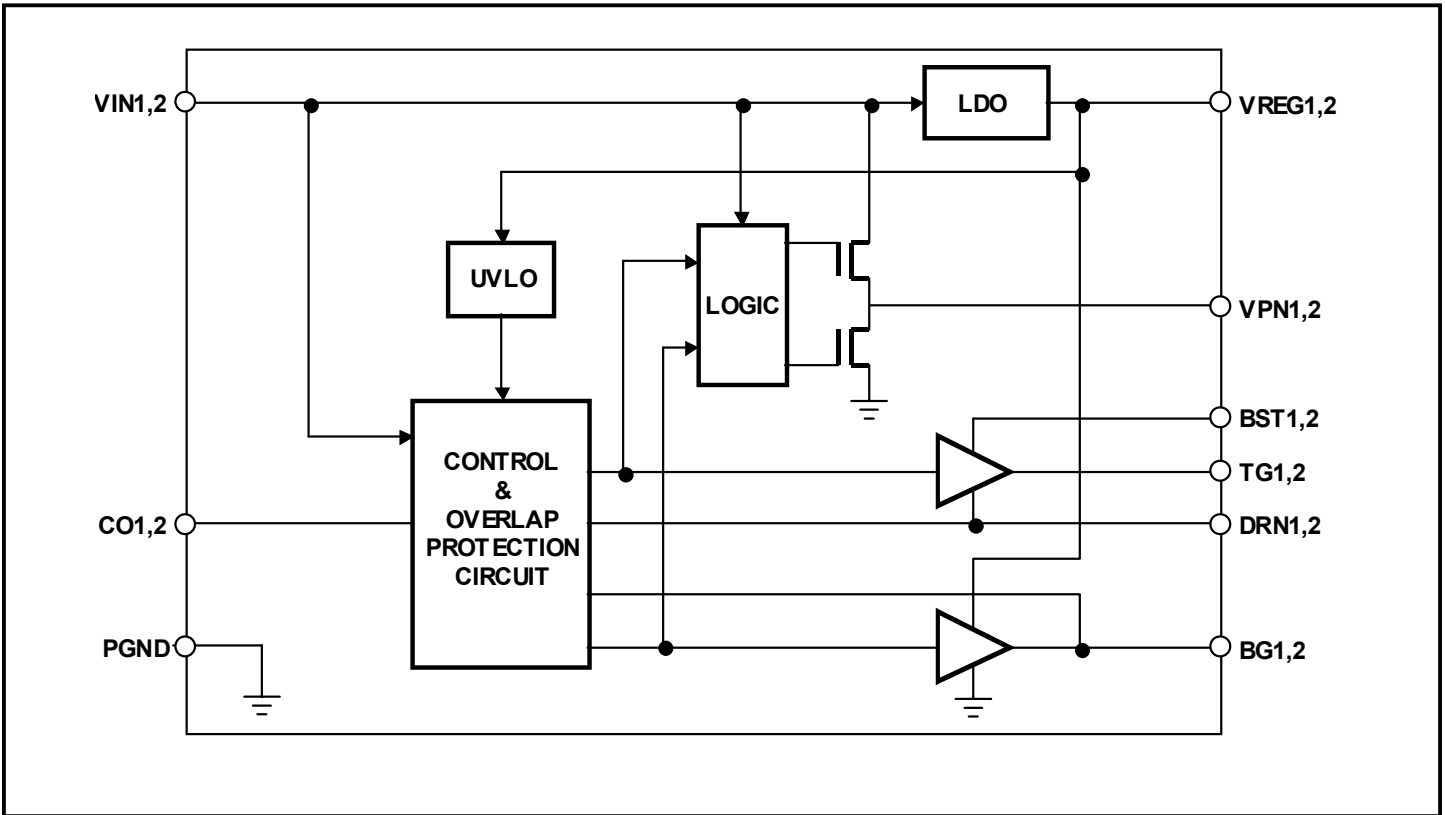
(2) Lead free product. This product is fully WEEE and RoHS compliant.

**Pin Descriptions**

Pin#	Pin Name	Pin Function
2,12	TG1, TG2	Output gate drive for the switching (top) MOSFET.
1,11	DRN1, DRN2	The power phase node (or switching node) of the synchronous buck converter. This pin can be subjected to a negative spike up to -VREG relative to PGND without affecting operation.
3, 13	BST1, BST2	Bootstrap pin. A capacitor is connected between BST and DRN pins to develop the floating bootstrap voltage for the high-side MOSFET. The capacitor value is typically 1μF (ceramic).
18,8	VREG1,VREG2	LDO output. Decouple with 1μF to 4.7μF (ceramic) with lead length no more than 0.2" (5mm).
4,14	CO1, CO2	Logic level PWM input signal to the SC1214 supplied by external controller. An internal 50kohm resistor is connected from this pin to PGND.
16,6	VPN1, VPN2	Virtual Phase Node. Connect an RC between this pin and the output sense point to Enable Combi-Sense™ operation. See the Typical Application Circuit.
10, 20	PGND	Ground. Keep these pins close to the synchronous MOSFETs source.
19,9	BG1, BG2	Output gate drive for the synchronous (bottom) MOSFET.
17,7	VIN1,VIN2	Supply power for low gate drive, LDO and the internal Combi-Sense™ circuitry. Connect to input power rail of the converter.

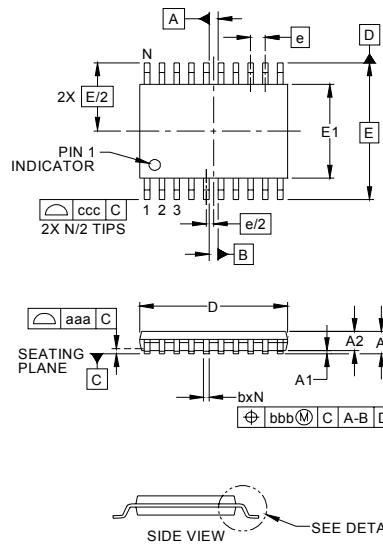
**POWER MANAGEMENT**

**Block Diagram**



POWER MANAGEMENT

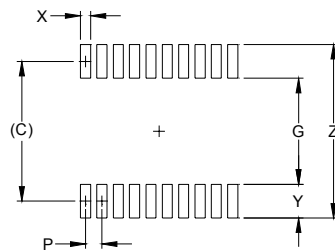
Outline Drawing - TSSOP-20



DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	.047	-	-	1.20
A1	.002	-	.006	0.05	-	0.15
A2	.031	-	.042	0.80	-	1.05
b	.007	-	.012	0.19	-	0.30
c	.003	-	.007	0.09	-	0.20
D	.251	.255	.259	6.40	6.50	6.60
E1	.169	.173	.177	4.30	4.40	4.50
E	.252 BSC			6.40 BSC		
e	.026 BSC			0.65 BSC		
L	.018	.024	.030	0.45	0.60	0.75
L1	(.039)			(1.0)		
N	20			20		
g1	0°	-	8°	0°	-	8°
aaa	.004			0.10		
bbb	.004			0.10		
ccc	.008			0.20		

- NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
  2. DATUMS **-A-** AND **-B-** TO BE DETERMINED AT DATUM PLANE **-H-**
  3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
  4. REFERENCE JEDEC STD MO-153, VARIATION AC.

Land Pattern - TSSOP-20



DIM	DIMENSIONS	
	INCHES	MILLIMETERS
C	(.222)	(5.65)
G	.161	4.10
P	.026	0.65
X	.016	0.40
Y	.061	1.55
Z	.283	7.20

- NOTES:
1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

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