

Description

The μ PD41257 is a 262,144-word by 1-bit dynamic NMOS RAM designed to operate from a single +5-volt power supply. A double-polylayer N-channel silicon gate fabrication process provides for high storage cell density, high performance, and high reliability. The device also uses a single-transistor dynamic storage cell and advanced dynamic circuitry, including 1024 sense amplifiers, which ensure that power dissipation is minimized. The negative voltage substrate bias is automatically generated internally.

The three-state output is controlled by $\overline{\text{CAS}}$ independent of $\overline{\text{RAS}}$. Nibble mode read or write cycles are available by cycling $\overline{\text{CAS}}$.

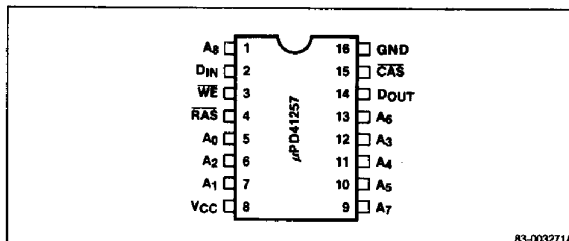
Refreshing is initiated by a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ cycle that enables internal generation of the refresh address. Refreshing is also accomplished by means of $\overline{\text{RAS}}$ -only refresh cycles, hidden refresh cycles, or by normal read or write cycles on the 256 address combinations of A_0 - A_7 during a 4-ms period.

Features

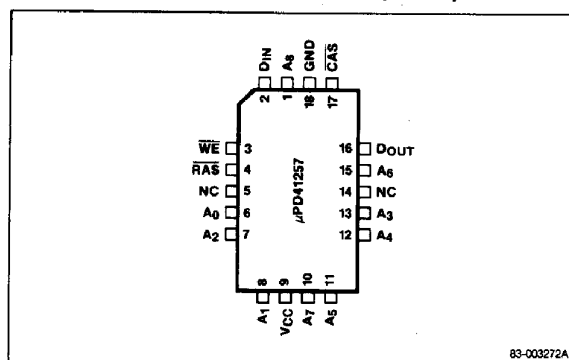
- 262,144-word x 1-bit organization
- Multiplexed address inputs
- Single +5-volt $\pm 10\%$ power supply
- Nibble read, write, or read-modify-write cycles
- $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ internal refreshing
- Low power dissipation
 - 28 mW max (standby)
 - 413 mW max (active, $t_{RC} = 220$ ns)
- Nonlatched, three-state output
- TTL-compatible inputs with low input capacitance
- 256-cycle/4-ms refresh period (A_0 - A_7 are refresh addresses)
- High-density plastic DIP and PLCC packaging

Pin Configurations

16-Pin Plastic DIP

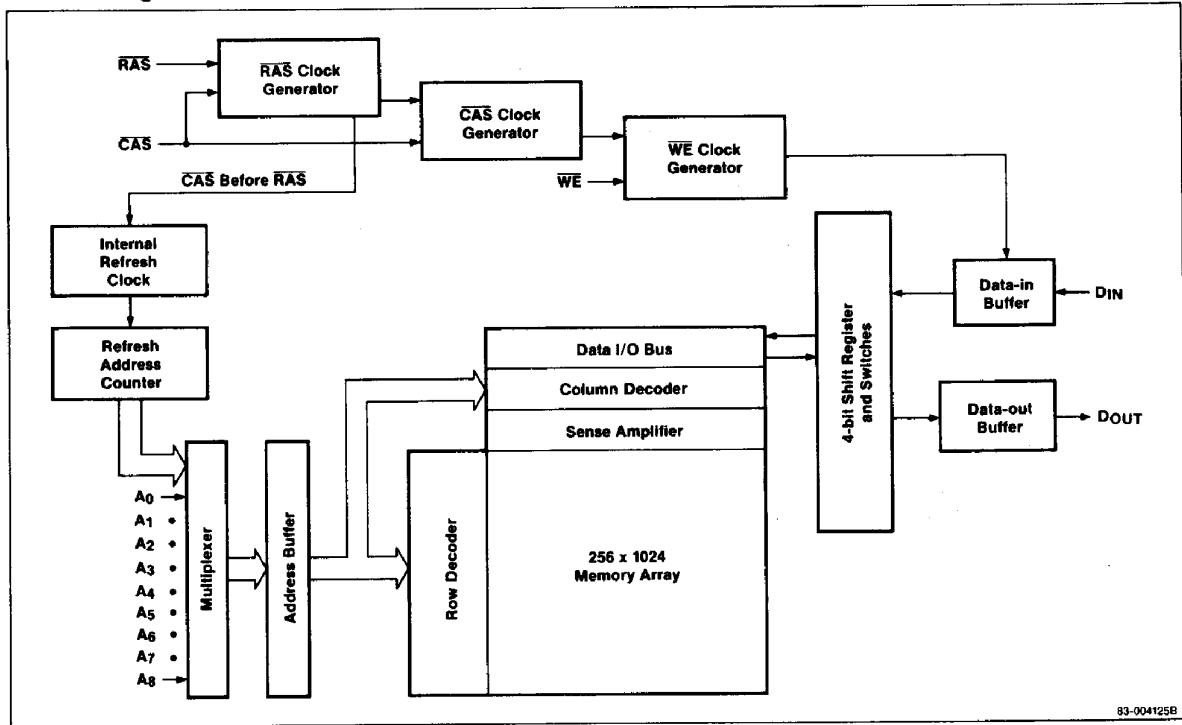


18-Pin Plastic Leaded Chip Carrier (PLCC)



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Block Diagram



Pin Identification

Symbol	Function
A ₀ -A ₈	Address inputs
D _{IN}	Data input
D _{OUT}	Data output
WE	Write enable
RAS	Row address strobe
CAS	Column address strobe
GND	Ground
V _{CC}	+5.0-volt power supply

Capacitance

T_A = 0 to +70 °C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Limits			Unit	Test Conditions
		Min	Typ	Max		
Input capacitance	C _{I1}			5	pF	A ₀ -A ₈ , D _{IN}
	C _{I2}			8		
Output capacitance	C _O			7	pF	D _{OUT}

Absolute Maximum Ratings

Voltage on any pin relative to GND	-1.0 to +7.0 V
Short-circuit output current	50 mA
Power dissipation, P _D	1 W
Operating temperature, T _A	0 to +70 °C
Storage temperature, T _{STG}	-55 to +150 °C

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Ordering Information

Part Number	Access Time (max)	R/W Cycle (min)	Package
μPD41257C-12	120 ns	220 ns	16-pin plastic DIP
C-15	150 ns	260 ns	
C-20	200 ns	330 ns	
μPD41257L-12	120 ns	220 ns	18-pin PLCC
L-15	150 ns	260 ns	
L-20	200 ns	330 ns	

DC Characteristics

T_A = 0 to +70°C; V_{CC} = 5.0 V ±10%; GND = 0 V

Parameter	Symbol	Limits			Unit	Test Conditions
		Min	Typ	Max		
Standby power supply current	I _{CC2}			5	mA	$\overline{\text{RAS}} = V_{IH}$; D _{OUT} = high impedance
Input leakage current	I _{I(L)}	-10		10	μA	Any input V _{IN} = 0 V to V _{CC} ; all other pins not under test = 0 V
Output leakage current	I _{O(L)}	-10		10	μA	D _{OUT} disabled; V _{OUT} = 0 to 5.5 V
Output voltage, high	V _{OH}	2.4		V _{CC}	V	I _O = -5 mA
Output voltage, low	V _{OL}	0		0.4	V	I _O = 4.2 mA
Supply voltage	V _{CC}	4.5	5.0	5.5	V	
	GND	0	0	0	V	
Input voltage, high	V _{IH}	2.4		5.5	V	All inputs
Input voltage, low	V _{IL}	-1.0		0.8	V	All inputs

AC Characteristics

T_A = 0 to +70°C; V_{CC} = 5.0 V ±10%

Parameter	Symbol	Limits						Unit	Test Conditions
		μPD41257-12		μPD41257-15		μPD41257-20			
		Min	Max	Min	Max	Min	Max		
Standard Operation									
Average power supply operating current	I _{CC1}		75		70		60	mA	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$ cycling; t _{RC} = t _{RC min} (Note 5)
Average power supply current, refresh cycle	I _{CC3}		60		55		55	mA	$\overline{\text{RAS}}$ cycling; $\overline{\text{CAS}} = V_{IH}$; t _{RC} = t _{RC min} (Note 5)
Random read or write cycle time	t _{RC}	220		260		330		ns	(Note 6)
Read-write cycle time	t _{RWC}	265		310		390		ns	(Note 6)
Access time from $\overline{\text{RAS}}$	t _{RAC}		120		150		200	ns	(Notes 7, 8)
Access time from $\overline{\text{CAS}}$	t _{CAC}		60		75		100	ns	(Notes 7, 9)
Output buffer turnoff delay	t _{OFF}	0	30	0	40	0	50	ns	(Note 10)
Rise and fall transition time	t _T	3	50	3	50	3	50	ns	(Note 4)
$\overline{\text{RAS}}$ precharge time	t _{RP}	90		100		120		ns	
$\overline{\text{RAS}}$ pulse width	t _{RAS}	120	10,000	150	10,000	200	10,000	ns	
$\overline{\text{RAS}}$ hold time	t _{RSH}	60		75		100		ns	
$\overline{\text{CAS}}$ pulse width	t _{CAS}	60	10,000	75	10,000	100	10,000	ns	
$\overline{\text{CAS}}$ hold time	t _{CSH}	120		150		200		ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	t _{RCD}	25	60	25	75	35	100	ns	(Note 11)
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	t _{CRP}	10		10		10		ns	(Note 12)
$\overline{\text{CAS}}$ precharge time	t _{CPN}	30		30		35		ns	
$\overline{\text{RAS}}$ precharge $\overline{\text{CAS}}$ hold time	t _{RPC}	0		0		0		ns	
Row address setup time	t _{ASR}	0		0		0		ns	

AC Characteristics (cont)

Parameter	Symbol	μPD41257-12		μPD41257-15		μPD41257-20		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
Standard Operation (cont)									
Row address hold time	t _{RAH}	15		15		25		ns	
Column address setup time	t _{ASC}	0		0		0		ns	
Column address hold time	t _{CAH}	20		25		55		ns	
Column address hold time referenced to RAS	t _{AR}	80		100		155		ns	
Read command setup time	t _{RCS}	0		0		0		ns	
Read command hold time referenced to RAS	t _{RRH}	10		10		25		ns	(Note 13)
Read command hold time referenced to CAS	t _{RCH}	0		0		0		ns	(Note 13)
Write command hold time	t _{WCH}	30		40		55		ns	
Write command hold time referenced to RAS	t _{WCR}	90		115		155		ns	
Write command pulse width	t _{WP}	20		25		55		ns	
Write command to RAS lead time	t _{RWL}	40		45		55		ns	
Write command to CAS lead time	t _{CWL}	40		45		55		ns	
Data-in setup time	t _{DS}	0		0		0		ns	(Note 14)
Data-in hold time	t _{DH}	30		40		55		ns	(Note 14)
Data-in hold time referenced to RAS	t _{DHR}	90		115		155		ns	
Refresh period	t _{REF}		4		4		4	ms	
WE command setup time	t _{WCS}	0		0		0		ns	(Note 15)
CAS to WE delay	t _{CWD}	60		75		100		ns	(Note 15)
RAS to WE delay	t _{RWD}	120		150		200		ns	(Note 15)
Nibble Mode									
Average power supply current, nibble mode	I _{CC6}		35		27		27	mA	RAS = V _{IL} ; CAS cycling; t _{NC} = t _{NC min} (Note 5)
Nibble-mode cycle time	t _{NC}	60		70		100		ns	(Note 6)
Nibble-mode access time	t _{NAC}		30		35		50	ns	(Note 7)
Nibble-mode precharge time	t _{NP}	20		25		40		ns	
Nibble-mode WE pulse width	t _{NWP}	20		25		40		ns	
Nibble-mode CAS pulse width	t _{NAS}	30		35		50		ns	
Nibble-mode RAS hold time (read cycle)	t _{NRRSH}	30		35		50		ns	
Nibble-mode RAS hold time (write cycle)	t _{NWRSH}	35		35		50		ns	
Nibble-mode CAS to WE delay	t _{NCWD}	30		35		50		ns	
Nibble-mode WE to CAS lead time	t _{NCWL}	30		35		50		ns	

AC Characteristics (cont)

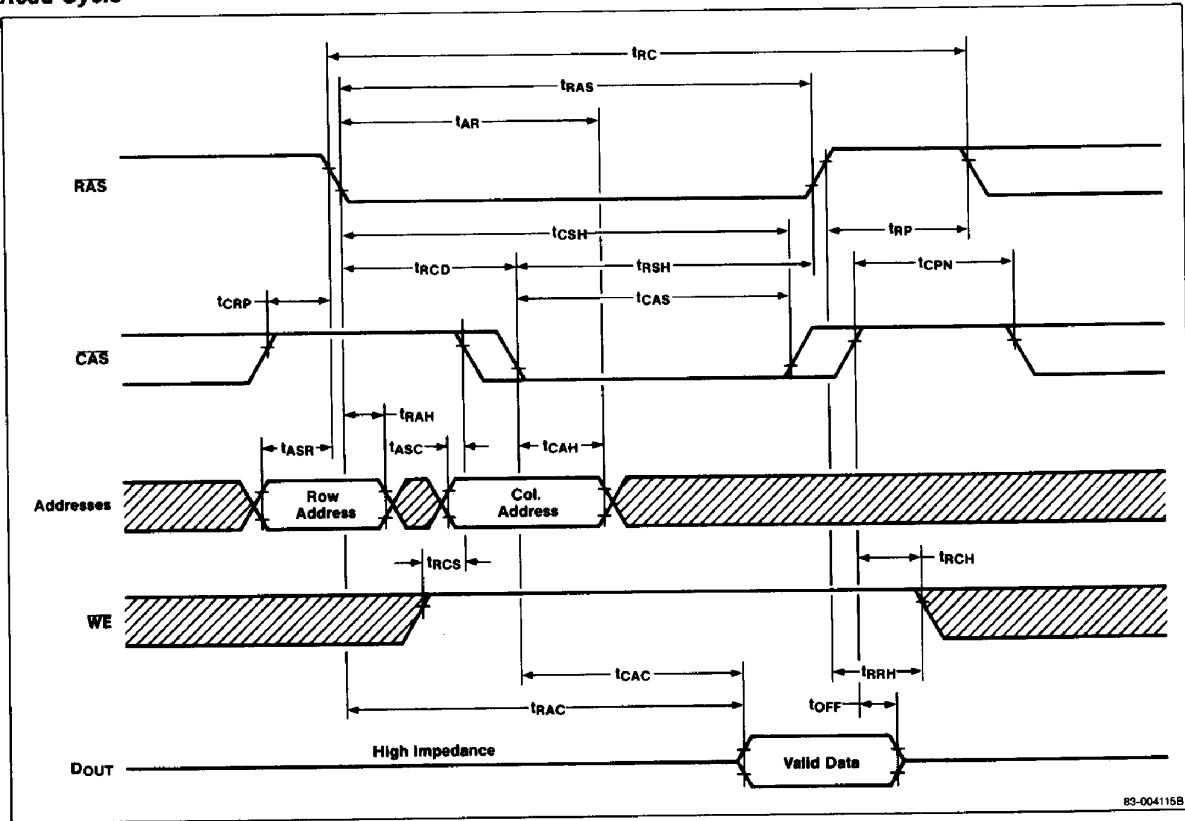
Parameter	Symbol	μPD41257-12		μPD41257-15		μPD41257-20		Unit	Test Conditions
		Min	Max	Min	Max	Min	Max		
CAS Before RAS Refresh Cycle									
Average power supply current, CAS before RAS refreshing	I _{CC4}		65		60		55	mA	RAS cycling; $\overline{\text{CAS}} = V_{\text{IL}}$; $t_{\text{RC}} = t_{\text{RC min}}$ (Note 5)
CAS setup time for CAS before RAS refreshing	t _{CSR}	10		10		10		ns	
CAS hold time for CAS before RAS refreshing	t _{CHR}	25		30		30		ns	
Read or write cycle time (counter test cycle)	t _{TRC}	245		285		350		ns	
Read-write cycle time (counter test cycle)	t _{TRWC}	290		335		410		ns	
CAS precharge time (counter test cycle)	t _{TCP}	50		60		80		ns	

Notes:

- (1) An initial pause of 100 μs is required after power-up, followed by any eight RAS cycles before proper device operation is achieved.
- (2) Ac measurements assume t_T = 5 ns.
- (3) V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
- (4) All voltages are referenced to GND.
- (5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC6} depend on output loading and cycle rates. Specified values are obtained with the output open.
- (6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.
- (7) Load = 2 TTL loads and 100 pF.
- (8) Assumes that t_{RCD} ≤ t_{RCD (max)}. If t_{RCD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} exceeds the value shown. For the $\overline{\text{CAS}}$ before RAS refresh counter test cycle, t_{RAC} is specified as t_{RAC} = t_{CHR} + t_{TCP} + t_{CAC} + 2t_T and is greater than the maximum specified value shown in this table.
- (9) Assumes that t_{RCD} ≥ t_{RCD (max)}.
- (10) t_{OFF (max)} defines the time at which the output achieves the open-circuit condition and is not referenced to V_{OH} or V_{OL}.
- (11) Operation within the t_{RCD (max)} limit assures that t_{RAC (max)} can be met. Time t_{RCD (max)} is specified as a reference point only; if t_{RCD} is greater than t_{RCD (max)}, access time is controlled exclusively by t_{CAC}.
- (12) The t_{CRP} requirement should be applicable for $\overline{\text{RAS}}/\overline{\text{CAS}}$ cycles preceded by any cycle.
- (13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
- (14) These parameters are referenced to the leading edge of $\overline{\text{CAS}}$ for early write cycles and to the leading edge of $\overline{\text{WE}}$ for delayed write or read-modify-write cycles.
- (15) t_{WCS}, t_{CWD}, t_{NCWD}, and t_{RWD} are restrictive operating parameters in read-write/read-modify-write cycles only.
 - If t_{WCS} ≥ t_{WCS (min)}, the cycle is an early write cycle or a nibble mode early write cycle and the data output pin will remain open-circuit throughout the entire cycle.
 - If t_{CWD} ≥ t_{CWD (min)} and t_{RWD} ≥ t_{RWD (min)}, the cycle is a read-write cycle and the data output pin will contain data read from the selected cell.
 - If t_{NCWD} ≥ t_{NCWD (min)}, the cycle is a nibble mode read-write cycle and the data output pin will contain data read from the selected cell.
 - If none of the above conditions is met, the condition of the data output pin (at access time and until $\overline{\text{CAS}}$ returns to V_{IH}) is indeterminate.

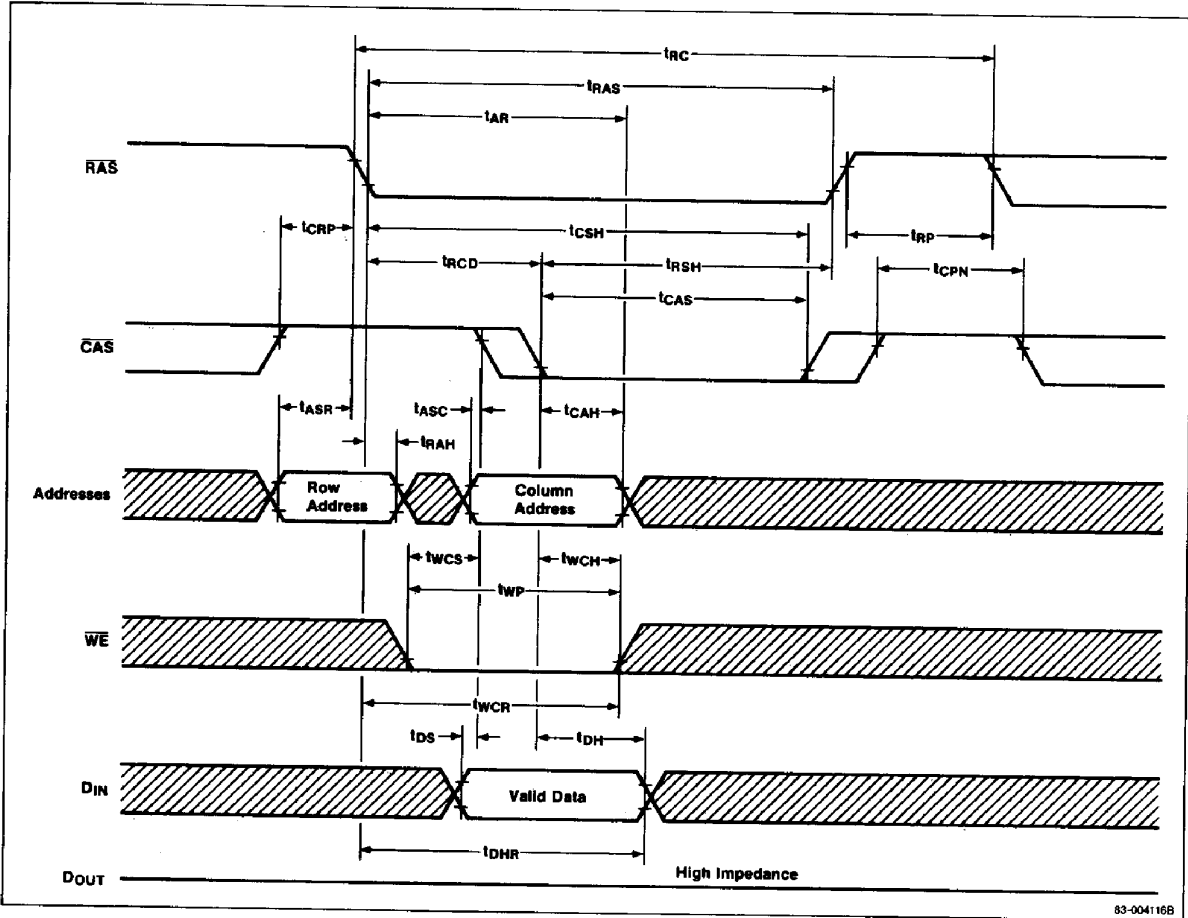
Timing Waveforms

Read Cycle



Timing Waveforms (cont)

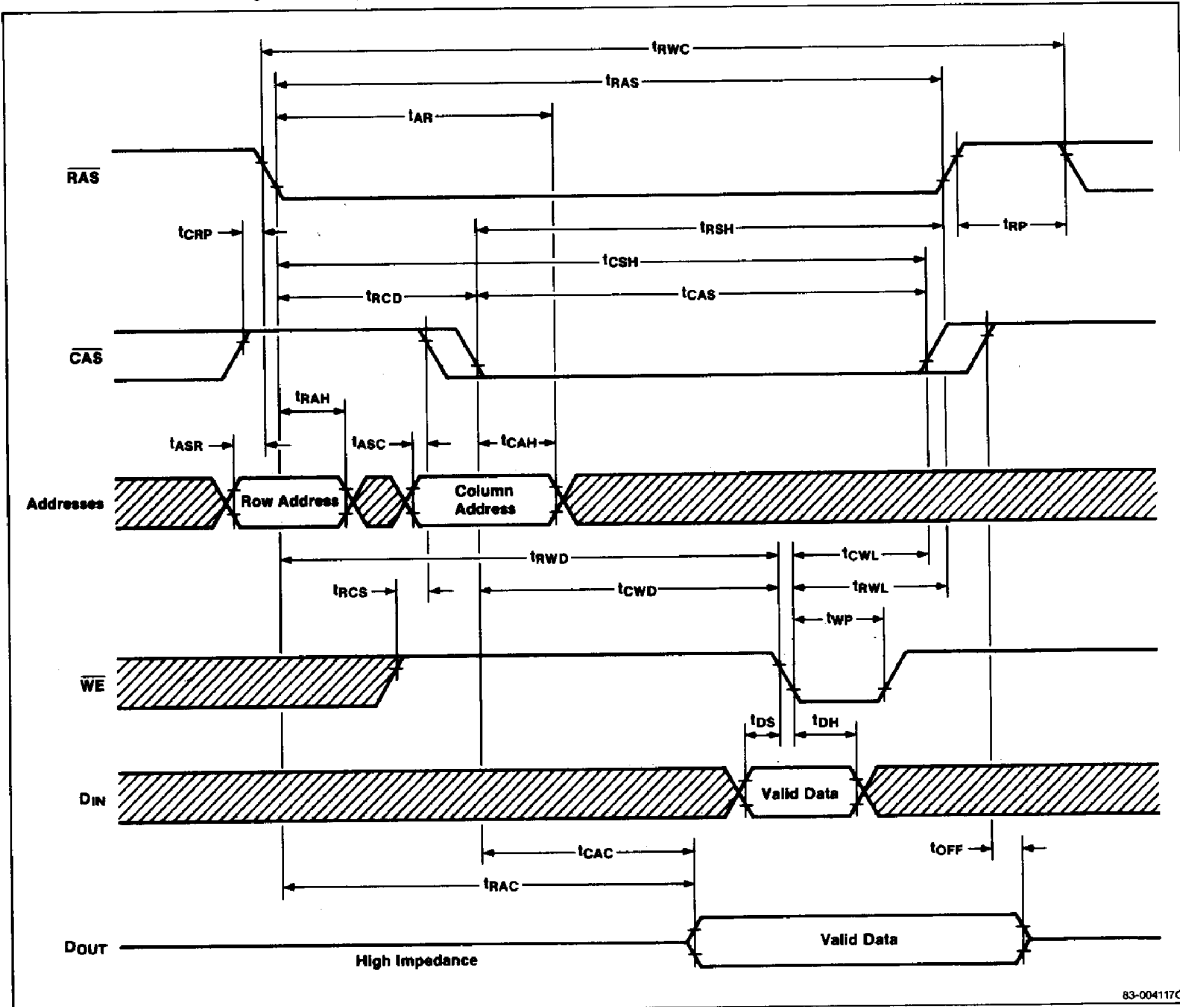
Write Cycle (Early Write)



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Timing Waveforms (cont)

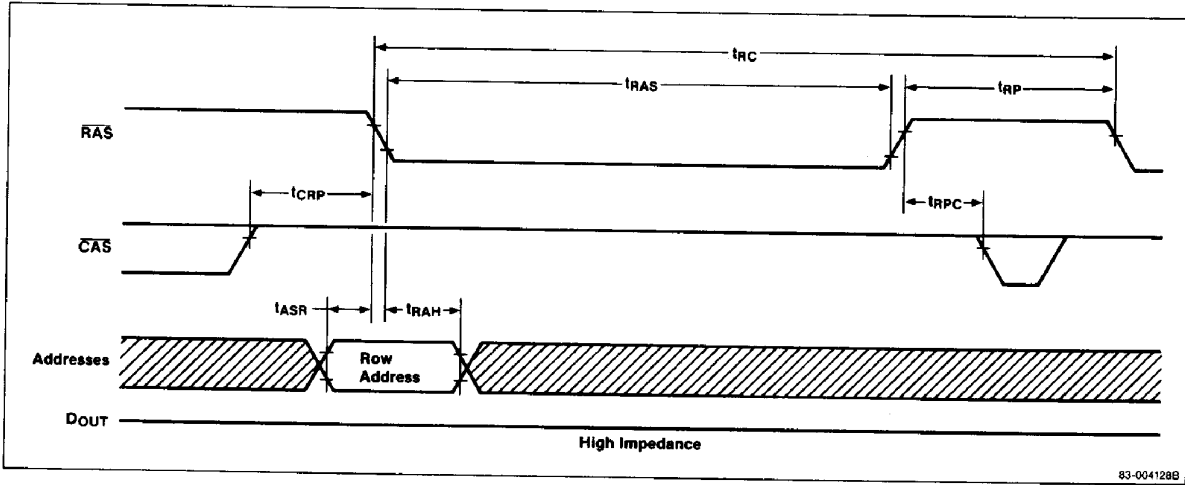
Read-Write/Read-Modify-Write Cycle



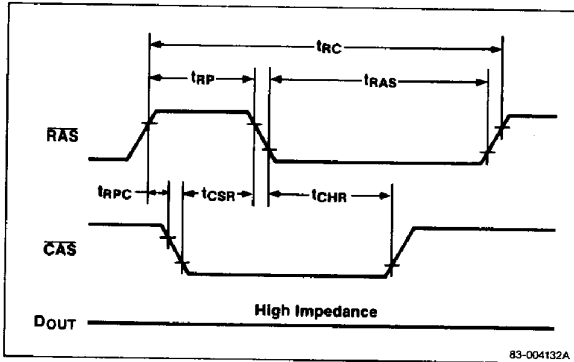
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Timing Waveforms (cont)

RAS-Only Refresh Cycle



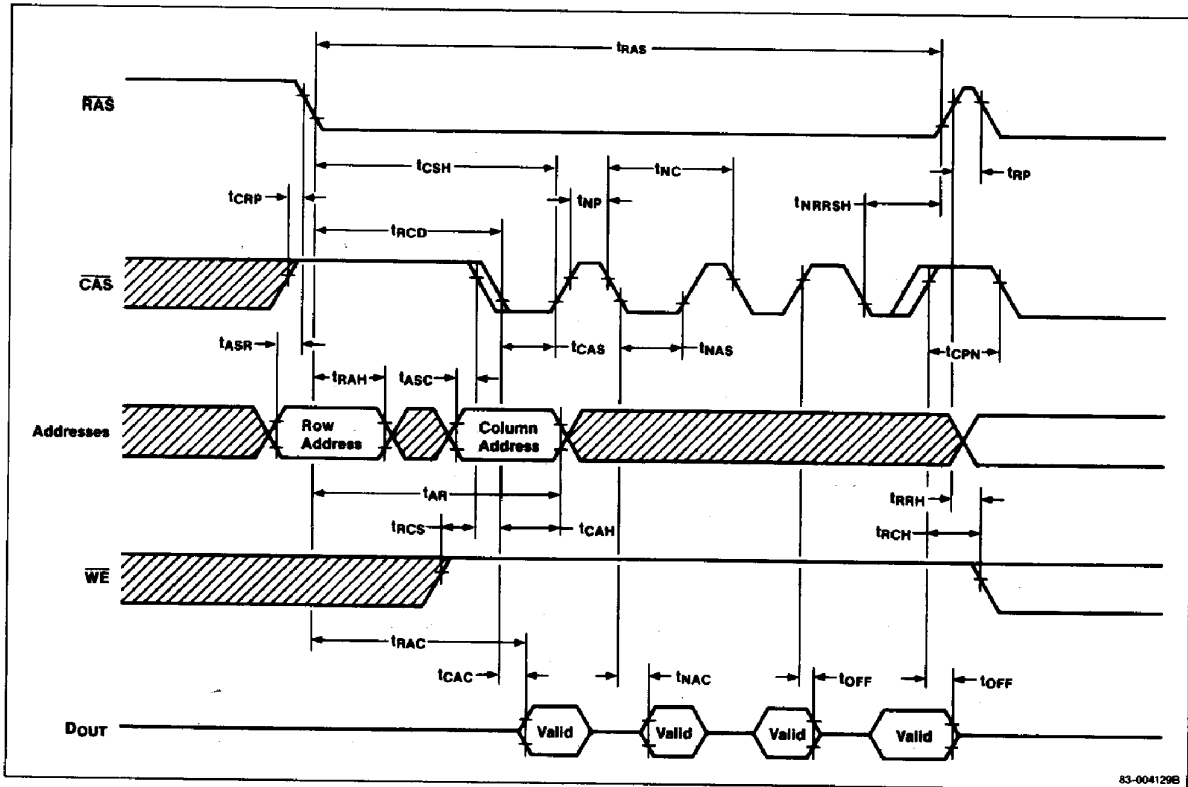
CAS Before RAS Refresh Cycle



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Timing Waveforms (cont)

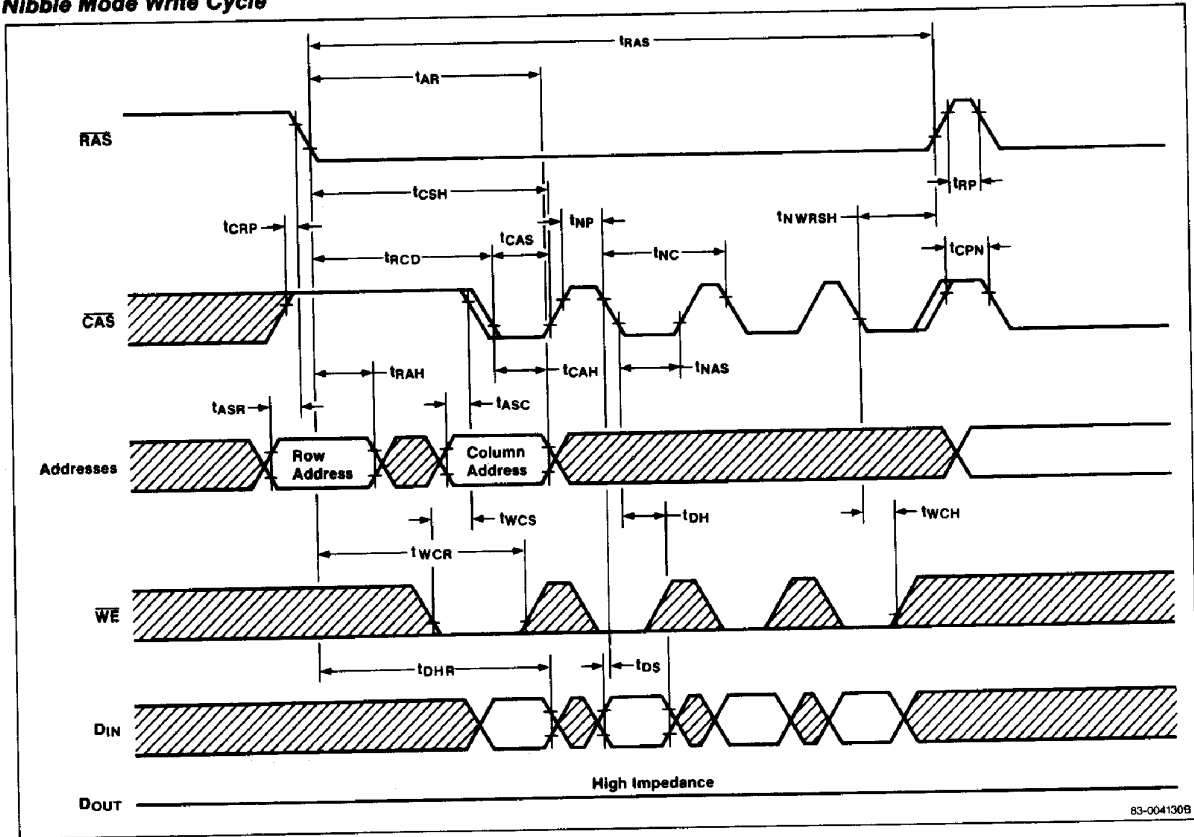
Nibble Mode Read Cycle



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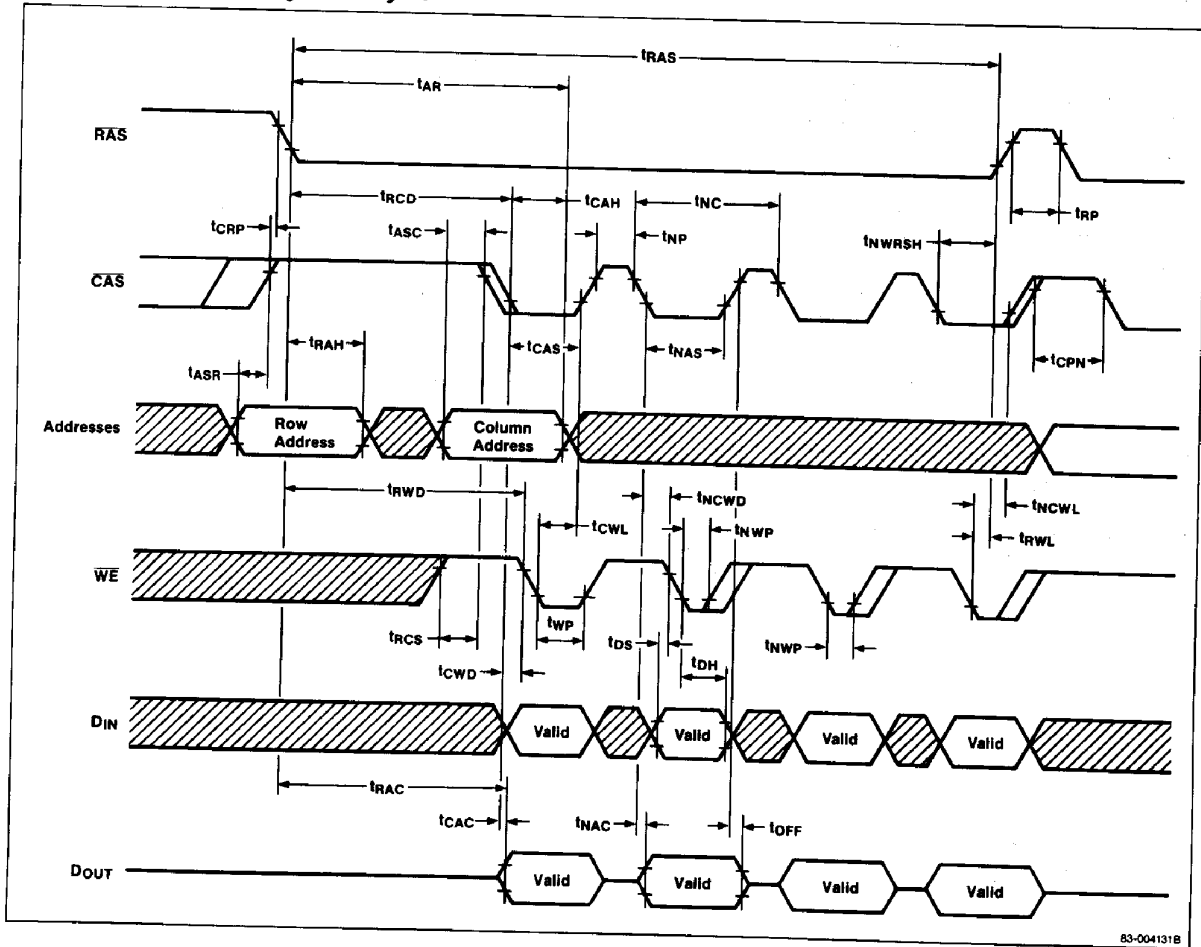
Timing Waveforms (cont)

Nibble Mode Write Cycle



Timing Waveforms (cont)

Nibble Mode Read-Modify-Write Cycle

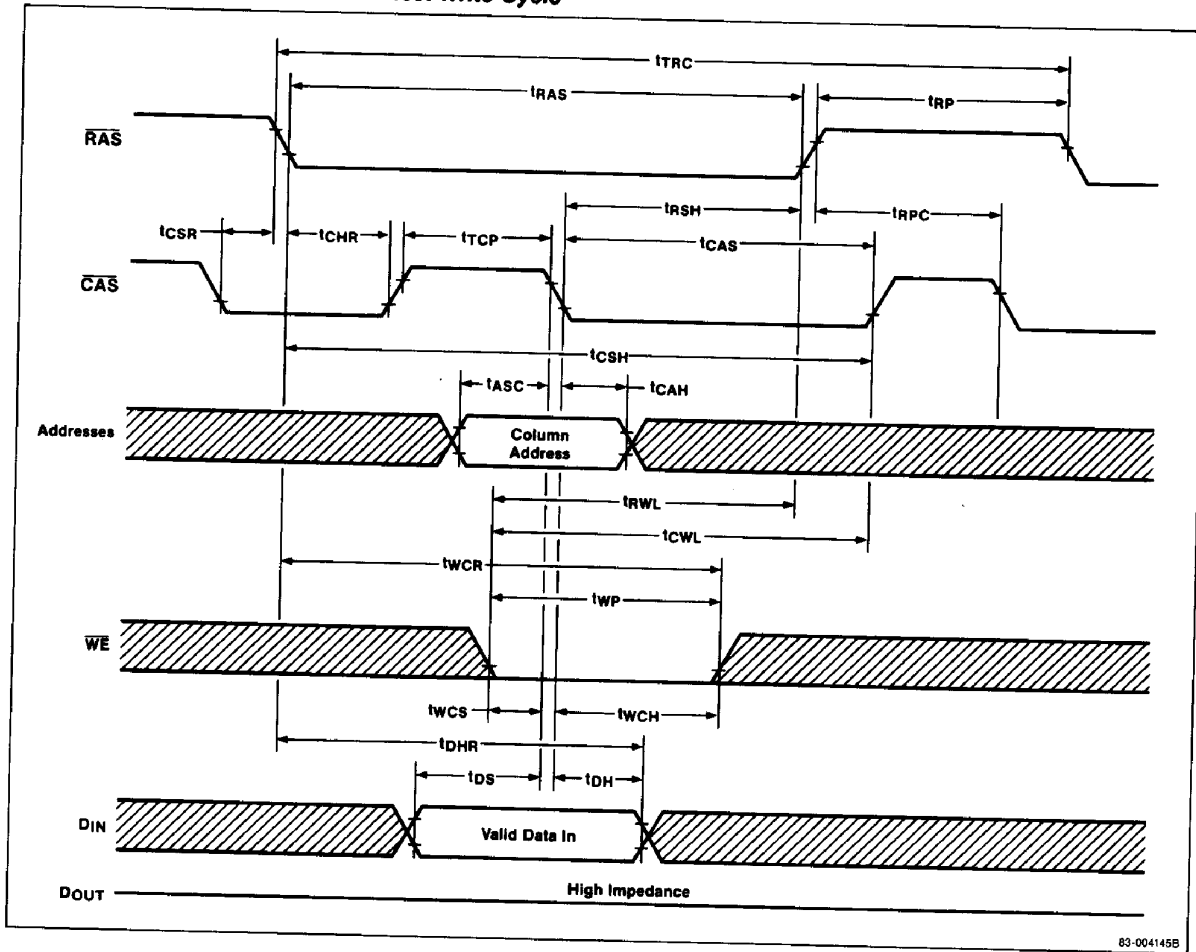


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Timing Waveforms (cont)

CAS Before RAS Refresh Counter Test Write Cycle



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