

Description

The NEC μ PD4168 is an 8,192 word by 8-bit NMOS XRAM designed to operate from a single +5V power supply. The NEC μ PD4168 is termed an XRAM because it incorporates some of the best features of both SRAMs (Non-multiplexed addresses, simple interface requirements) and DRAMs (the one-transistor core cell provides high density at low cost). The negative voltage substrate bias is internally generated and provides automatic and transparent operation.

The incorporation of an internal refresh address counter and refresh multiplexer allows the user to select one of three refresh modes. The self-refresh mode provides transparent refresh without system overhead. Internal latches for address, data, and chip select allow for use in systems incorporating multiplexed address/data buses.

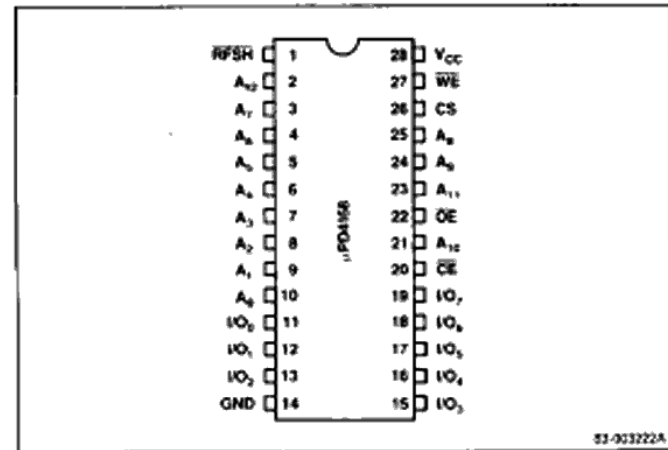
Features

- 8,192 words by 8-bit organization
- Single +5V \pm 10% power supply
- On-chip substrate bias generator
- Fast access times
- Low power dissipation:
28 mW max-Standby
19 mW max-Self refresh
- TTL-compatible
- 28-pin SRAM/ROM/EPROM compatible package
- Built-in refresh multiplexer and refresh address counter
- Power-down self-refresh mode
- Automatic precharge allows cycle time to be independent of system skews
- Latched address, CS, and \overline{OE} functions allow use on multiplexed address/data bus
- Read, early write, late write, external refresh, pulse refresh, and self-refresh cycles

Performance Ranges

| Device | t_{CEA} | t_{OEA} | t_C | I_{CC1} |
|------------------|-----------|-----------|--------|-----------|
| μ PD4168C-12 | 120 ns | 45 ns | 220 ns | 65 mA |
| μ PD4168C-15 | 150 ns | 55 ns | 260 ns | 60 mA |
| μ PD4168C-20 | 200 ns | 70 ns | 330 ns | 55 mA |

Pin Configuration



Pin Identification

| No. | Symbol | Function |
|-----------------|-------------------|------------------|
| 1 | RFSH | Internal refresh |
| 2-10, 21, 23-25 | A_0 - A_{12} | Address inputs |
| 11-13, 15-19 | I/O_0 - I/O_7 | Data in / out |
| 14 | GND | Ground |
| 20 | \overline{CE} | Chip enable |
| 22 | \overline{OE} | Output enable |
| 26 | CS | Chip select |
| 27 | \overline{WE} | Write enable |
| 28 | V_{CC} | +5V power supply |

Pin Functions

\overline{RFSH} (Refresh Input)

A built-in refresh control circuit enables this input. Two refresh modes are available: pulse refresh, using the \overline{RFSH} input as a clock input, and power-down self-refresh, using the \overline{RFSH} input as logic level input. \overline{RFSH} is high (inactive) during normal read and write cycles.

A_0 - A_{12} (Address Inputs)

The μ PD4168 requires 13 address inputs to select a word of data. Because these address inputs are internally read onto the chip at the falling edge of a \overline{CE} clock pulse, the \overline{CE} clock determines their address setup and hold times. Inputs A_0 - A_8 perform external refresh.

I/O₀-I/O₇ (Data Inputs/Outputs)

Common I/O pins require \overline{WE} and \overline{OE} to control data. The \overline{CE} clock and \overline{WE} determine the data setup and hold times (t_{DSC} , t_{DHC} , t_{DSW} , t_{DHW}) for these pins during a memory write cycle; \overline{OE} determines the access time (t_{OEA}) during a read cycle.

GND (Ground)

All voltages are referenced to GND.

\overline{CE} (Chip Enable)

The chip enable clock initiates read/write cycles and external refresh cycles. It allows addresses, CS, and (during an early write cycle) data inputs to be internally read onto the chip.

\overline{OE} (Output Enable)

\overline{OE} controls the output timing for I/O₀-I/O₇. Access time (t_{CEA} , t_{OEA}) is determined by the \overline{CE} clock or by the \overline{OE} input, according to \overline{OE} input timing.

CS (Chip Select)

When CS is high (active) while the \overline{CE} clock is enabled, the μPD4168 can perform read/write operations. If CS is latched low (inactive) while the \overline{CE} clock is enabled, I/O₀-I/O₇ remain in the high-impedance state, regardless of the status of \overline{WE} and \overline{OE} .

\overline{WE} (Write Enable)

\overline{WE} controls read/write operations. \overline{WE} input timing determines whether a write cycle is an early write or a late write.

VCC (Power Supply)

+5 V power supply.

μPD4168 Functional Modes

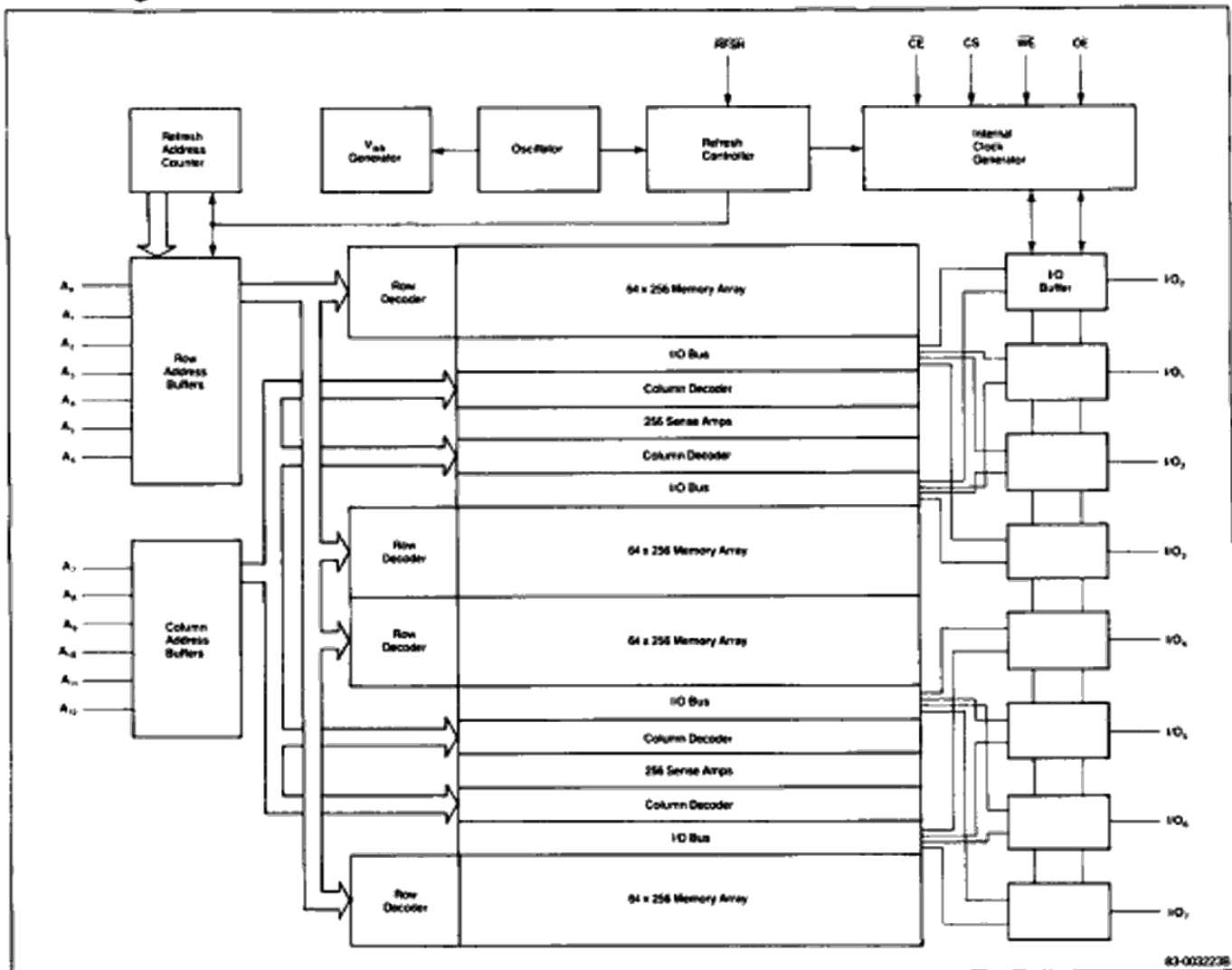
| Mode | RFSH | \overline{CE} | CS | \overline{WE} | \overline{OE} | I/O | Comments |
|-------------------------|------|-----------------|----|-----------------|-----------------|----------|--|
| Read cycle | H | C' | H | H | L | Data out | \overline{OE} : low logic level or clock pulse |
| Early write | H | C' | H | L | H | Data in | |
| Late Write | H | C' | H | C' | H | Data in | |
| External refresh | H | C' | H | H | H | High-Z | |
| | H | C' | L | X | X | High-Z | Standby |
| Pulse refresh | C' | H | X | X | X | High-Z | |
| | C' | C' | H | H | H | High-Z | After external refresh cycle |
| | C' | C' | H | H | L | (Note 1) | After read cycle |
| | C' | C' | H | L | H | Data in | After early write cycle |
| | C' | C' | H | C' | H | Data in | After late write cycle |
| Power down self-refresh | L | H | X | X | X | High-Z | |
| Standby | H | H | X | X | X | High-Z | |

H = V_{SH}, L = V_{SL}, C' = negative edge of clock pulse, X = V_{SH} or V_{SL}

Note:

(1) Depends on previous cycle

Block Diagram



Absolute Maximum Ratings

| | |
|--|----------------|
| Voltage on any pin relative to GND | -1.0 to +7.0 V |
| Operating temperature, T_{OPR} | 0 to +70°C |
| Storage temperature, T_{STG} | -55 to +125°C |
| Short circuit output current, I_{OS} | 50 mA |
| Power dissipation, P_D | 1 W |

Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of the specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

$T_A = 0$ to $+70^\circ\text{C}$; $V_{CC} = 5\text{V} \pm 10\%$

| Parameter | Symbol | Limits | | | Unit | Test Conditions |
|---------------------|----------|--------|-----|-----|------|------------------------|
| | | Min | Typ | Max | | |
| Supply voltage | V_{CC} | 4.5 | 5.0 | 5.5 | V | Referenced to GND |
| Input voltage, low | V_{IL} | -1.0 | | 0.8 | V | Referenced to GND |
| Input voltage, high | V_{IH} | 2.4 | | 5.5 | V | Referenced to GND |
| Output voltage, low | V_{OL} | 0 | | 0.4 | V | $I_{OL} = 2\text{ mA}$ |

DC Characteristics (cont)

| Parameter | Symbol | Limits | | | Unit | Test Conditions |
|--|-------------------|--------|-----|-----------------|------|--|
| | | Min | Typ | Max | | |
| Output voltage, high | V _{OH} | 2.4 | | V _{CC} | V | I _{OH} = -1 mA |
| Average V _{CC} supply current, active | I _{CC1} | | | 65 | mA | t _C = 220 ns |
| | | | | 60 | mA | t _C = 260 ns |
| | | | | 55 | mA | t _C = 330 ns |
| Standby current | I _{CC2} | | | 5 | mA | $\overline{CE} \geq V_{IH} \text{ min,}$ RFSH $\geq V_{IH} \text{ min}$ |
| Self-refresh average current | I _{CC3} | | | 3.5 | mA | RFSH $\leq V_{IL} \text{ max}$ |
| Input leakage current | I _{I(L)} | -10 | | 10 | μA | V _{IN} = 0 to 5.5 V; others = 0 V |
| Output leakage current | I _{O(L)} | -10 | | 10 | μA | V _{OUT} = 0 to 5.5 V; D _{OUT} = High-Z |

Capacitance

T_A = 0 to +70°C, V_{CC} = 5.0 V ± 10%

| Parameter | Symbol | Limits | | | Unit | Test Conditions |
|----------------------|------------------|--------|-----|-----|------|-----------------|
| | | Min | Typ | Max | | |
| Input capacitance | C _I | | | 10 | pF | f = 1 MHz |
| Data I/O capacitance | C _{I/O} | | | 10 | pF | f = 1 MHz |

AC Characteristics

T_A = 0 to +70°C, V_{CC} = 5 V ± 10%

| Parameter | Symbol | Limits | | | | | | Unit | Test Conditions |
|--|-------------------|------------|-------|------------|-------|------------|-------|------|---------------------------------------|
| | | μPD4168-12 | | μPD4168-15 | | μPD4168-20 | | | |
| | | Min | Max | Min | Max | Min | Max | | |
| Average V _{CC} supply current, active | I _{CC1} | | 65 | | 60 | | 55 | mA | t _C = t _C (min) |
| Read, write, or refresh cycle time | t _C | 220 | | 260 | | 330 | | ns | |
| Access time from \overline{CE} | t _{CEA} | | 120 | | 150 | | 200 | ns | (Note 5) |
| Data off time from \overline{CE} | t _{CEZ} | | 30 | | 35 | | 45 | ns | (Note 6) |
| Access time from \overline{OE} | t _{OE A} | | 45 | | 55 | | 70 | ns | (Note 5) |
| Data off time from \overline{OE} | t _{OEZ} | | 30 | | 35 | | 45 | ns | (Note 6) |
| \overline{CE} pulse width | t _{CE} | 120 | 10000 | 150 | 10000 | 200 | 10000 | ns | |
| \overline{CE} precharge time | t _p | 90 | | 100 | | 120 | | ns | |
| Address setup time to \overline{CE} | t _{ASC} | 0 | | 0 | | 0 | | ns | |
| Address hold time from \overline{CE} | t _{AHC} | 35 | | 45 | | 55 | | ns | |
| CS setup time to \overline{CE} | t _{CSC} | 0 | | 0 | | 0 | | ns | |
| CS hold time from \overline{CE} | t _{CHC} | 35 | | 45 | | 55 | | ns | |
| Data setup time to \overline{CE} , early write | t _{DSC} | -10 | | -10 | | -10 | | ns | |
| Data hold time from \overline{CE} , early write | t _{DHC} | 90 | | 100 | | 120 | | ns | |
| Data setup time to \overline{WE} , late write | t _{DSW} | 0 | | 0 | | 0 | | ns | |
| Data hold time from \overline{WE} , late write | t _{DHW} | 50 | | 60 | | 70 | | ns | |
| \overline{WE} setup time to \overline{CE} , early write | t _{WSC} | -30 | | -30 | | -30 | | ns | (Note 7) |
| \overline{WE} hold time from \overline{CE} , early write | t _{WHC} | 90 | | 100 | | 125 | | ns | |
| \overline{WE} pulse duration | t _{WD} | 60 | | 70 | | 90 | | ns | |
| \overline{CE} hold time from \overline{WE} , late write | t _{CHW} | 90 | | 105 | | 135 | | ns | |
| \overline{WE} setup time to \overline{CE} , read cycle | t _{RCS} | 0 | | 0 | | 0 | | ns | |
| \overline{WE} hold time from \overline{CE} , read cycle | t _{RCH} | 0 | | 0 | | 0 | | ns | |
| \overline{CE} hold time from \overline{OE} , read cycle | t _{CHO} | 45 | | 55 | | 70 | | ns | |
| \overline{OE} setup time to \overline{CE} , write cycle | t _{OES} | 0 | | 0 | | 0 | | ns | |
| \overline{OE} hold time from \overline{CE} , write cycle | t _{OEH} | 0 | | 0 | | 0 | | ns | |

AC Characteristics (cont)

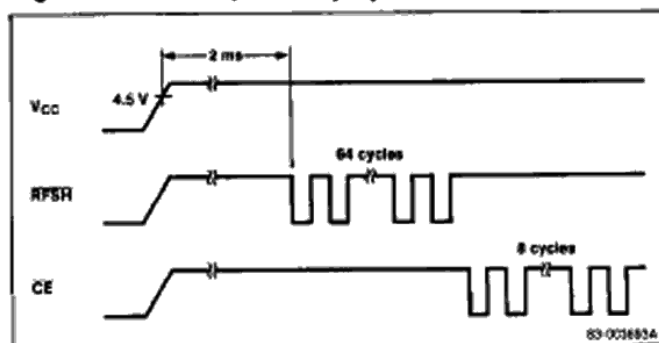
$T_A = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$

| Parameter | Symbol | Limits | | | | | | Unit | Test Conditions |
|---|------------------|------------|------|------------|------|------------|------|------|-----------------|
| | | μPD4168-12 | | μPD4168-15 | | μPD4168-20 | | | |
| | | Min | Max | Min | Max | Min | Max | | |
| CE delay to $\overline{\text{RFSH}}$, pulse refresh | t_{CRD} | 50 | | 65 | | 80 | | ns | |
| $\overline{\text{RFSH}}$ pulse width, pulse refresh | t_{RDP} | 50 | 4000 | 65 | 4000 | 80 | 4000 | ns | |
| $\overline{\text{RFSH}}$ recovery time, pulse refresh | t_{RPR} | 90 | | 100 | | 120 | | ns | |
| $\overline{\text{RFSH}}$ pulse width, self refresh | t_{RDS} | 40 | | 40 | | 40 | | μs | (Note 8) |
| $\overline{\text{RFSH}}$ recovery time, self refresh | t_{RSR} | 2 | | 2 | | 2 | | μs | |
| CE hold time from $\overline{\text{RFSH}}$, self refresh | t_{CSH} | 40 | | 40 | | 40 | | μs | |
| CE setup time to $\overline{\text{RFSH}}$, self refresh | t_{CSS} | 35 | | 40 | | 50 | | ns | |
| Transition time, rise and fall | t_T | 3 | 50 | 3 | 50 | 3 | 50 | ns | (Note 4) |
| Refresh period | t_{REF} | | 2 | | 2 | | 2 | ms | |
| $\overline{\text{RFSH}}$ precharge time | t_{PP} | 90 | | 100 | | 120 | | ns | |
| $\overline{\text{OE}}$ lead time to refresh cycle | t_{OEL} | 170 | | 210 | | 260 | | ns | |
| $\overline{\text{WE}}$ lead time to refresh cycle | t_{WEL} | 170 | | 210 | | 260 | | ns | |
| $\overline{\text{RFSH}}$ setup time to CE | t_{RC} | 280 | | 320 | | 410 | | ns | |

Note:

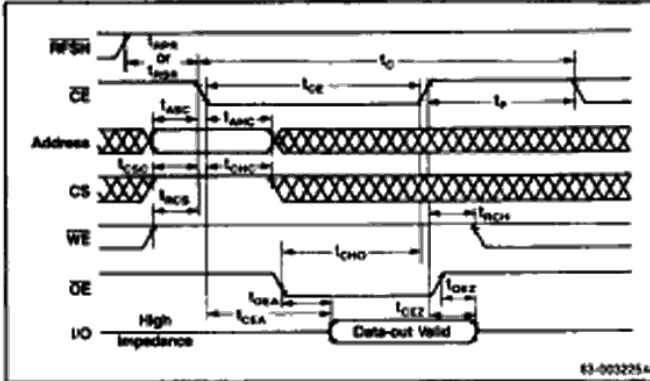
- (1) All voltages referenced to GND (0 V).
- (2) An initial pause of 2 ms is required after power up, followed by any 8 $\overline{\text{CE}}$ cycles and 64 $\overline{\text{RFSH}}$ cycles before proper device operation is achieved. Read, write, and external refresh cycles may be used as $\overline{\text{CE}}$ dummy cycles for initialization. The 64 refresh dummy cycles can be performed before or after the 8 $\overline{\text{CE}}$ dummy cycles. Both dummy cycles must be within AC parameters. See figure 1, below.
- (3) AC measurements assume $t_T = 5$ ns.
- (4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring input signal timing. Transition times are measured between V_{IH} and V_{IL} .
- (5) Load = 2 TTL loads and 50 pF.
- (6) t_{CEZ} (max) and t_{OEZ} (max) define the time at which the output achieves the open circuit condition and are not referenced to V_{OH} or V_{OL} .
- (7) $t_{\text{WSC}} \leq t_{\text{WSC}}$ (min), the cycle is a late write cycle.
- (8) A power down self-refresh cycle is initiated when the $\overline{\text{RFSH}}$ input is active low for a period of 40 μs. The refresh interval is about 15.6 μs.

Figure 1. Power-up Dummy Cycles

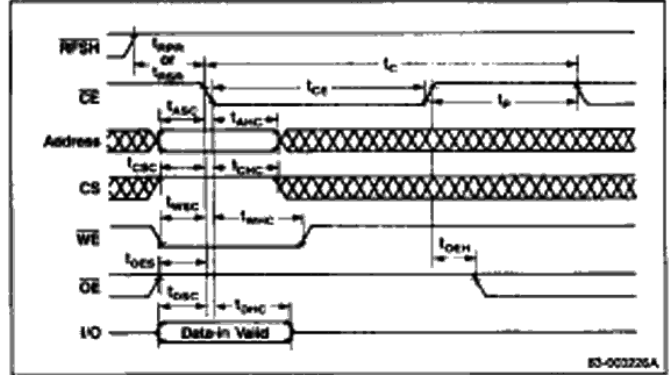


Timing Waveforms

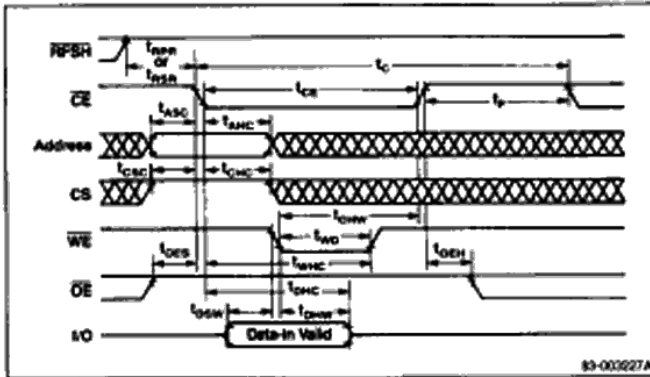
Read Cycle



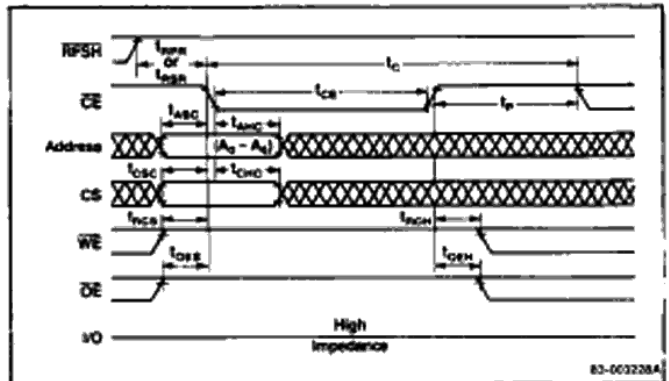
Early Write Cycle



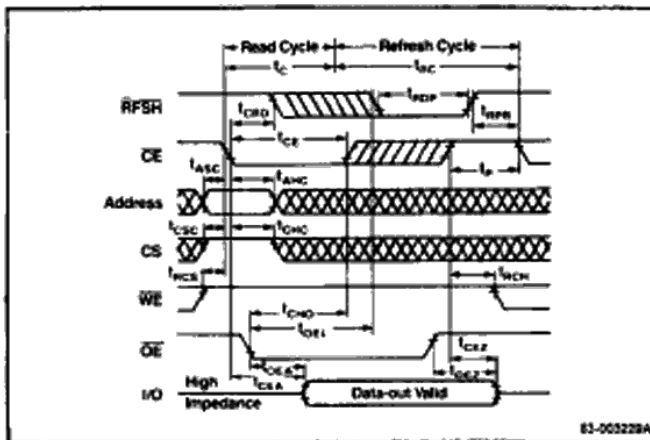
Late Write Cycle



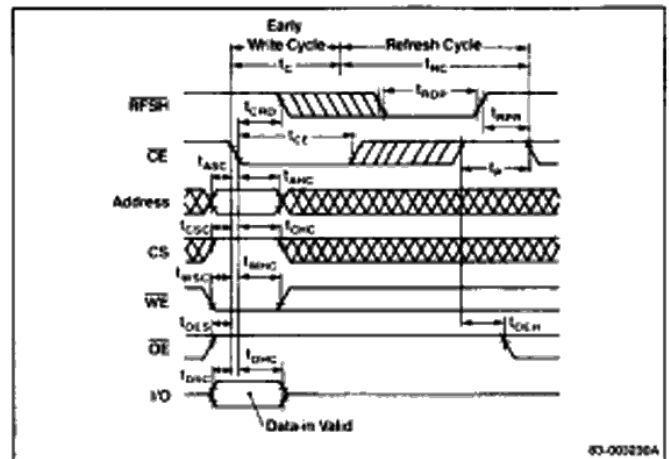
External Refresh Cycle



Pulse Refresh Cycle after Read Cycle Complete

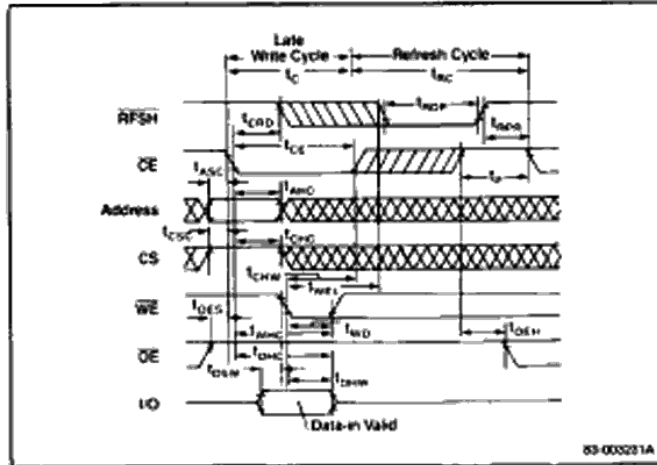


Pulse Refresh Cycle after Early Write Cycle Complete

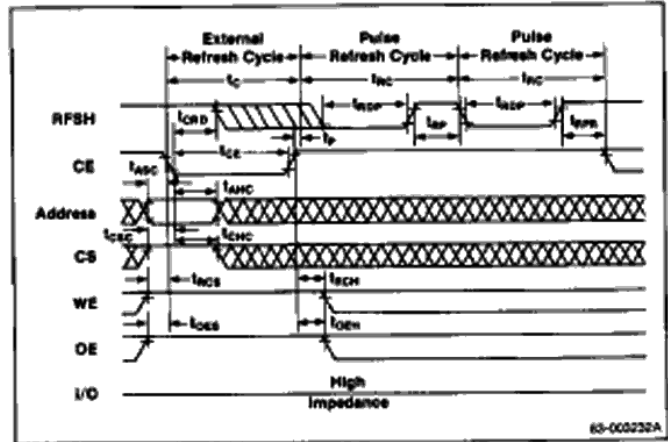


Timing Waveforms (cont)

Pulse Refresh Cycle after Late Write Cycle Complete



Pulse Refresh Cycle after External Refresh Cycle Complete



Power-down Self Refresh

