NEC

MOS INTEGRATED CIRCUIT
μPD4702

INCREMENTAL ENCODER 8-BIT UP/DOWN COUNTER
CMOS INTEGRATED CIRCUITS

DESCRIPTION

The μPD4702 is 8-bit up/down counters for an incremental encoder. Two-phase (A, B) incremental input signals are phase-differentiated, and on each signal edge, an up-count is executed if the A phase is leading, or a down-count if the B phase is leading. Eight-bit count data is output in real time. A carry output and borrow output are also provided for counter overflow and underflow.

The μPD4704 is also available; use of these enables the count width to be extended.

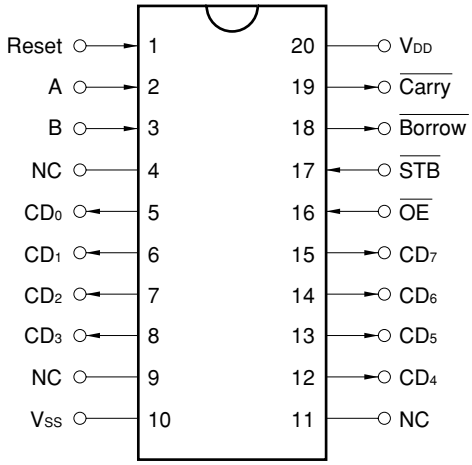
FEATURES

- Incremental inputs (A, B)
- On-chip phase discrimination circuit (up-count mode when the phase order is A → B, down-count mode when B → A) 4-multiplication count method
- On-chip edge detection circuit
- 8-bit up/down counter latch output
- Carry output, borrow output
- Count data output controllable (3-state output)
- CMOS, single +5 V power supply

★ ORDERING INFORMATION

Part Number	Package
μPD4702C	20-pin plastic DIP (7.62 mm (300))
μPD4702G	20-pin plastic SOP (7.62 mm (300))

PIN CONFIGURATION (Top View)



PIN NAMES

A, B: 2-phase incremental signal inputs
Reset : Counter reset input
STB : Latch strobe signal input
OE : Output control signal input
CD0 to CD7 : Count data outputs
Carry : Carry pulse output
Borrow : Borrow pulse output

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The mark ★ shows major revised points.

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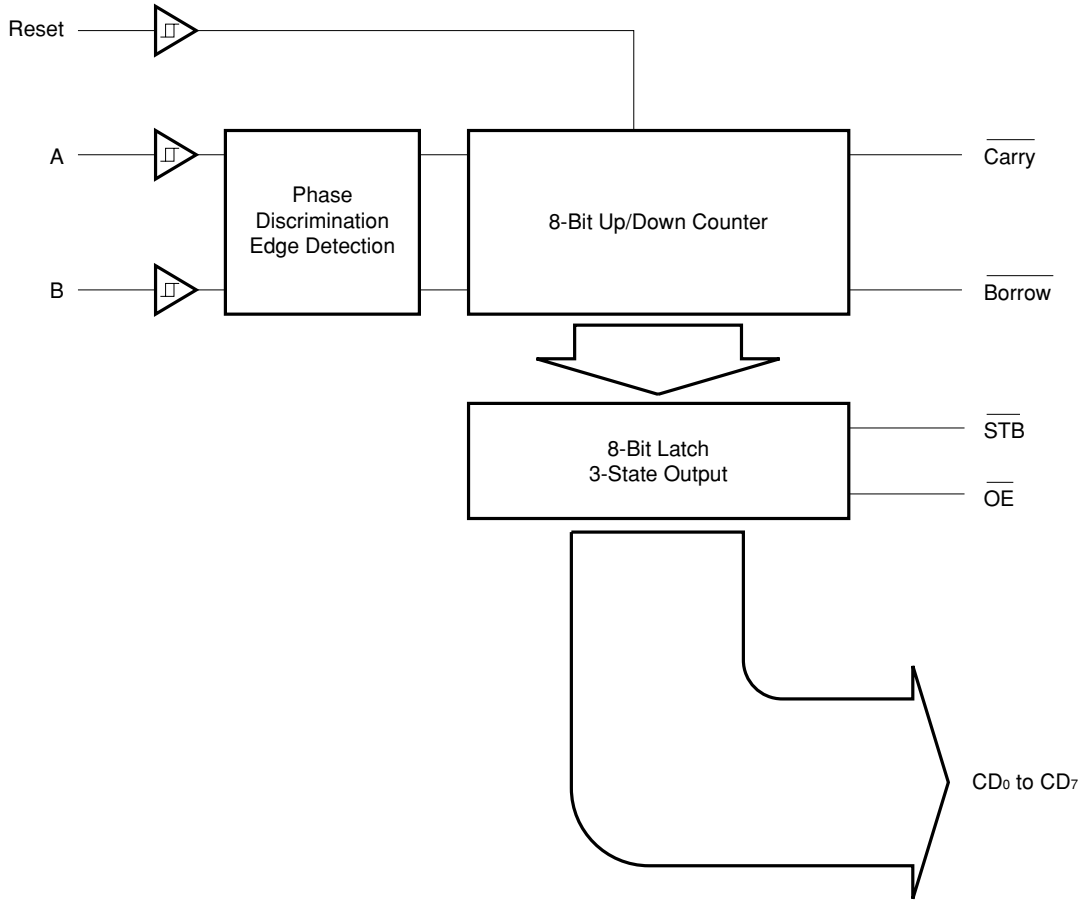
BLOCK DIAGRAM



PIN FUNCTIONS

Pin Name	Input/Output	Function
A, B	Input (Schmitt)	Incremental signal A phase and B phase signal input pins (Schmitt input)
CD_0 to CD_7	Output (3-state)	Count data output pins. Activated when $\overline{OE}$ is "L", high impedance outputs when $\overline{OE}$ is "H". 8-bit counter carry signal output pin (active-low)
$\overline{Carry}$	Output	8-bit counter borrow signal output pin (active-low)
$\overline{Borrow}$	Output	8-bit counter reset signal output pin
RESET	Input (Schmitt)	Counter is reset when this pin is "H".
$\overline{OE}$	Input	Count data output control signal input pin
$\overline{STB}$	Input	Counter data output latch signal. Data is latched on the fall of $\overline{STB}$, and is held while $\overline{STB}$ = "L".
V_{DD}	–	Power supply input pin
GND	–	Ground pin

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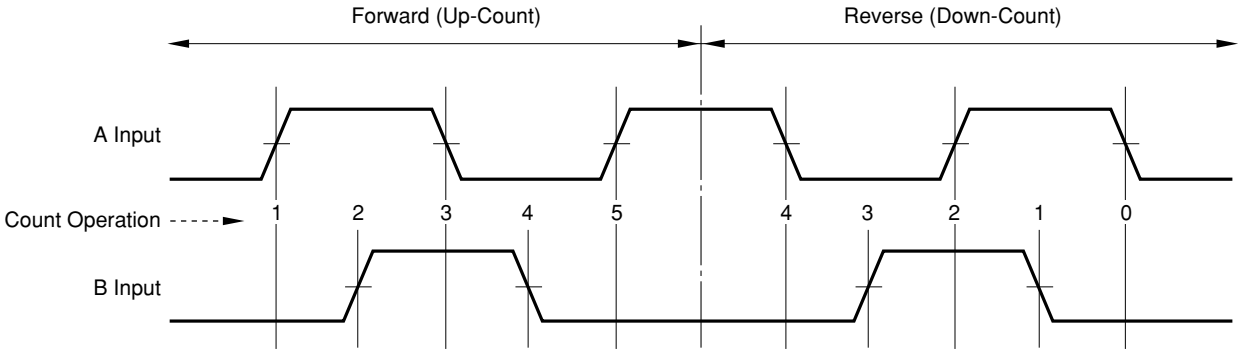
1. DESCRIPTION OF OPERATIONS

(1) Count operation

The μPD4702 incorporates a phase discrimination circuit, and counts by 4-multiplication of the A and B input 2-phase pulses. Therefore, a count operation is performed by an A input edge and a B input edge.

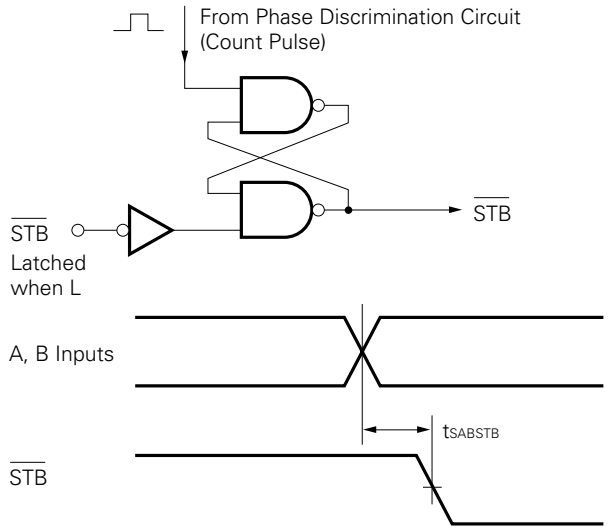
Figure 1–1. Count Operation Timing Chart



(2) Latch operation

An R-S flip-flop is inserted in the strobe input of the latch circuit as shown in Figure 1–2, and when $\overline{STB}$ changes from "H" to "L" during a count operation, the internal latch signal $\overline{STB}$ remains at "H" until the end of the count operation. Therefore, the count value is latched correctly even if $\overline{STB}$ input is performed asynchronously from the A and B input (if $\overline{STB}$ changes from "H" to "L" within t_{SABSTB} (40 ns) after the A input or B input edge, the latch contents will be either the pre-count or post-count value). However, when a μPD4704 is added, the correct value cannot be latched if all digits are latched simultaneously when a carry or borrow is generated (the high-order digit may be latched before carry/borrow transmission).

Figure 1–2. STB Input Circuit



If t_{SABSTB} is 40 ns or longer, the post-count value is input to the latch.

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(3) Carry & borrow outputs

If the counter performs an up-count operation when the count value is 0FFH, an active-low pulse is output to the $\overline{\text{Carry}}$ output (the pulse width is 25 ns MIN. 120 ns MAX. irrespective of the A/B phase input cycle. Similarly, if the counter performs a down-count operation when the count value is 00H, an active-low pulse is output to the $\overline{\text{Borrow}}$ output.

A $\overline{\text{Borrow}}$ pulse is also output if a down-count operation is performed while RESET is “H” (during a reset), and therefore, when a μPD4704 is added, a reset must be executed at the same time.

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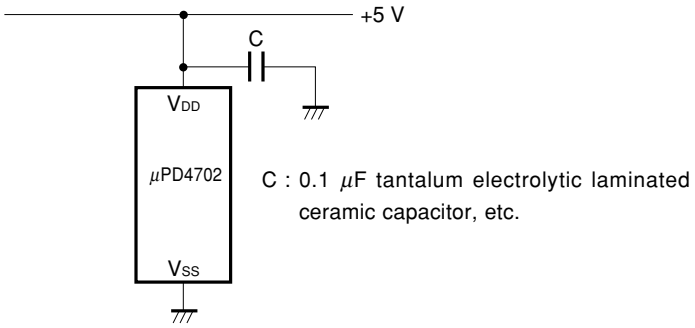
2. OPERATING PRECAUTIONS

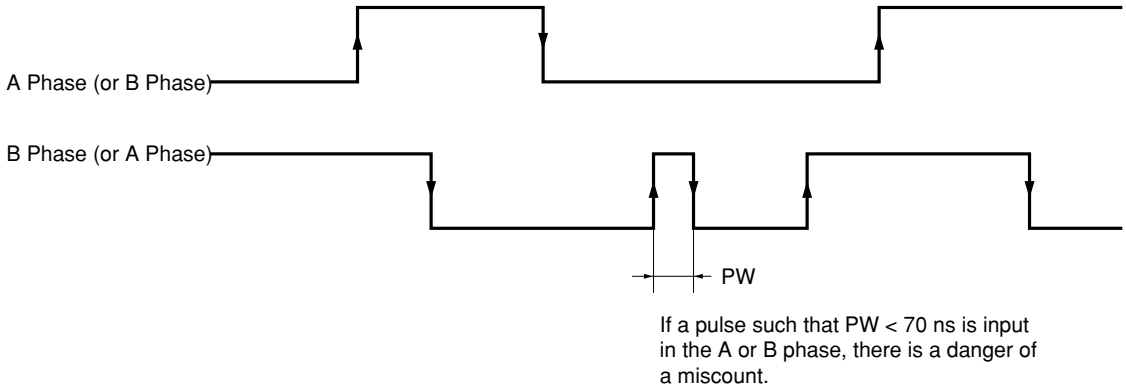
As the μPD4702 incorporates an 8-bit counter, a large transient current flows in the case of a count value which changes all the bits (such as 00H ↔ 0FFH or 7FH ↔ 080H). This will cause misoperation unless the impedance of the power supply line is sufficiently low. It is therefore recommended that a decoupling capacitor (of around 0.1 μF) be connected between V_{DD} and V_{SS} right next to the IC as shown in Figure 2–1.

Figure 2–1. Decoupling Capacitor



Also, if a pulse shorter than the phase difference time t_{SAB} (70 ns) is input to the A/ B phase inputs, this will result in a miscount. Therefore, if this kind of pulse is to be input because of encoder bounds, etc., a filter should be inserted in the A & B phase inputs.

Figure 2–2. A & B Phase Input Pulses



If PW is at 70 ns or more, the count value remains the same before and after pulse input. (UP count → DOWN count or DOWN count → UP count is implemented, and therefore the the result is no change in the count value.)

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3. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, V_{SS} = 0 V)

PARAMETER	SYMBOL	RATING		UNIT
Supply voltage	V_{DD}	–0.5 to +7.0		V
Input voltage	V_I	–1.0 to V_{DD} +1.0		V
Output voltage	V_O	–0.5 to V_{DD} +0.5		V
Operating temperature	T_{opt}	–40 to +85		°C
Storage temperature	T_{stg}	–65 to +150		°C
Permissible loss	P_D	500 (DIP)	200 (SOP)	mW

DC CHARACTERISTICS (T_A = –40 to +85 °C, V_{DD} = +5 V ±10 %)

PARAMETER	SYMBOL	TEST CONDITIONS	RATING		UNIT
			MIN.	MAX.	
Input voltage high	V_{IL}			0.8	V
Input voltage low	V_{IH}	A, B, Reset	2.6		V
	V_{IH}	Other than the above	2.2		V
Output voltage low	V_{OL}	I_{OL} = 12 mA		0.45	V
Output voltage high	V_{OH}	I_{OH} = –4 mA	V_{DD} – 0.8		V
Static consumption current	I_{DD}	V_I = V_{DD}, V_{SS}		50	μA
Input current	I_I	V_I = V_{DD}, V_{SS}	–1.0	1.0	μA
3-state output leak current	I_{OFF}		–10	10	μA
Dynamic consumption current	$I_{DD\ dyn}$	f_{IN} = 3.6 MHz, C_L = 50 pF		12	mA
Hysteresis voltage	V_H	A, B, Reset	0.2		V

AC CHARACTERISTICS (T_A = –40 to +85 °C, V_{DD} = +5 V ±10 %)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN.	MAX.	UNIT
A, B	Cycle	t_{CYAB}	f_{IN} = 3.6 MHz	280		ns
	High-level width	t_{PWABH}		140		ns
	Low-level width	t_{PWABL}		140		ns
	Phase difference time	t_{SAB}		70		ns
	Setting time	t_{SRSAB}		0		ns
CD_0 to CD_7	Reset time	t_{DRSCD}			60	ns
	Output delay	t_{DABCD}			100	ns
	Output delay	t_{DOECD}			50	ns
	Output delay	t_{DSTBCD}			60	ns
	Float time	t_{FOECD}			40	ns
$\overline{Carry}$	Output delay	t_{DABCB}			120	ns
$\overline{Borrow}$	Output pulse width	t_{PWCB}		25	120	ns
RESET	Reset pulse width	t_{PWRS}		40		ns
$\overline{STB}$	Setting time	t_{SABSTB}		40		ns

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AC Timings

Figure 3–1. Two-Phase Signal Input Timing

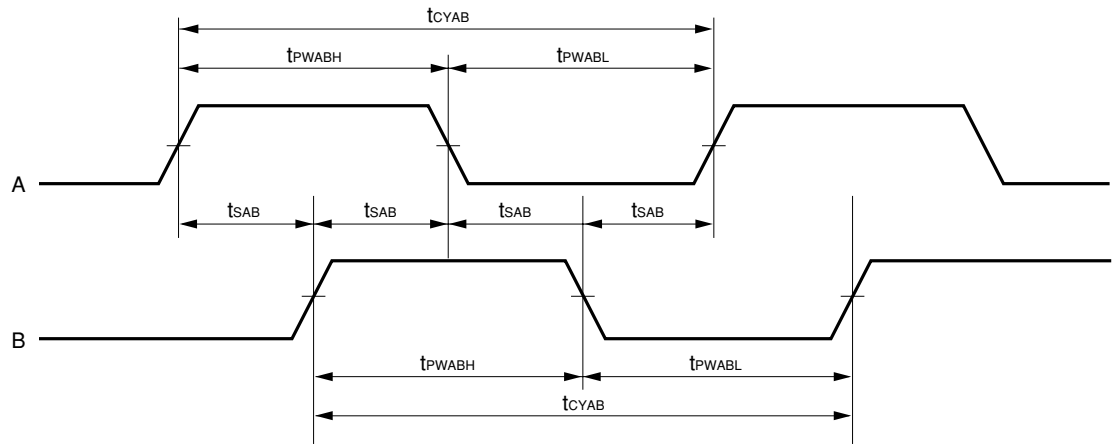


Figure 3–2. Count Data Output Timing

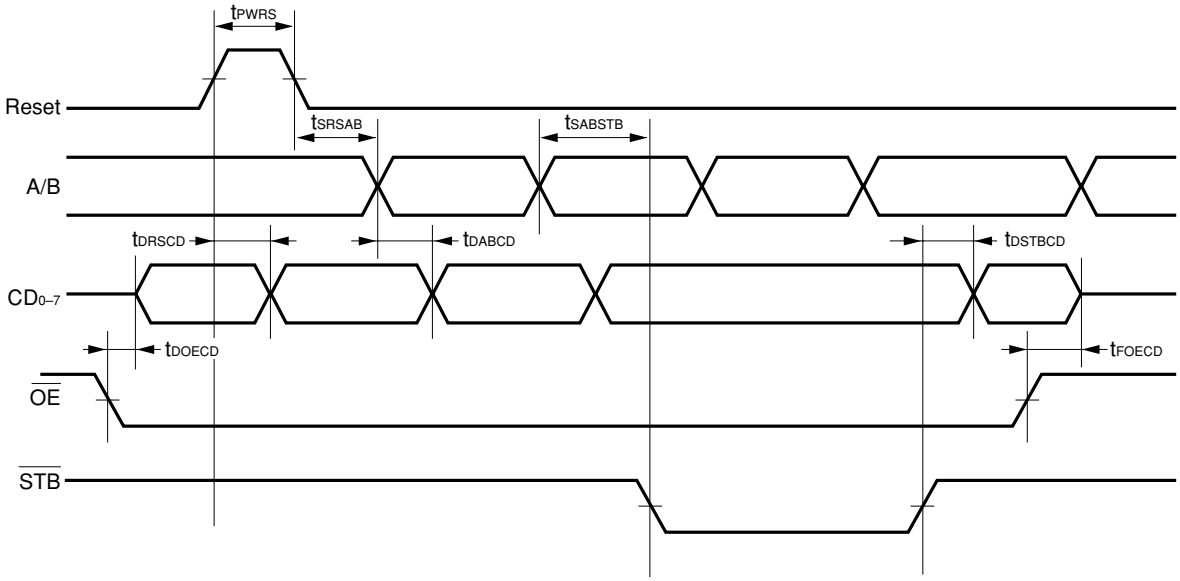
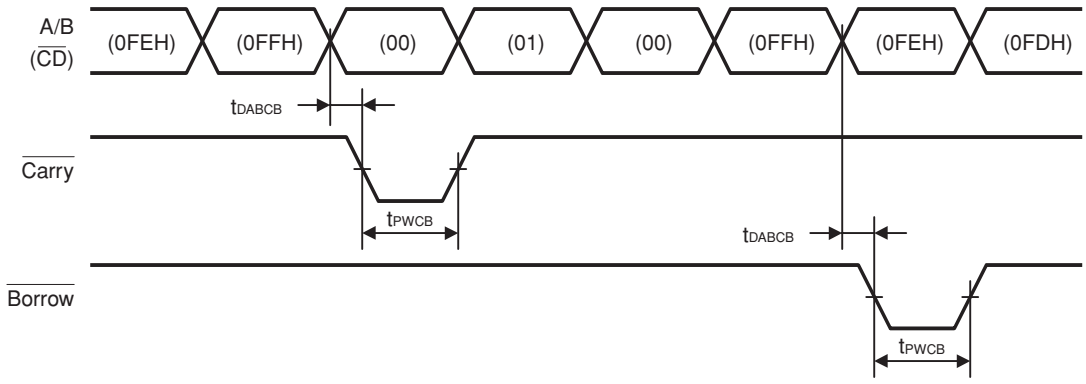


Figure 3–3. $\overline{\text{Carry}}$/$\overline{\text{Borrow}}$ Signal Output Timing



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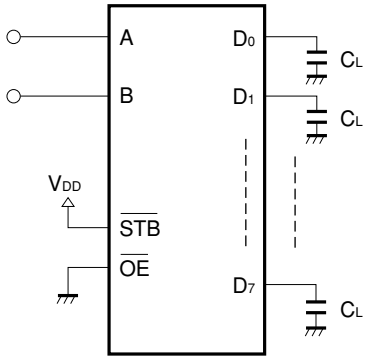
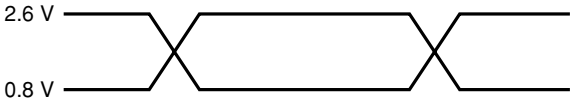
Consumption Current Measurement Circuit

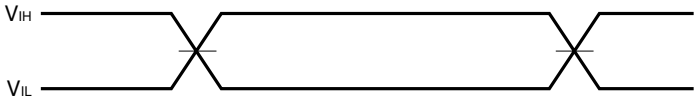


Measurement Conditions
A, B inputs
f_{IN} = 3.6 MHz



$\overline{STB}$ input connected to V_{DD} or
$\overline{OE}$ input connected to V_{SS}.
Load on all outputs, C_L = 50 pF.

AC Test Input Waveform



V_{IH} = 2.6 V (A, B, RESET inputs)
V_{IH} = 2.2 V (inputs other than A, B, RESET)
V_{IL} = 0.8 V
Timing measurement is performed at 1.5 V.

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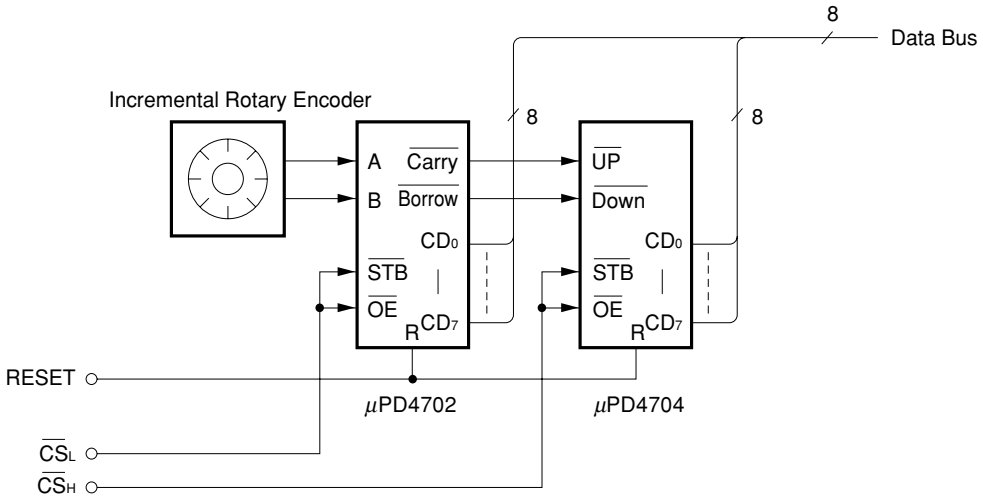
4. SAMPLE APPLICATION CIRCUITS

16-bit counter



The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

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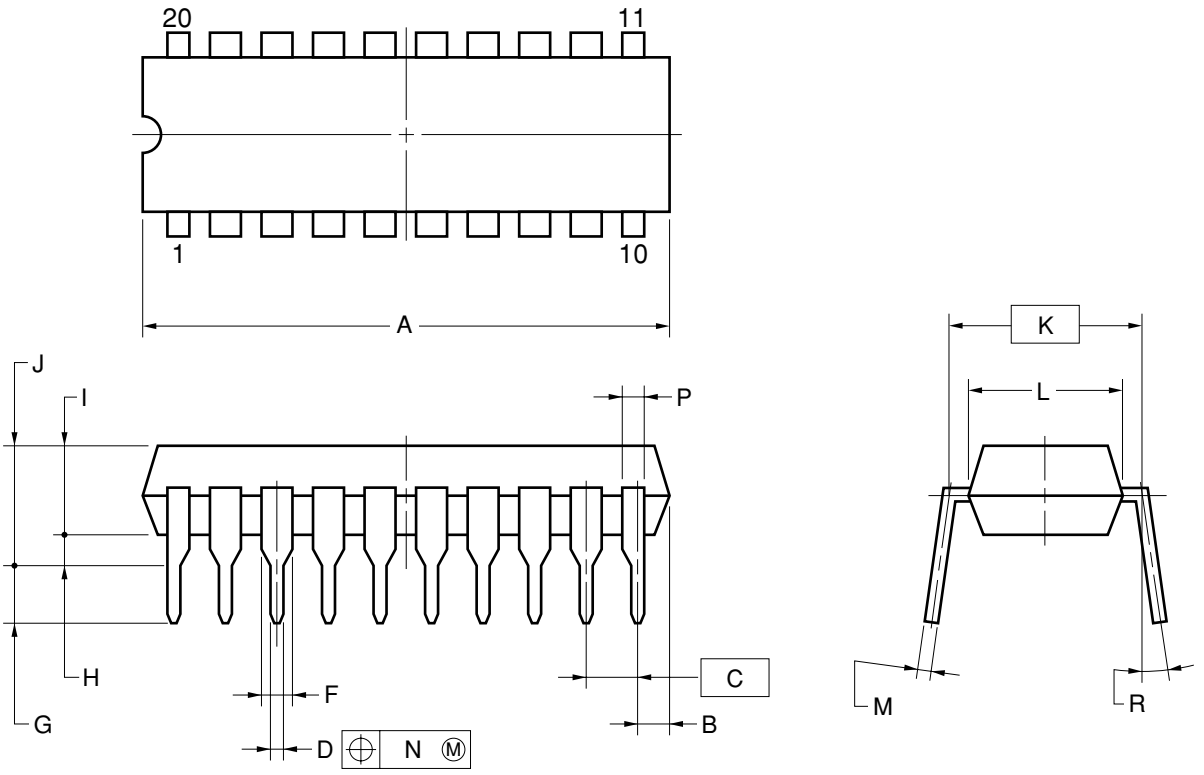
★ 5. PACKAGE DRAWINGS

20-PIN PLASTIC DIP (7.62mm(300))



NOTES

1. Each lead centerline is located within 0.25 mm of its true position (T.P.) at maximum material condition.

2. Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS
A	25.40 MAX.
B	1.27 MAX.
C	2.54 (T.P.)
D	0.50±0.10
F	1.1 MIN.
G	3.5±0.3
H	0.51 MIN.
I	4.31 MAX.
J	5.08 MAX.
K	7.62 (T.P.)
L	6.4
M	$0.25^{+0.10}_{-0.05}$
N	0.25
P	0.9 MIN.
R	0~15°

P20C-100-300A,C-2

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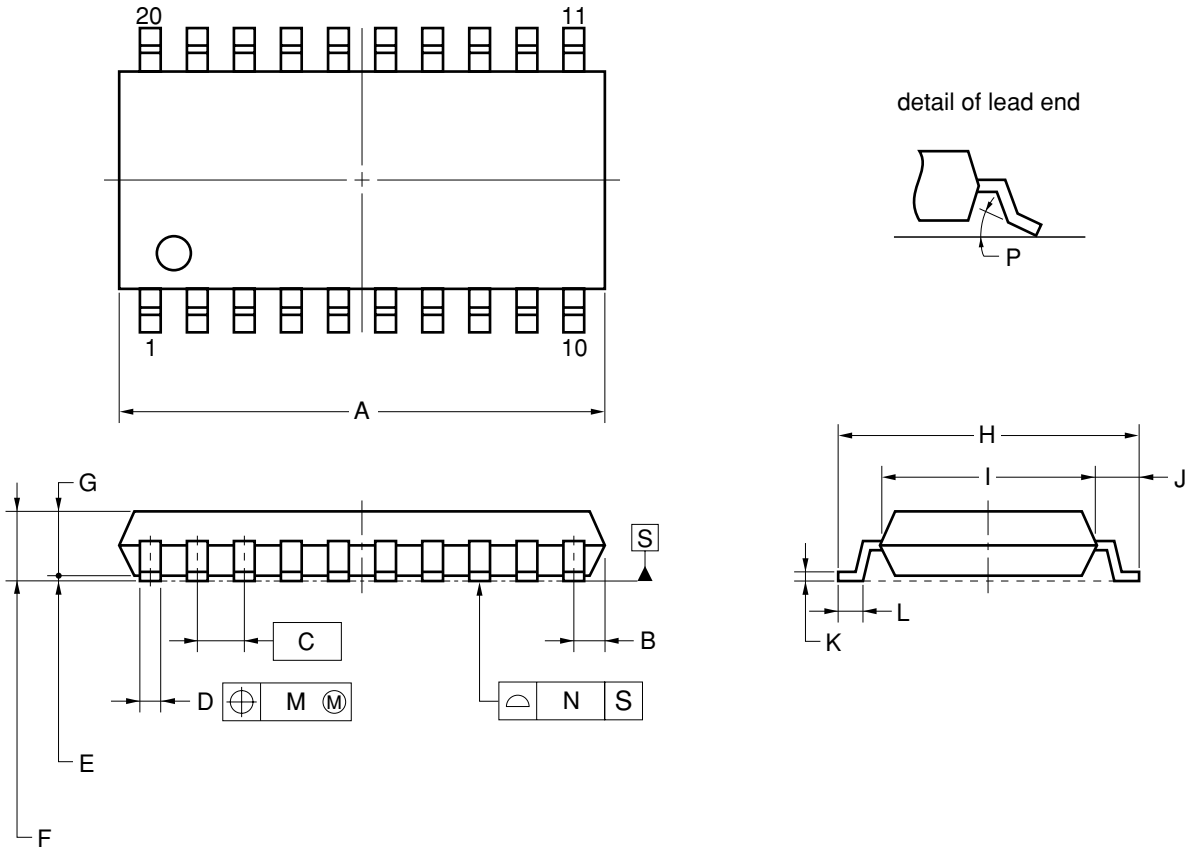
20-PIN PLASTIC SOP (7.62 mm (300))



NOTE

Each lead centerline is located within 0.12 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	12.7±0.3
B	0.78 MAX.
C	1.27 (T.P.)
D	$0.42^{+0.08}_{-0.07}$
E	0.1±0.1
F	1.8 MAX.
G	1.55±0.05
H	7.7±0.3
I	5.6±0.2
J	1.1
K	$0.22^{+0.08}_{-0.07}$
L	0.6±0.2
M	0.12
N	0.10
P	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$

P20GM-50-300B, C-7

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★ 6. RECOMMENDED SOLDERING CONDITIONS

The μPD4702 should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, contact an NEC Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (http://www.necel.com/pkg/en/mount/index.html)

TYPES OF SURFACE MOUNT DEVICE

μPD4702G

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak package's surface temperature: 235 °C or below, Reflow time: 30 seconds or below (210 °C or higher), Number of reflow process: 3, Exposure limit* : None	IR35-00-3
VPS	Peak package's surface temperature: 215 °C or below, Reflow time: 40 seconds or below (200 °C or higher), Number of reflow process: 3, Exposure limit* : None	VP15-00-3
Wave soldering	Solder temperature: 260 °C or below, Flow time: 10 seconds or below, Number of flow process: 1, Exposure limit* : None	WS60-00-1
Partial heating method	Terminal temperature: 300 °C or below, Flow time: 10 seconds or below, Exposure limit* : None	

* Exposure limit before soldering after dry-pack package is opened.
Storage conditions: 25 °C and relative humidity at 65 % or less.

Caution Do not use different soldering methods together (except for partial heating) .

TYPES OF THROUGH HOLE MOUNT DEVICE

μPD4702C

Process	Conditions
Wave soldering (only to leads)	Solder temperature: 260 °C or below, Flow time: 10 seconds or below
Partial Heating Method	Pin temperature: 300 °C or below, Heat time: 3 seconds or less (per each lead).

Caution For through-hole device, the wave soldering process must be applied only to leads, and make sure that the package body does not get jet soldered.

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★ REFERENCE DOCUMENTS

NEC Semiconductor Device Reliability/Quality Control System (C10983E)
Quality Grades on NEC Semiconductor Devices (C11531E)
Guide to Quality Assurance for Semiconductor devices (MEI-1202)
Semiconductor Selection Guide - Products and Packages - (X13769X)

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NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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