

SOURCE DRIVER FOR 300/288-OUTPUT TFT-LCD (NAVIGATION, AUTOMOBILE LCD-TV)

DESCRIPTION

μ PD16782 is a source driver for TFT liquid crystal panels. This IC consists of a multiplexer circuit supporting a variety of pixel arrays, a shift register that generates sampling timing, and two sample and hold circuits that sample analog voltages. Because the two sample and hold circuits alternately execute sampling and holding, a high definition can be obtained.

In addition, simultaneous sampling and successive sampling are automatically selected according to the pixel array of the LCD panel. It is ideal for a wide range of applications, including navigation systems and automobile LCD-TVs.

FEATURES

- Can be driven on 5 V (Dynamic range: 4.3 V, $V_{DD2} = 5.0$ V)
- 300/288-output
- $f_{CLK} = 15$ MHz MAX. ($V_{DD1} = 3.0$ V)
- Simultaneous/successive sampling selectable according to pixel array
 - Simultaneous sampling: Vertical stripe
 - Successive sampling: Delta array, mosaic array
- Two sample and hold circuits
- Low output deviation between pins (± 20 mV MAX.)
- Stripe, delta, and mosaic pixel arrays supported by internal multiplexer circuit
- Left and right shift selected by R,/L pin
- COG mounting possible

Remark /xxx indicates active low signal.

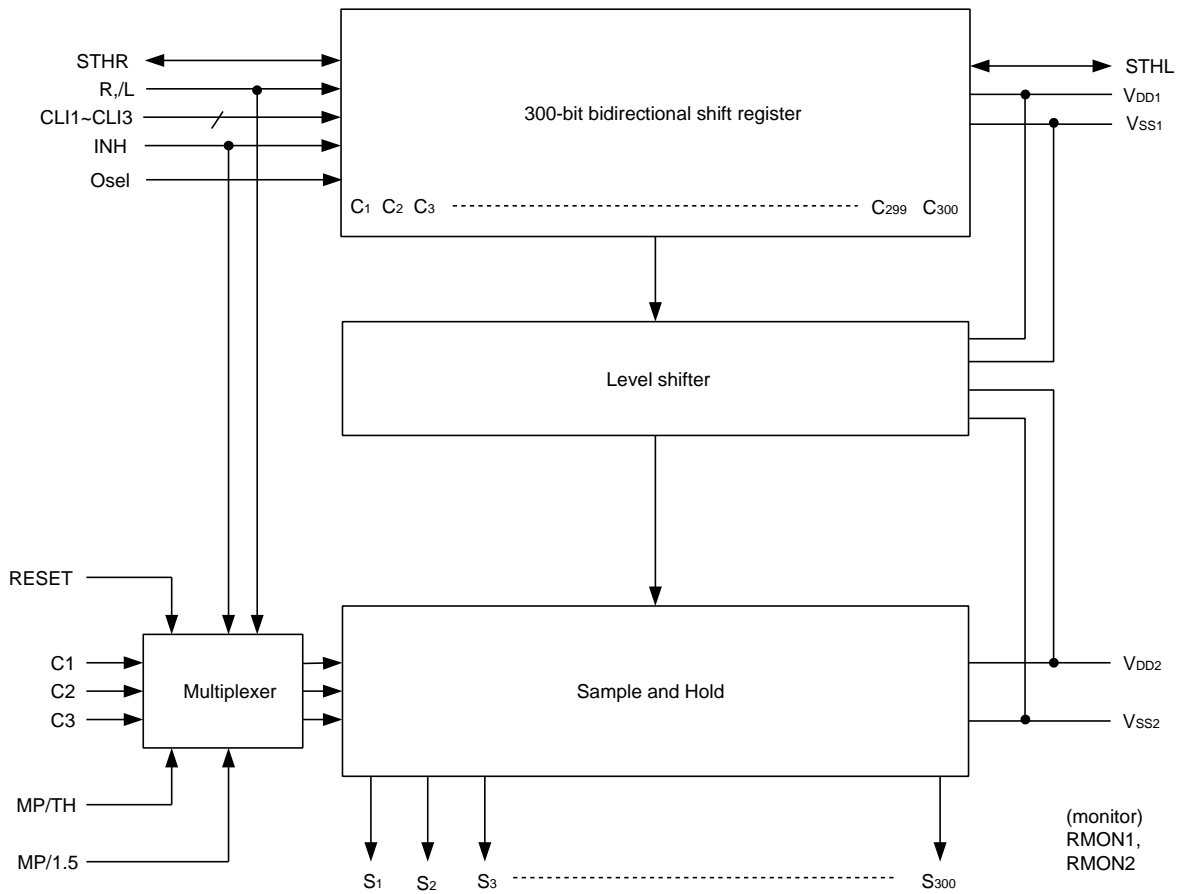
ORDERING INFORMATION

Part Number	Package
μ PD16782P	Chip

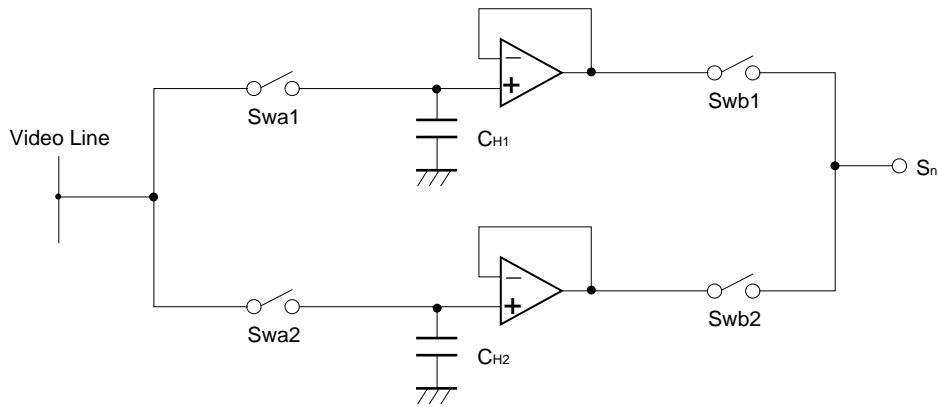
Remark Purchasing the above chip entails the exchange of documents such as a separate memorandum or product quality, so please contact one of our sales representative.

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1. BLOCK DIAGRAM



2. SAMPLE AND HOLD CIRCUIT AND OUTPUT CIRCUIT



3. PIN CONFIGURATION

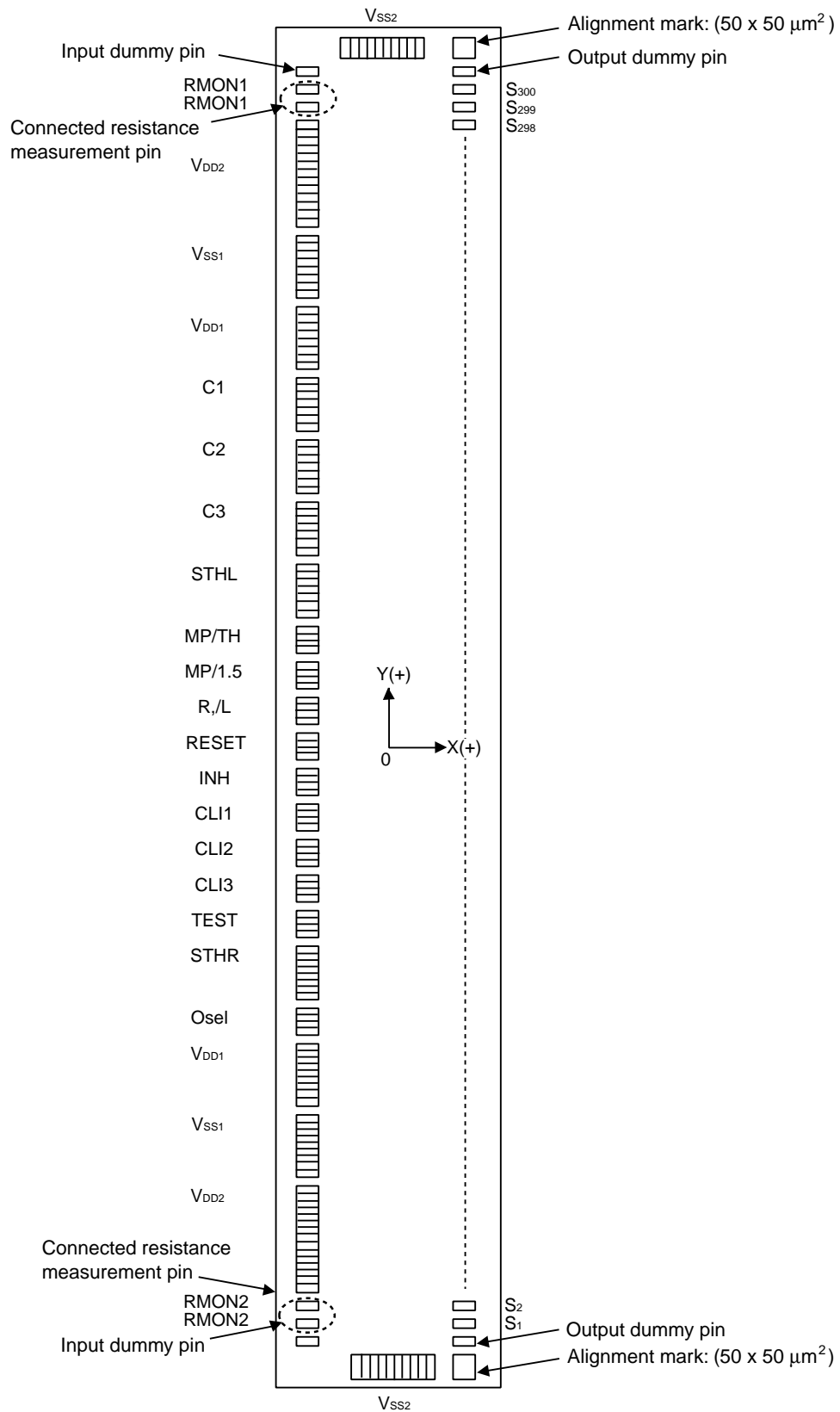


Table 3-1. Pad Layout (1/4)

No.	PAD Name	X [μm]	Y [μm]	Bump Size (X:Y) [μm]
1	Dummy1	-464.0	8451.0	100:60
2	RMON1	-464.0	8014.2	100:60
3	RMON1	-464.0	7842.0	100:60
4	VDD2	-464.0	7538.6	100:60
5	VDD2	-464.0	7458.6	100:60
6	VDD2	-464.0	7378.6	100:60
7	VDD2	-464.0	7298.6	100:60
8	VDD2	-464.0	7218.6	100:60
9	VDD2	-464.0	7138.6	100:60
10	VDD2	-464.0	7058.6	100:60
11	VDD2	-464.0	6978.6	100:60
12	VDD2	-464.0	6898.6	100:60
13	VDD2	-464.0	6818.6	100:60
14	VDD2	-464.0	6738.6	100:60
15	VDD2	-464.0	6658.6	100:60
16	VSS1	-464.0	6181.0	100:60
17	VSS1	-464.0	6101.0	100:60
18	VSS1	-464.0	6021.0	100:60
19	VSS1	-464.0	5941.0	100:60
20	VSS1	-464.0	5861.0	100:60
21	VSS1	-464.0	5781.0	100:60
22	VSS1	-464.0	5701.0	100:60
23	VDD1	-464.0	5239.4	100:60
24	VDD1	-464.0	5159.4	100:60
25	VDD1	-464.0	5079.4	100:60
26	VDD1	-464.0	4999.4	100:60
27	VDD1	-464.0	4919.4	100:60
28	VDD1	-464.0	4839.4	100:60
29	VDD1	-464.0	4759.4	100:60
30	C1	-464.0	4335.2	100:60
31	C1	-464.0	4255.2	100:60
32	C1	-464.0	4175.2	100:60
33	C1	-464.0	4095.2	100:60
34	C1	-464.0	4015.2	100:60
35	C1	-464.0	3935.2	100:60
36	C2	-464.0	3470.4	100:60
37	C2	-464.0	3390.4	100:60
38	C2	-464.0	3310.4	100:60
39	C2	-464.0	3230.4	100:60
40	C2	-464.0	3150.4	100:60
41	C2	-464.0	3070.4	100:60
42	C3	-464.0	2605.6	100:60
43	C3	-464.0	2525.6	100:60
44	C3	-464.0	2445.6	100:60
45	C3	-464.0	2365.6	100:60
46	C3	-464.0	2285.6	100:60
47	C3	-464.0	2205.6	100:60
48	STHL	-464.0	1384.2	100:60
49	STHL	-464.0	1304.2	100:60
50	STHL	-464.0	1224.2	100:60
51	STHL	-464.0	1144.2	100:60
52	STHL	-464.0	1064.2	100:60
53	STHL	-464.0	984.2	100:60
54	MP/TH	-464.0	538.6	100:60
55	MP/TH	-464.0	458.6	100:60

No.	PAD Name	X [μm]	Y [μm]	Bump Size (X:Y) [μm]
56	MP/TH	-464.0	378.6	100:60
57	MP/1.5	-464.0	145.5	100:60
58	MP/1.5	-464.0	65.5	100:60
59	MP/1.5	-464.0	-14.5	100:60
60	R, /L	-464.0	-247.6	100:60
61	R, /L	-464.0	-327.6	100:60
62	R, /L	-464.0	-407.6	100:60
63	RESET	-464.0	-640.7	100:60
64	RESET	-464.0	-720.7	100:60
65	RESET	-464.0	-800.7	100:60
66	INH	-464.0	-1033.8	100:60
67	INH	-464.0	-1113.8	100:60
68	INH	-464.0	-1193.8	100:60
69	CL11	-464.0	-1427.0	100:60
70	CL11	-464.0	-1507.0	100:60
71	CL11	-464.0	-1587.0	100:60
72	CL12	-464.0	-1820.1	100:60
73	CL12	-464.0	-1900.1	100:60
74	CL12	-464.0	-1980.1	100:60
75	CL13	-464.0	-2213.2	100:60
76	CL13	-464.0	-2293.2	100:60
77	CL13	-464.0	-2373.2	100:60
78	TEST	-464.0	-2606.3	100:60
79	TEST	-464.0	-2686.3	100:60
80	TEST	-464.0	-2766.3	100:60
81	STHR	-464.0	-3227.0	100:60
82	STHR	-464.0	-3307.0	100:60
83	STHR	-464.0	-3387.0	100:60
84	STHR	-464.0	-3467.0	100:60
85	STHR	-464.0	-3547.0	100:60
86	STHR	-464.0	-3627.0	100:60
87	Osel	-464.0	-4170.4	100:60
88	Osel	-464.0	-4250.4	100:60
89	Osel	-464.0	-4330.4	100:60
90	VDD1	-464.0	-4759.4	100:60
91	VDD1	-464.0	-4839.4	100:60
92	VDD1	-464.0	-4919.4	100:60
93	VDD1	-464.0	-4999.4	100:60
94	VDD1	-464.0	-5079.4	100:60
95	VDD1	-464.0	-5159.4	100:60
96	VDD1	-464.0	-5239.4	100:60
97	VSS1	-464.0	-5701.0	100:60
98	VSS1	-464.0	-5781.0	100:60
99	VSS1	-464.0	-5861.0	100:60
100	VSS1	-464.0	-5941.0	100:60
101	VSS1	-464.0	-6021.0	100:60
102	VSS1	-464.0	-6101.0	100:60
103	VSS1	-464.0	-6181.0	100:60
104	VDD2	-464.0	-6658.6	100:60
105	VDD2	-464.0	-6738.6	100:60
106	VDD2	-464.0	-6818.6	100:60
107	VDD2	-464.0	-6898.6	100:60
108	VDD2	-464.0	-6978.6	100:60
109	VDD2	-464.0	-7058.6	100:60
110	VDD2	-464.0	-7138.6	100:60

Table 3-1. Pad Layout (2/4)

No.	PAD Name	X [μm]	Y [μm]	Bump Size (X:Y) [μm]
111	V _{DD2}	-464.0	-7218.6	100:60
112	V _{DD2}	-464.0	-7298.6	100:60
113	V _{DD2}	-464.0	-7378.6	100:60
114	V _{DD2}	-464.0	-7458.6	100:60
115	V _{DD2}	-464.0	-7538.6	100:60
116	RMON2	-464.0	-7842.0	100:60
117	RMON2	-464.0	-8014.2	100:60
118	Dummy2	-464.0	-8451.0	100:60
119	V _{SS2}	-399.8	-8769.0	60 100
120	V _{SS2}	-319.8	-8769.0	60 100
121	V _{SS2}	-239.8	-8769.0	60 100
122	V _{SS2}	-159.8	-8769.0	60 100
123	V _{SS2}	-79.8	-8769.0	60 100
124	V _{SS2}	0.2	-8769.0	60 100
125	V _{SS2}	80.2	-8769.0	60 100
126	V _{SS2}	160.2	-8769.0	60 100
127	V _{SS2}	240.2	-8769.0	60 100
128	V _{SS2}	320.2	-8769.0	60 100
129	Dummy3	402.0	-8642.5	80:37
130	S ₁	402.0	-8585.5	80:37
131	S ₂	402.0	-8528.5	80:37
132	S ₃	402.0	-8471.5	80:37
133	S ₄	402.0	-8414.5	80:37
134	S ₅	402.0	-8357.5	80:37
135	S ₆	402.0	-8300.5	80:37
136	S ₇	402.0	-8243.5	80:37
137	S ₈	402.0	-8186.5	80:37
138	S ₉	402.0	-8129.5	80:37
139	S ₁₀	402.0	-8072.5	80:37
140	S ₁₁	402.0	-8015.5	80:37
141	S ₁₂	402.0	-7958.5	80:37
142	S ₁₃	402.0	-7901.5	80:37
143	S ₁₄	402.0	-7844.5	80:37
144	S ₁₅	402.0	-7787.5	80:37
145	S ₁₆	402.0	-7730.5	80:37
146	S ₁₇	402.0	-7673.5	80:37
147	S ₁₈	402.0	-7616.5	80:37
148	S ₁₉	402.0	-7559.5	80:37
149	S ₂₀	402.0	-7502.5	80:37
150	S ₂₁	402.0	-7445.5	80:37
151	S ₂₂	402.0	-7388.5	80:37
152	S ₂₃	402.0	-7331.5	80:37
153	S ₂₄	402.0	-7274.5	80:37
154	S ₂₅	402.0	-7217.5	80:37
155	S ₂₆	402.0	-7160.5	80:37
156	S ₂₇	402.0	-7103.5	80:37
157	S ₂₈	402.0	-7046.5	80:37
158	S ₂₉	402.0	-6989.5	80:37
159	S ₃₀	402.0	-6932.5	80:37
160	S ₃₁	402.0	-6875.5	80:37
161	S ₃₂	402.0	-6818.5	80:37
162	S ₃₃	402.0	-6761.5	80:37
163	S ₃₄	402.0	-6704.5	80:37
164	S ₃₅	402.0	-6647.5	80:37
165	S ₃₆	402.0	-6590.5	80:37

No.	PAD Name	X [μm]	Y [μm]	Bump Size (X:Y) [μm]
166	S ₃₇	402.0	-6533.5	80:37
167	S ₃₈	402.0	-6476.5	80:37
168	S ₃₉	402.0	-6419.5	80:37
169	S ₄₀	402.0	-6362.5	80:37
170	S ₄₁	402.0	-6305.5	80:37
171	S ₄₂	402.0	-6248.5	80:37
172	S ₄₃	402.0	-6191.5	80:37
173	S ₄₄	402.0	-6134.5	80:37
174	S ₄₅	402.0	-6077.5	80:37
175	S ₄₆	402.0	-6020.5	80:37
176	S ₄₇	402.0	-5963.5	80:37
177	S ₄₈	402.0	-5906.5	80:37
178	S ₄₉	402.0	-5849.5	80:37
179	S ₅₀	402.0	-5792.5	80:37
180	S ₅₁	402.0	-5735.5	80:37
181	S ₅₂	402.0	-5678.5	80:37
182	S ₅₃	402.0	-5621.5	80:37
183	S ₅₄	402.0	-5564.5	80:37
184	S ₅₅	402.0	-5507.5	80:37
185	S ₅₆	402.0	-5450.5	80:37
186	S ₅₇	402.0	-5393.5	80:37
187	S ₅₈	402.0	-5336.5	80:37
188	S ₅₉	402.0	-5279.5	80:37
189	S ₆₀	402.0	-5222.5	80:37
190	S ₆₁	402.0	-5165.5	80:37
191	S ₆₂	402.0	-5108.5	80:37
192	S ₆₃	402.0	-5051.5	80:37
193	S ₆₄	402.0	-4994.5	80:37
194	S ₆₅	402.0	-4937.5	80:37
195	S ₆₆	402.0	-4880.5	80:37
196	S ₆₇	402.0	-4823.5	80:37
197	S ₆₈	402.0	-4766.5	80:37
198	S ₆₉	402.0	-4709.5	80:37
199	S ₇₀	402.0	-4652.5	80:37
200	S ₇₁	402.0	-4595.5	80:37
201	S ₇₂	402.0	-4538.5	80:37
202	S ₇₃	402.0	-4481.5	80:37
203	S ₇₄	402.0	-4424.5	80:37
204	S ₇₅	402.0	-4367.5	80:37
205	S ₇₆	402.0	-4310.5	80:37
206	S ₇₇	402.0	-4253.5	80:37
207	S ₇₈	402.0	-4196.5	80:37
208	S ₇₉	402.0	-4139.5	80:37
209	S ₈₀	402.0	-4082.5	80:37
210	S ₈₁	402.0	-4025.5	80:37
211	S ₈₂	402.0	-3968.5	80:37
212	S ₈₃	402.0	-3911.5	80:37
213	S ₈₄	402.0	-3854.5	80:37
214	S ₈₅	402.0	-3797.5	80:37
215	S ₈₆	402.0	-3740.5	80:37
216	S ₈₇	402.0	-3683.5	80:37
217	S ₈₈	402.0	-3626.5	80:37
218	S ₈₉	402.0	-3569.5	80:37
219	S ₉₀	402.0	-3512.5	80:37
220	S ₉₁	402.0	-3455.5	80:37

Table 3-1. Pad Layout (3/4)

No.	PAD Name	X [μm]	Y [μm]	Bump Size (X:Y) [μm]
221	S ₉₂	402.0	-3398.5	80:37
222	S ₉₃	402.0	-3341.5	80:37
223	S ₉₄	402.0	-3284.5	80:37
224	S ₉₅	402.0	-3227.5	80:37
225	S ₉₆	402.0	-3170.5	80:37
226	S ₉₇	402.0	-3113.5	80:37
227	S ₉₈	402.0	-3056.5	80:37
228	S ₉₉	402.0	-2999.5	80:37
229	S ₁₀₀	402.0	-2942.5	80:37
230	S ₁₀₁	402.0	-2885.5	80:37
231	S ₁₀₂	402.0	-2828.5	80:37
232	S ₁₀₃	402.0	-2771.5	80:37
233	S ₁₀₄	402.0	-2714.5	80:37
234	S ₁₀₅	402.0	-2657.5	80:37
235	S ₁₀₆	402.0	-2600.5	80:37
236	S ₁₀₇	402.0	-2543.5	80:37
237	S ₁₀₈	402.0	-2486.5	80:37
238	S ₁₀₉	402.0	-2429.5	80:37
239	S ₁₁₀	402.0	-2372.5	80:37
240	S ₁₁₁	402.0	-2315.5	80:37
241	S ₁₁₂	402.0	-2258.5	80:37
242	S ₁₁₃	402.0	-2201.5	80:37
243	S ₁₁₄	402.0	-2144.5	80:37
244	S ₁₁₅	402.0	-2087.5	80:37
245	S ₁₁₆	402.0	-2030.5	80:37
246	S ₁₁₇	402.0	-1973.5	80:37
247	S ₁₁₈	402.0	-1916.5	80:37
248	S ₁₁₉	402.0	-1859.5	80:37
249	S ₁₂₀	402.0	-1802.5	80:37
250	S ₁₂₁	402.0	-1745.5	80:37
251	S ₁₂₂	402.0	-1688.5	80:37
252	S ₁₂₃	402.0	-1631.5	80:37
253	S ₁₂₄	402.0	-1574.5	80:37
254	S ₁₂₅	402.0	-1517.5	80:37
255	S ₁₂₆	402.0	-1460.5	80:37
256	S ₁₂₇	402.0	-1403.5	80:37
257	S ₁₂₈	402.0	-1346.5	80:37
258	S ₁₂₉	402.0	-1289.5	80:37
259	S ₁₃₀	402.0	-1232.5	80:37
260	S ₁₃₁	402.0	-1175.5	80:37
261	S ₁₃₂	402.0	-1118.5	80:37
262	S ₁₃₃	402.0	-1061.5	80:37
263	S ₁₃₄	402.0	-1004.5	80:37
264	S ₁₃₅	402.0	-947.5	80:37
265	S ₁₃₆	402.0	-890.5	80:37
266	S ₁₃₇	402.0	-833.5	80:37
267	S ₁₃₈	402.0	-776.5	80:37
268	S ₁₃₉	402.0	-719.5	80:37
269	S ₁₄₀	402.0	-662.5	80:37
270	S ₁₄₁	402.0	-605.5	80:37
271	S ₁₄₂	402.0	-548.5	80:37
272	S ₁₄₃	402.0	-491.5	80:37
273	S ₁₄₄	402.0	-434.5	80:37
274	S ₁₄₅	402.0	-377.5	80:37
275	S ₁₄₆	402.0	-320.5	80:37

No.	PAD Name	X [μm]	Y [μm]	Bump Size (X:Y) [μm]
276	S ₁₄₇	402.0	-263.5	80:37
277	S ₁₄₈	402.0	-206.5	80:37
278	S ₁₄₉	402.0	-149.5	80:37
279	S ₁₅₀	402.0	-92.5	80:37
280	S ₁₅₁	402.0	-35.5	80:37
281	S ₁₅₂	402.0	21.5	80:37
282	S ₁₅₃	402.0	78.5	80:37
283	S ₁₅₄	402.0	135.5	80:37
284	S ₁₅₅	402.0	192.5	80:37
285	S ₁₅₆	402.0	249.5	80:37
286	S ₁₅₇	402.0	306.5	80:37
287	S ₁₅₈	402.0	363.5	80:37
288	S ₁₅₉	402.0	420.5	80:37
289	S ₁₆₀	402.0	477.5	80:37
290	S ₁₆₁	402.0	534.5	80:37
291	S ₁₆₂	402.0	591.5	80:37
292	S ₁₆₃	402.0	648.5	80:37
293	S ₁₆₄	402.0	705.5	80:37
294	S ₁₆₅	402.0	762.5	80:37
295	S ₁₆₆	402.0	819.5	80:37
296	S ₁₆₇	402.0	876.5	80:37
297	S ₁₆₈	402.0	933.5	80:37
298	S ₁₆₉	402.0	990.5	80:37
299	S ₁₇₀	402.0	1047.5	80:37
300	S ₁₇₁	402.0	1104.5	80:37
301	S ₁₇₂	402.0	1161.5	80:37
302	S ₁₇₃	402.0	1218.5	80:37
303	S ₁₇₄	402.0	1275.5	80:37
304	S ₁₇₅	402.0	1332.5	80:37
305	S ₁₇₆	402.0	1389.5	80:37
306	S ₁₇₇	402.0	1446.5	80:37
307	S ₁₇₈	402.0	1503.5	80:37
308	S ₁₇₉	402.0	1560.5	80:37
309	S ₁₈₀	402.0	1617.5	80:37
310	S ₁₈₁	402.0	1674.5	80:37
311	S ₁₈₂	402.0	1731.5	80:37
312	S ₁₈₃	402.0	1788.5	80:37
313	S ₁₈₄	402.0	1845.5	80:37
314	S ₁₈₅	402.0	1902.5	80:37
315	S ₁₈₆	402.0	1959.5	80:37
316	S ₁₈₇	402.0	2016.5	80:37
317	S ₁₈₈	402.0	2073.5	80:37
318	S ₁₈₉	402.0	2130.5	80:37
319	S ₁₉₀	402.0	2187.5	80:37
320	S ₁₉₁	402.0	2244.5	80:37
321	S ₁₉₂	402.0	2301.5	80:37
322	S ₁₉₃	402.0	2358.5	80:37
323	S ₁₉₄	402.0	2415.5	80:37
324	S ₁₉₅	402.0	2472.5	80:37
325	S ₁₉₆	402.0	2529.5	80:37
326	S ₁₉₇	402.0	2586.5	80:37
327	S ₁₉₈	402.0	2643.5	80:37
328	S ₁₉₉	402.0	2700.5	80:37
329	S ₂₀₀	402.0	2757.5	80:37
330	S ₂₀₁	402.0	2814.5	80:37

Table 3-1. Pad Layout (4/4)

No.	PAD Name	X [μm]	Y [μm]	Bump Size (X:Y) [μm]
331	S202	402.0	2871.5	80:37
332	S203	402.0	2928.5	80:37
333	S204	402.0	2985.5	80:37
334	S205	402.0	3042.5	80:37
335	S206	402.0	3099.5	80:37
336	S207	402.0	3156.5	80:37
337	S208	402.0	3213.5	80:37
338	S209	402.0	3270.5	80:37
339	S210	402.0	3327.5	80:37
340	S211	402.0	3384.5	80:37
341	S212	402.0	3441.5	80:37
342	S213	402.0	3498.5	80:37
343	S214	402.0	3555.5	80:37
344	S215	402.0	3612.5	80:37
345	S216	402.0	3669.5	80:37
346	S217	402.0	3726.5	80:37
347	S218	402.0	3783.5	80:37
348	S219	402.0	3840.5	80:37
349	S220	402.0	3897.5	80:37
350	S221	402.0	3954.5	80:37
351	S222	402.0	4011.5	80:37
352	S223	402.0	4068.5	80:37
353	S224	402.0	4125.5	80:37
354	S225	402.0	4182.5	80:37
355	S226	402.0	4239.5	80:37
356	S227	402.0	4296.5	80:37
357	S228	402.0	4353.5	80:37
358	S229	402.0	4410.5	80:37
359	S230	402.0	4467.5	80:37
360	S231	402.0	4524.5	80:37
361	S232	402.0	4581.5	80:37
362	S233	402.0	4638.5	80:37
363	S234	402.0	4695.5	80:37
364	S235	402.0	4752.5	80:37
365	S236	402.0	4809.5	80:37
366	S237	402.0	4866.5	80:37
367	S238	402.0	4923.5	80:37
368	S239	402.0	4980.5	80:37
369	S240	402.0	5037.5	80:37
370	S241	402.0	5094.5	80:37
371	S242	402.0	5151.5	80:37
372	S243	402.0	5208.5	80:37
373	S244	402.0	5265.5	80:37
374	S245	402.0	5322.5	80:37
375	S246	402.0	5379.5	80:37
376	S247	402.0	5436.5	80:37
377	S248	402.0	5493.5	80:37
378	S249	402.0	5550.5	80:37
379	S250	402.0	5607.5	80:37
380	S251	402.0	5664.5	80:37
381	S252	402.0	5721.5	80:37
382	S253	402.0	5778.5	80:37
383	S254	402.0	5835.5	80:37
384	S255	402.0	5892.5	80:37
385	S256	402.0	5949.5	80:37

No.	PAD Name	X [μm]	Y [μm]	Bump Size (X:Y) [μm]
386	S257	402.0	6006.5	80:37
387	S258	402.0	6063.5	80:37
388	S259	402.0	6120.5	80:37
389	S260	402.0	6177.5	80:37
390	S261	402.0	6234.5	80:37
391	S262	402.0	6291.5	80:37
392	S263	402.0	6348.5	80:37
393	S264	402.0	6405.5	80:37
394	S265	402.0	6462.5	80:37
395	S266	402.0	6519.5	80:37
396	S267	402.0	6576.5	80:37
397	S268	402.0	6633.5	80:37
398	S269	402.0	6690.5	80:37
399	S270	402.0	6747.5	80:37
400	S271	402.0	6804.5	80:37
401	S272	402.0	6861.5	80:37
402	S273	402.0	6918.5	80:37
403	S274	402.0	6975.5	80:37
404	S275	402.0	7032.5	80:37
405	S276	402.0	7089.5	80:37
406	S277	402.0	7146.5	80:37
407	S278	402.0	7203.5	80:37
408	S279	402.0	7260.5	80:37
409	S280	402.0	7317.5	80:37
410	S281	402.0	7374.5	80:37
411	S282	402.0	7431.5	80:37
412	S283	402.0	7488.5	80:37
413	S284	402.0	7545.5	80:37
414	S285	402.0	7602.5	80:37
415	S286	402.0	7659.5	80:37
416	S287	402.0	7716.5	80:37
417	S288	402.0	7773.5	80:37
418	S289	402.0	7830.5	80:37
419	S290	402.0	7887.5	80:37
420	S291	402.0	7944.5	80:37
421	S292	402.0	8001.5	80:37
422	S293	402.0	8058.5	80:37
423	S294	402.0	8115.5	80:37
424	S295	402.0	8172.5	80:37
425	S296	402.0	8229.5	80:37
426	S297	402.0	8286.5	80:37
427	S298	402.0	8343.5	80:37
428	S299	402.0	8400.5	80:37
429	S300	402.0	8457.5	80:37
430	Dummy4	402.0	8514.5	80:37
431	VSS2	320.2	8769.0	60:100
432	VSS2	240.2	8769.0	60:100
433	VSS2	160.2	8769.0	60:100
434	VSS2	80.2	8769.0	60:100
435	VSS2	0.2	8769.0	60:100
436	VSS2	-79.8	8769.0	60:100
437	VSS2	-159.8	8769.0	60:100
438	VSS2	-239.8	8769.0	60:100
439	VSS2	-319.8	8769.0	60:100
440	VSS2	-399.8	8769.0	60:100
441	Alignment mark 1	429.2	8779.8	
442	Alignment mark 2	429.2	-8779.8	

4. PIN FUNCTIONS

Symbol	Pin Name	Pad No.	I/O	Description															
C1 to C3	Video signal input	30 to 47	Input	Input R, G, and B video signals.															
S ₁ to S ₃₀₀	Video signal output	130 to 429	Output	Video signal output pins. Output sampled and held video signals during horizontal period.															
STHR, STHL	Cascade I/O	81 to 86, 48 to 53	I/O	Start pulse I/O pins of sample hold timing. STHR serves as an input pin and STHL, as an output pin, in the case of right shift. In the case of left shift, STHL serves as an input pin, and STHR, as an output pin.															
CLI1 to CLI3	Shift clock input	69 to 77	Input	A start pulse is read at the rising edge of CLI1. Sampling pulse SHP _n is generated at the rising edge of CLI1 through CLI3 during successive sampling, and at the rising edge of CLI1 during simultaneous sampling (for details, refer to the Timing charts in 5. FUNCTIONAL DESCRIPTION).															
INH	Inhibit input	66 to 68	Input	Selects a multiplexer and one of the two sample and hold circuits at the falling edge.															
RESET	Reset input	63 to 65	Input	Resets the select counter of the multiplexer and the selector circuit of the two sample and hold circuits when it goes high. After reset, the multiplexer is turned OFF, so sure to input one pulse of the INH signal before inputting the video signal. If the video signal is input without the INH signal, sampling is not executed.															
MP/TH	Multiplexer circuit select input (1)	54 to 56	Input	Four types of color filter arrays can be supported by combination of MP/TH and MP/1.5.															
MP/1.5	Multiplexer circuit select input (2)	57 to 59	Input	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Mode</th> <th>MP/TH</th> <th>MP/1.5</th> </tr> </thead> <tbody> <tr> <td>Vertical stripe array</td> <td>L</td> <td>L</td> </tr> <tr> <td>Single-side delta array</td> <td>L</td> <td>H</td> </tr> <tr> <td>Mosaic array</td> <td>H</td> <td>L</td> </tr> <tr> <td>Double-side delta array</td> <td>H</td> <td>H</td> </tr> </tbody> </table>	Mode	MP/TH	MP/1.5	Vertical stripe array	L	L	Single-side delta array	L	H	Mosaic array	H	L	Double-side delta array	H	H
Mode	MP/TH	MP/1.5																	
Vertical stripe array	L	L																	
Single-side delta array	L	H																	
Mosaic array	H	L																	
Double-side delta array	H	H																	
R, _/ L	Shift direction select input	60 to 62	Input	R, _/ L = H: Right shift: STHR → S ₁ → S ₃₀₀ → STHL R, _/ L = L: Left shift: STHL → S ₃₀₀ → S ₁ → STHR															
Osel	Selection of Number of outputs switching input	87 to 89	Input	Selects number of outputs. Osel = L: 288 output mode Osel = H: 300 output mode Output pins S ₁₄₅ through S ₁₅₆ are invalid in 288 output mode. The signal which is with S ₁₅₇ to S ₁₆₈ (R, _/ L = H) or S ₁₃₃ to S ₁₄₄ (R, _/ L = L) is output identically.															
RMON1, RMON2	Monitor	2, 3, 116, 117		This pin can measure the connection resistance at the time of COG mounting. RMON1 and RMON2 are each short inside IC. It does not connect with other pins inside IC.															
Dummy1 to Dummy4	Dummy	1, 118, 129, 430		No dummy pins are connected with other pins inside IC.															
V _{DD1}	Logic power supply	23 to 29, 90 to 96		3.0 to 5.5 V															
V _{DD2}	Driver power supply	4 to 15, 104 to 115		5.0 ± 0.5 V															
V _{SS1}	Logic ground	16 to 22, 97 to 103		Connect this pin to ground of system.															
V _{SS2}	Driver ground	119 to 128, 431 to 440		Connect this pin to ground of system.															
TEST	Test	78 to 80		Fix this pin to low level.															

5. FUNCTIONAL DESCRIPTION

5.1 Multiplexer Circuit

This circuit selects RGB video signals input to the C1 to C3 pins according to the pixel array of the liquid crystal panel, and outputs the signals to the S₁ through S₃₀₀ pins.

Vertical stripe array, single-/double-side delta array, or mosaic array can be selected by using the MP/TH and MP/1.5 pins.

5.1.1 Vertical stripe array mode (MP/TH = L, MP/1.5 = L)

In this mode, the relation between video signals C1 to C3, and output pins is as shown below. This mode is used to drive a panel of vertical stripe array. In this mode, the multiplexer circuit is in the through status.

Table 5-1. Relation between Video Signals C1 to C3, and Output Pins (during right shift)

Line No. (number of INHs)	RESET	INH	S ₁ to S ₃₀₀	S ₂ to S ₂₉₉	S ₃ to S ₂₉₈	S ₄ to S ₂₉₇	...	S ₂₉₉ to S ₂	S ₃₀₀ to S ₁
0	H	L	Sampling C1 (C3)	Sampling C2 (C2)	Sampling C3 (C1)	Sampling C1 (C3)	...	Sampling C2 (C2)	Sampling C3 (C1)
1	L	↓	Output C1 (C3)	Output C2 (C2)	Output C3 (C1)	Output C1 (C3)	...	Output C2 (C2)	Output C3 (C1)
2	L	↓	Output C1 (C3)	Output C2 (C2)	Output C3 (C1)	Output C1 (C3)	...	Output C2 (C2)	Output C3 (C1)
3	L	↓	Output C1 (C3)	Output C2 (C2)	Output C3 (C1)	Output C1 (C3)	...	Output C2 (C2)	Output C3 (C1)
:	:	:	:	:	:	:	...	:	:

Remark () indicates the case of left shift.

Figure 5-1. Pixel Arrangement of Vertical Stripe Array and Multiplexer Operation

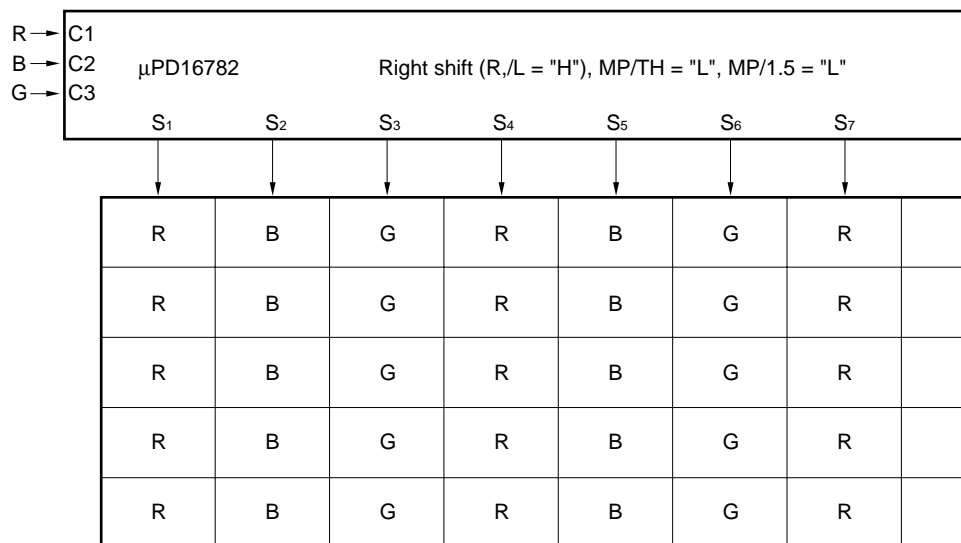
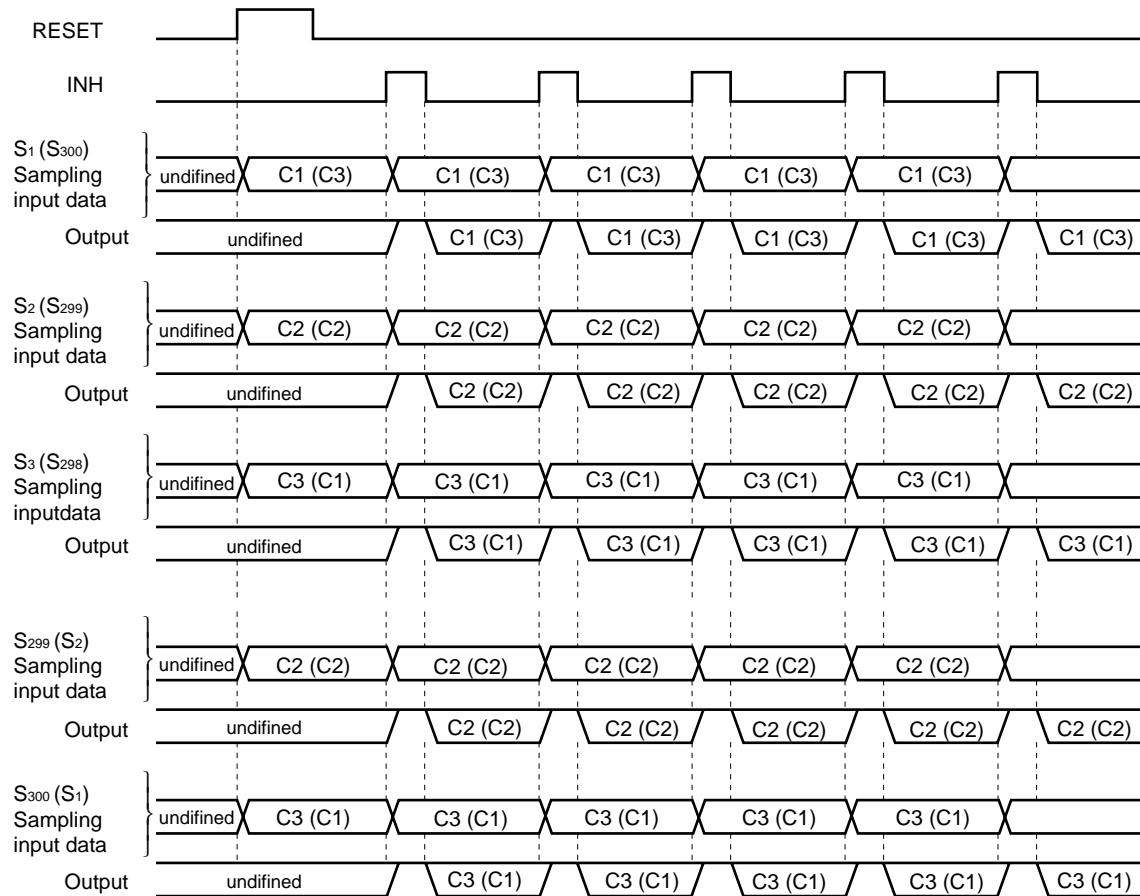


Figure 5-2. Timing Chart of Vertical Stripe Array



5.1.2 Single-side delta array mode (MP/TH = L, MP/1.5 = H)

Table 5-2. Relation between Video Signals C1 to C3, and Output Pins

Line No. (number of INHs)	RESET	INH	S ₁ to S ₃₀₀	S ₂ to S ₂₉₉	S ₃ to S ₂₉₈	S ₄ to S ₂₉₇	...	S ₂₉₉ to S ₂	S ₃₀₀ to S ₁
0	H	L	Undefined	Undefined	Undefined	Undefined	...	Undefined	Undefined
1	L	↓	Sampling C1 (C3)	Sampling C2 (C2)	Sampling C3 (C1)	Sampling C1 (C3)	...	Sampling C2 (C2)	Sampling C3 (C1)
2	L	↓	Output C1 (C3)	Output C2 (C2)	Output C3 (C1)	Output C1 (C3)	...	Output C2 (C2)	Output C3 (C1)
3	L	↓	Output C2 (C1)	Output C3 (C3)	Output C1 (C2)	Output C2 (C1)	...	Output C3 (C3)	Output C1 (C2)
4	L	↓	Output C1 (C3)	Output C2 (C2)	Output C3 (C1)	Output C1 (C3)	...	Output C2 (C2)	Output C3 (C1)
5	L	↓	Output C2 (C1)	Output C3 (C3)	Output C1 (C2)	Output C2 (C1)	...	Output C3 (C3)	Output C1 (C2)
:	:	:	:	:	:	:	...	:	:

Remark () indicates the case of left shift.

Figure 5-3. Pixel Arrangement of Single-Side Delta Array and Multiplexer Operation

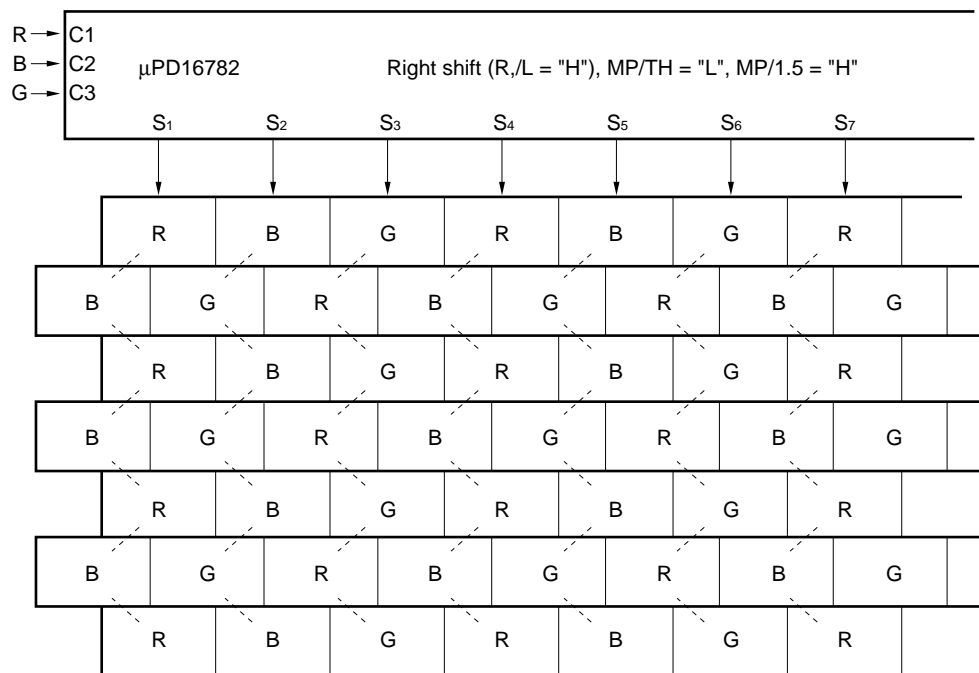


Figure 5-4. Timing Chart of Single-Side Delta Array

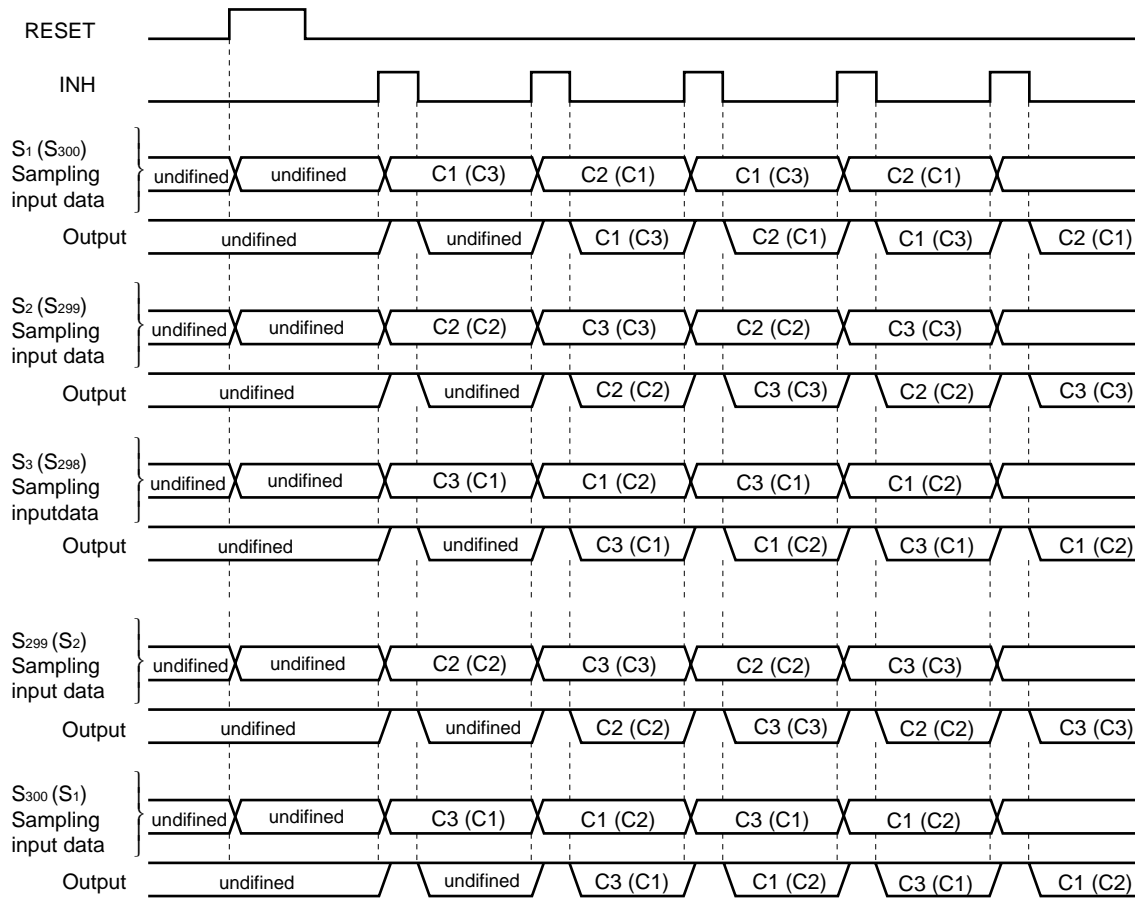
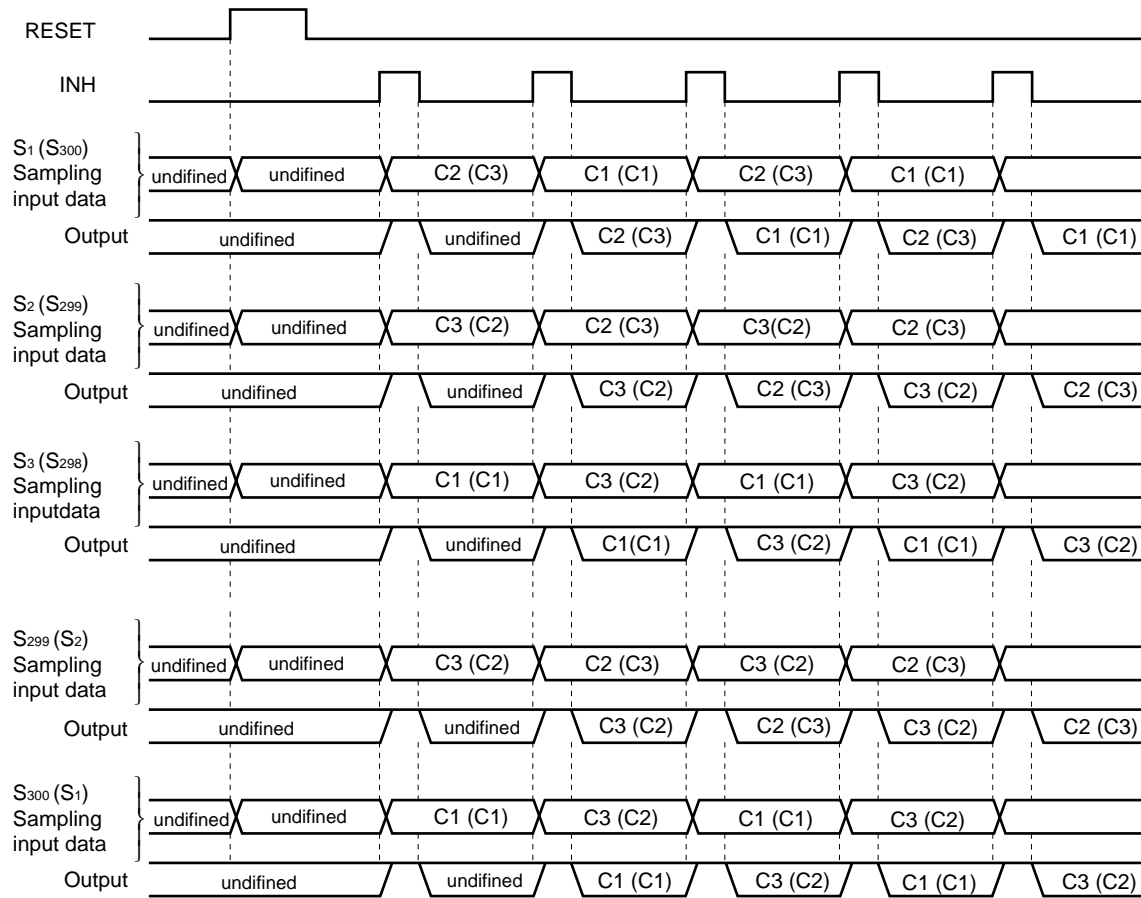


Figure 5-6. Timing Chart of Both-Sides Delta Array



5.1.4 Mosaic array mode (MP/TH = H, MP/1.5 = L)

Table 5-4. Relation between Video Signals C1 to C3, and Output Pins

Line No. (number of INHs)	RESET	INH	S ₁ to S ₃₀₀	S ₂ to S ₂₉₉	S ₃ to S ₂₉₈	S ₄ to S ₂₉₇	...	S ₂₉₉ to S ₂	S ₃₀₀ to S ₁
0	H	L	Undefined	Undefined	Undefined	Undefined	...	Undefined	Undefined
1	L	↓	Sampling C1 (C3)	Sampling C2 (C2)	Sampling C3 (C1)	Sampling C1 (C3)	...	Sampling C2 (C2)	Sampling C3 (C1)
2	L	↓	Output C1 (C3)	Output C2 (C2)	Output C3 (C1)	Output C1 (C3)	...	Output C2 (C2)	Output C3 (C1)
3	L	↓	Output C3 (C2)	Output C1 (C1)	Output C2 (C3)	Output C3 (C2)	...	Output C1 (C1)	Output C2 (C3)
4	L	↓	Output C2 (C1)	Output C3 (C3)	Output C1 (C2)	Output C2 (C1)	...	Output C3 (C3)	Output C1 (C2)
5	L	↓	Output C1 (C3)	Output C2 (C2)	Output C3 (C1)	Output C1 (C3)	...	Output C2 (C2)	Output C3 (C1)
:	:	:	:	:	:	:	...	:	:

Remark () indicates the case of left shift.

Figure 5-7. Pixel Arrangement of Mosaic Array and Multiplexer Operation

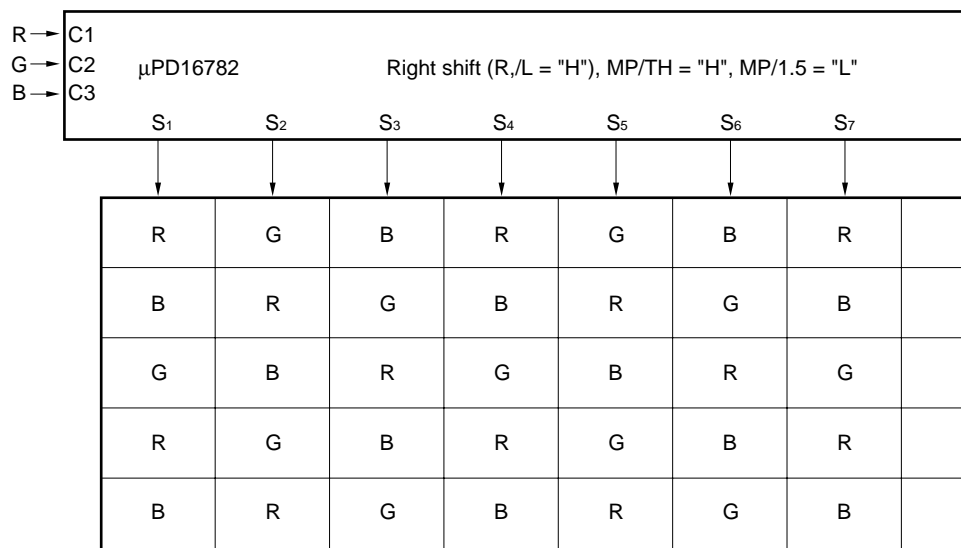
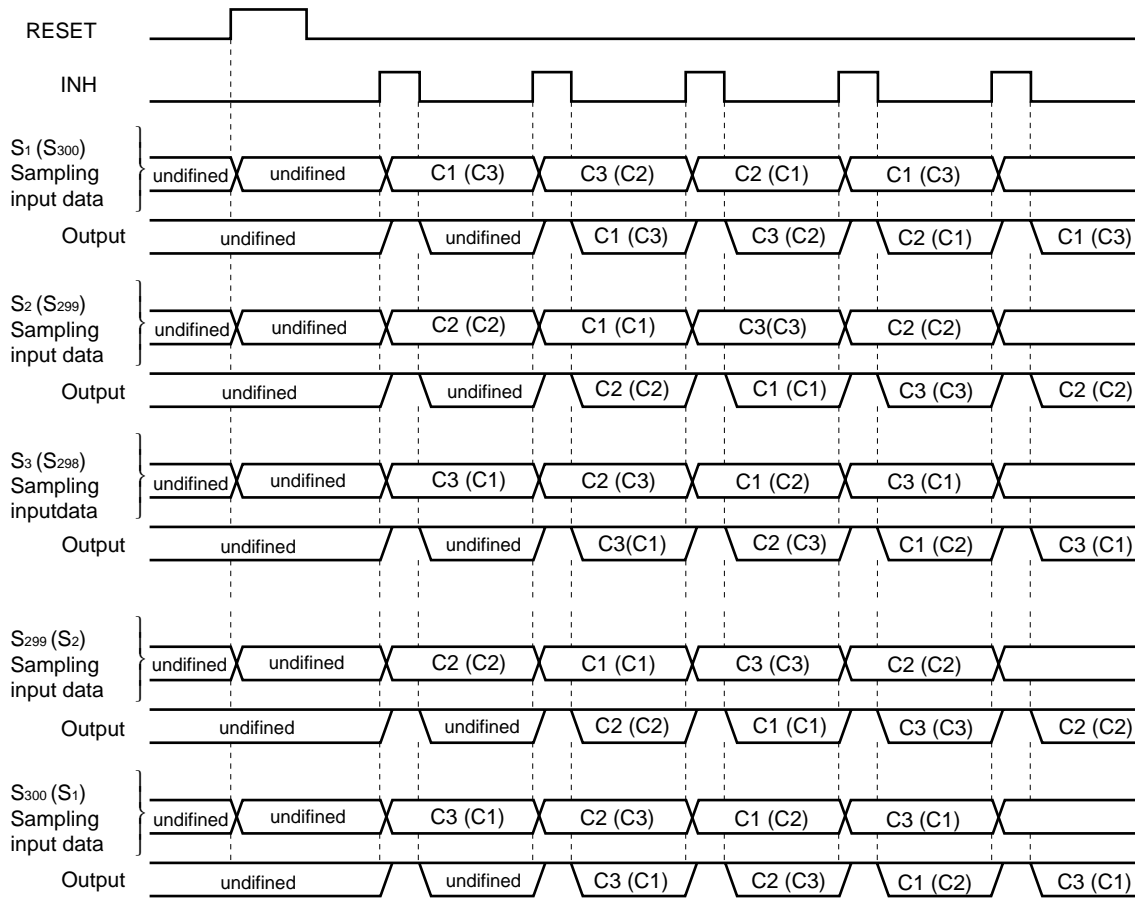
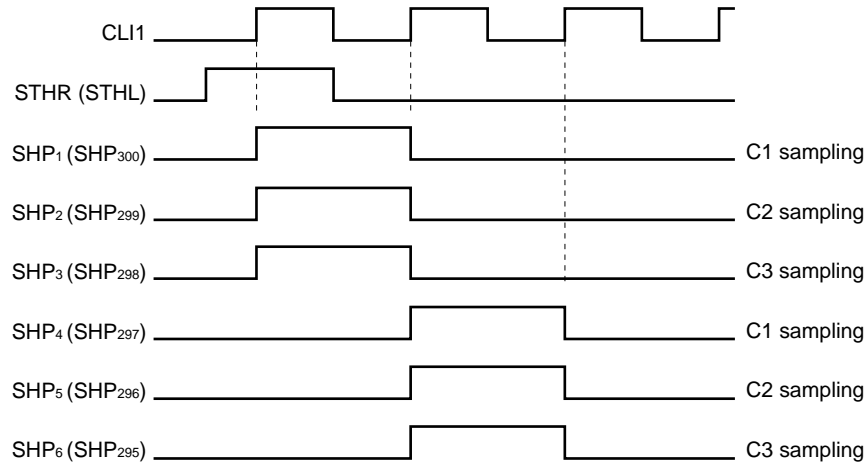


Figure 5-8. Timing Chart of Mosaic Array



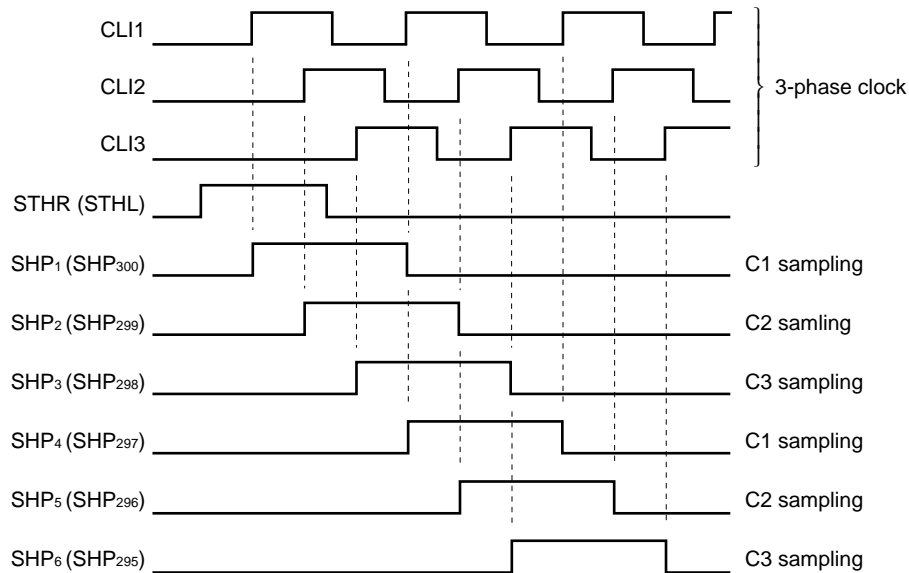
5.1.5 Relation between Shift Clock CLIn and Internal Sampling Pulse SHPn

(1) Simultaneous sampling () indicates the case of left shift.)



Remark C1 through C3 are sampled while SHPn is high level.

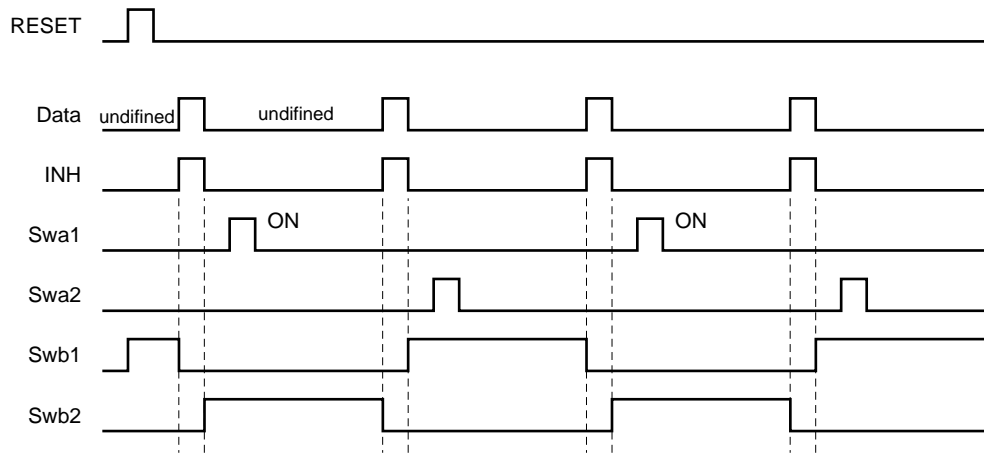
(2) Successive sampling () indicates the case of left shift.)



- Remarks 1.** Input a three-phase clock to shift clock pins CLI1 through CLI3.
2. The video signals (C1 to C3) are sampled while SHPn is high level.

5.2 Sample and Hold Circuit

The sample and hold circuit samples and holds the video input signals C1 through C3 selected by the multiplexer circuit in the timing shown below. Swa1 through Swb2 are reset by the RESET signal and change at the rising and falling edges of the INH signal (refer to 1. **BLOCK DIAGRAM.**).



5.3 Write Operation Timing

The sampled video signals are written to the LCD panel by output currents I_{VOL} and I_{VOH} via output buffer. The dynamic range is 4.3 V MIN. ($V_{DD2} = 5.0$ V).

While $INH = H$, do not stop shift clocks $CLI1$ through $CLI3$.

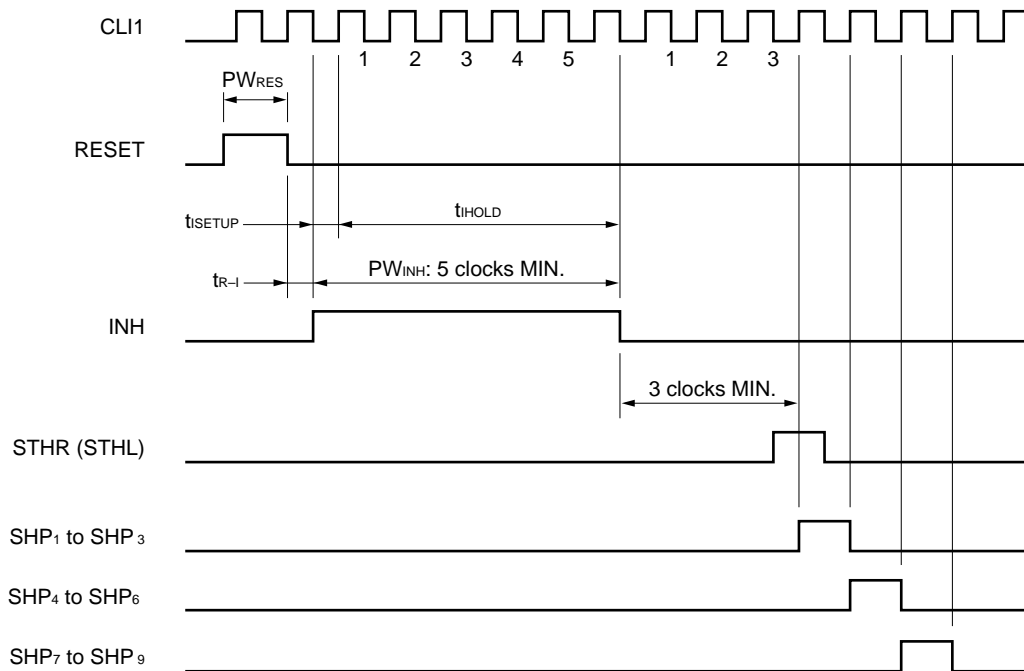
The output operation of this IC is controlled by INH signals.

$INH = Hi-Z$

$INH =$ Connected with internal circuit (switch sample and hold circuit at the falling edge.)

Therefore, performing V_{COM} inversion while $INH = L$ causes current flow to these IC output pins, which may result in malfunction. Perform V_{COM} in version during $INH = H$ (Hi-Z) and start output operation of the next line after the V_{COM} signal is stable enough to operate. Make sure to evaluate this output operation sufficiently.

- Cautions**
1. Turn on power to V_{DD1} , logic input, V_{DD2} , and video signal input in that order to prevent destruction due to latch-up, and turn off power in the reverse sequence. Observe this power sequence even during the transition period.
 2. The μPD16782 is designed to input successive signals such as chrome signals. The input band of the video signals is designed to be 9 MHz MAX. If video signals faster than that are input, display is not performed correctly.
 3. Insert a bypass capacitor of 0.1 μF between V_{DD1} and V_{SS1} and between V_{DD2} and V_{SS2} . If the power supply is not reinforced, the sampling voltage may be abnormal if the supply voltage fluctuates.
 4. Display may not be correctly performed if noise is superimposed on the start pulse pin. Therefore, be sure to input a reset signal during the vertical blanking period.
 5. Even if the start pulse width is extended by half a clock or more, sampling start timing SHP₁ is not affected, and the sampling operation is performed normally.
 6. When the multiplexer circuit is used in the vertical stripe mode, C1 to C3 are simultaneously sampled at the rising edge of SHP_n. Internally, however, only CLI1 is valid. Therefore, input a shift clock to CLI1 only. At this time, keep the CLI2 and CLI3 pins to "L".
When using the multiplexer circuit in the delta array mode or mosaic array mode, C1 to C3 are sequentially sampled. Input a three-phase clock to CLI1 through CLI3 (for the sampling timing, refer to 2. FUNCTIONAL DESCRIPTION.).
 7. The recommended timing of t_{R-1} and PW_{RES} on starting is shown below (The following timing chart shows simultaneous sampling.).
An INH pulse width of at least 5 clocks is required to reset the internal logic. Unless the INH pulse is input after reset, sampling is not performed in the correct sequence.



6. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C, V_{SS1} = 0 V)

Parameter	Symbol	Condition	Ratings	Unit
Logic supply voltage	V _{DD1}		-0.5 to +6.0	V
Driver supply voltage	V _{DD2}		-0.5 to +6.0	V
Logic input voltage	V _I		-0.5 to V _{DD1} +0.5	V
Video input voltage	V _{VI}	C1 to C3	-0.5 to V _{DD2} +0.5	V
Logic output voltage	V _{O1}		-0.5 to V _{DD1} +0.5	V
Driver output voltage	V _{O2}		-0.5 to V _{DD2} +0.5	V
Driver output current	I _{O2}		±10	mA
Operating ambient temperature	T _A		-30 to +85	°C
Storage temperature	T _{stg}		-65 to +125	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Conditions (T_A = -40 to +85°C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Logic supply voltage	V _{DD1}		3.0	3.3	5.5	V
Driver supply voltage	V _{DD2}		4.5	5.0	5.5	V
Video input voltage	V _{VI}		V _{SS2} + 0.35		V _{DD2} - 0.35	V
Driver output voltage	V _{O2}		V _{SS2} + 0.35		V _{DD2} - 0.35	V
High level Input voltage	V _{IH}		0.7 V _{DD1}		V _{DD1}	V
Low level Input voltage	V _{IL}		0		0.3 V _{DD1}	V

Electrical Characteristics (T_A = -30 to +85 °C, V_{DD1} = 3.0 to 5.5 V, V_{DD2} = 5.0 V ± 0.5 V, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit	
Maximum video signal output voltage	V _{VOH}		V _{DD2} - 0.35			V	
Minimum video signal output voltage	V _{VOL}				0.35	V	
Logic high level output voltage	V _{LOH}	STHL, STHR pins, I _{OH} = -1.0 mA	0.9 V _{DD1}			V	
Logic low level output voltage	V _{LOL}	STHL, STHR pins I _{OL} = 1.0 mA			0.1 V _{DD1}	V	
Video signal high level output current	I _{VOH}	INH = L, V _{OF} = V _{DD2} - 1.0 V V _O = V _{DD2} - 0.5 V		-0.20	-0.08	mA	
Video signal low level output current	I _{VOL}	INH = L, V _{OF} = 1.0 V, V _O = 0.5 V	0.08	0.20		mA	
Reference voltage 1	V _{REF1}	V _{DD2} = 5.0 V, T _A = 25°C, V _{VI} = 0.5 V		0.49		V	
Reference voltage 2	V _{REF2}	V _{DD2} = 5.0 V, T _A = 25°C, V _{VI} = 2.0 V		1.99		V	
Reference voltage 3	V _{REF3}	V _{DD2} = 5.0 V, T _A = 25°C, V _{VI} = 3.5 V		3.49		V	
Output voltage deviation 1	ΔV _{VO1}	V _{DD2} = 5.0 V, T _A = 25°C, V _{VI} = 0.5 V			±30	mV	
Output voltage deviation 2	ΔV _{VO2}	V _{DD2} = 5.0 V, T _A = 25°C, V _{VI} = 2.0 V			±30	mV	
Output voltage deviation 3	ΔV _{VO3}	V _{DD2} = 5.0 V, T _A = 25°C, V _{VI} = 3.5 V			±30	mV	
Logic input leakage current	I _{LL}	Logic input except Osel			±1.0	μA	
		Osel, V _I = V _{DD} = 3.3 V		90		μA	
Video input leakage current	I _{VL}				±10	μA	
Logic dynamic current consumption	I _{DD1}	f _{CLI} = 14 MHz V _{VI} = 2.0 V, no load, f _{INH} = 15.4 kHz, PW _{INH} = 5.0 μs	V _{DD1} = 3.3 ± 0.3 V			3	mA
			V _{DD1} = 5.0 ± 0.5 V				4.5
Driver dynamic current consumption	I _{DD2}	f _{CLI} = 14 MHz V _{VI} = 2.0 V, no load, f _{INH} = 15.4 kHz, PW _{INH} = 5.0 μs				12	mA

Remarks 1. V_{OF}: output applied voltage, V_O: output voltage without load

2. The reference values are typical values only. The output deviation is only guaranteed within the chip.

Switching Characteristics (T_A = -30 to +85°C, V_{DD1} = 3.0 to 5.5 V, V_{DD2} = 5.0 V ± 0.5 V, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Start pulse propagation delay time	t _{PHL}	C _L = 20 pF	10		54	ns
	t _{PLH}	C _L = 20 pF	10		54	ns
Clock frequency 1	f _{CLK 1}				15	MHz
Clock frequency 2	f _{CLK 2}	With 3-phase clock input			8	MHz
Logic input capacitance	C _{I1}	Other than STHL, STHR			15	pF
STHL, STHR input capacitance	C _{I2}	STHL, STHR			20	pF
Video input capacitance	C ₃	C1 to C3, V _{VI} = 2.0 V			50	pF

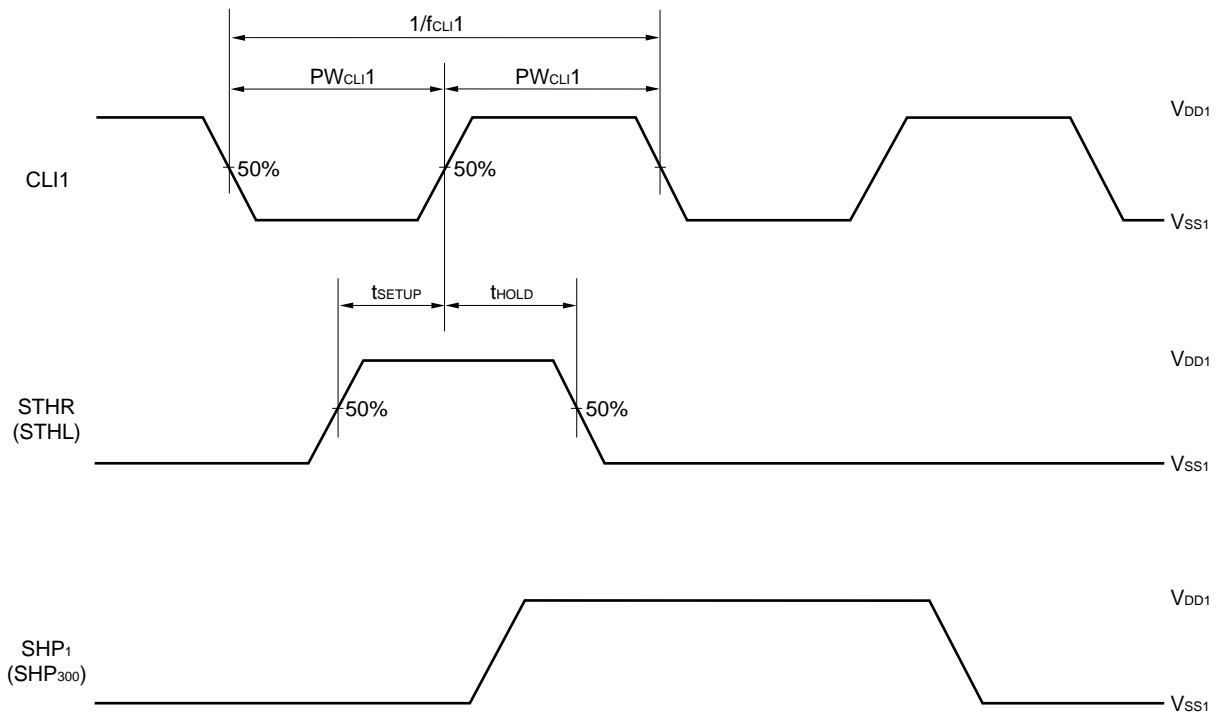
Timing Requirements (T_A = -30 to +85 °C, V_{DD1} = 3.0 to 5.5 V, V_{DD2} = 5.0 V ± 0.5 V, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock pulse width	PW _{CLI}	Duty = 50%	33			ns
Start pulse setup time	t _{SETUP}		8			ns
Start pulse hold time	t _{HOLD}		8			ns
Reset pulse width	PW _{RES}		66			ns
INH setup time	t _{SETUP}		33			ns
INH hold time	t _{HOLD}		33			ns
Reset-INH time	t _{R-I}		81			ns
INH pulse width	PW _{INH}		5			CLK

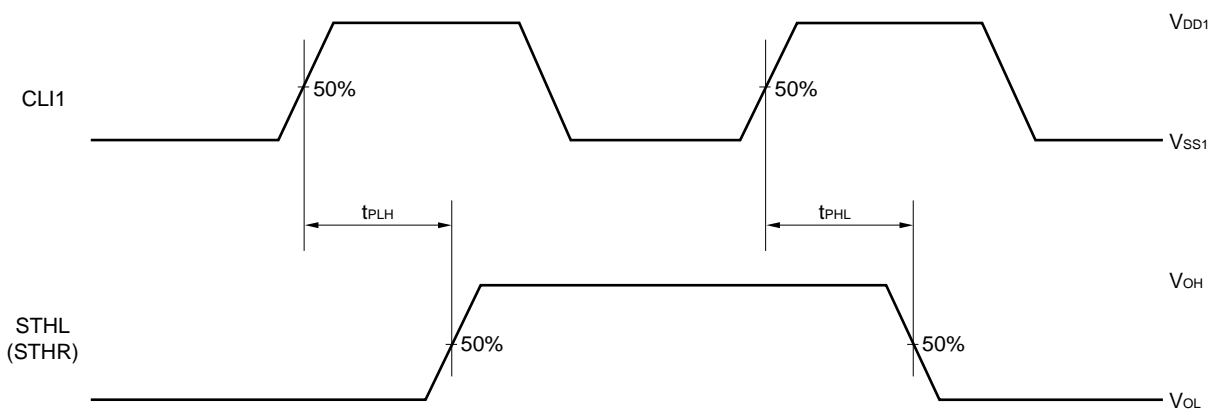
Remark Keep the rise and fall times of the logic input signals to within $t_r = t_f = 5 \text{ ns}$ (10 to 90%).
 As an example, the switching characteristic wave of CL11 is defined on the next page.

Switching Characteristic Waveform (Simultaneous/successive sampling)

Start Pulse Input Timing

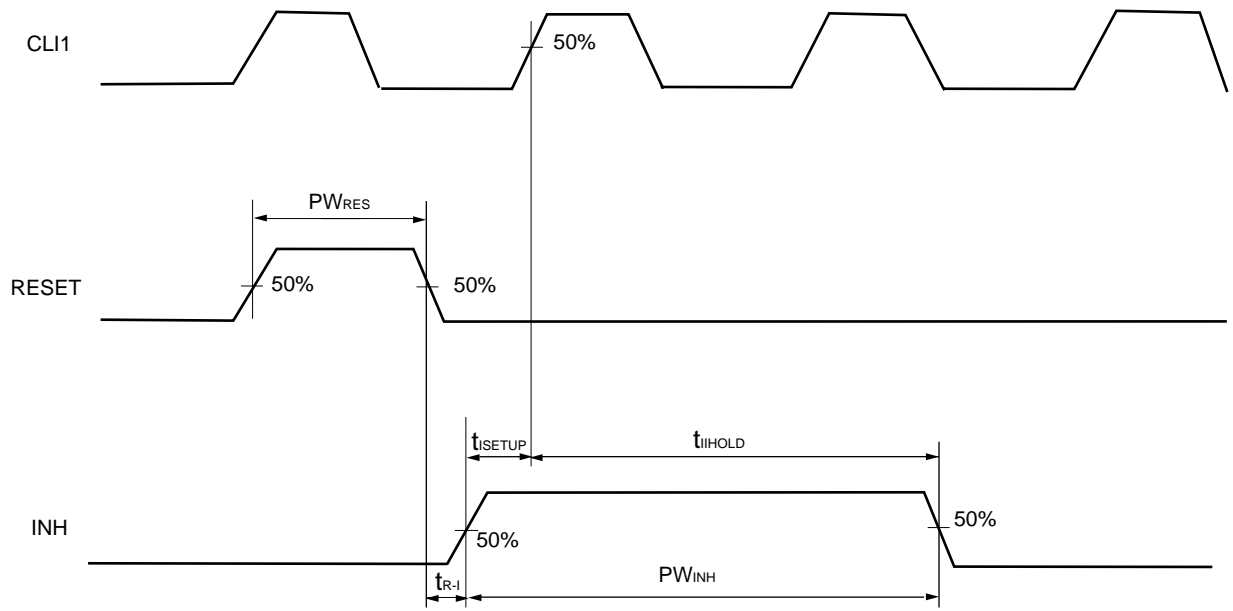


Start Pulse Output Timing



Remark The input/output timing of the start pulse is the same for simultaneous/successive sampling.

RESET INH Pulse Timing



NOTES FOR CMOS DEVICES**① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Reference Documents

NEC Semiconductor Device Reliability/Quality Control System (C10983E)

Quality Grades On NEC Semiconductor Devices (C11531E)

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