NEC

MOS INTEGRATED CIRCUIT

μPD160032A

480-OUTPUT TFT-LCD SOURCE DRIVER (COMPATIBLE WITH 256 GRAY SCALES, mini-LVDS INTERFACE SUPPORTED)

DESCRIPTION

The μPD160032A is a source driver for TFT-LCD's that supports the display of 256 gray scales and employs mini-LVDS interface. Which can realize a full-color display of 16,777,216 colors by output of 256 values γ-corrected by an internal D/A converter and 10-by-2 external power modules. Because the output dynamic range is as large as V_{SS2} + 0.2 V to V_{DD2} – 0.2 V, level inversion operation of the LCD's common electrode is rendered unnecessary. Also, to be able to deal with dot-line inversion, n-line inversion, this source driver is equipped with a built-in 8-bit D/A converter circuit whose odd output pins and even output pins respectively output gray scale voltages of differing polarity. Because of the

<R> incorporation of mini-LVDS interface, the data transfer speed has improved and the amount of wiring on the PWB (Print Wired Board) has been significantly reduced.

FEATURES

- Differential interface: CLK (1 pair), gray scale data (6 pair)
- CMOS interface: STHR(L), R,/L, STB, SB, POL, V_{sel1}, V_{sel2}, SRC, ORC, RxBIAS, H_2DOT, MODE1, MODE2
- 480 outputs
- Capable of outputting 256 values by means of 10-by-2 external power modules (20 units) and a D/A converter
- Logic power supply voltage (V_{DD1}): 2.7 to 3.6 V
- Driver power supply voltage (V_{DD2}): 10.0 to 16.5 V
- High-speed data transfer: f_{CLK} = 172 MHz MAX. (Internal data transfer speed when operating at V_{DD1} = 2.7 V)
- Output dynamic range: V_{SS2} + 0.2 V to V_{DD2} – 0.2 V
- Apply for dot-line inversion, n-line inversion
- Output voltage polarity inversion function (POL)

ORDERING INFORMATION

Part Number	Package
μPD160032AN-xxx	TCP (TAB package)
μPD160032ANL-xxx	COF (COF package)

Remark The TCP's/COF's external shape are customized. To order the required shape, please contact one of our sales representatives.

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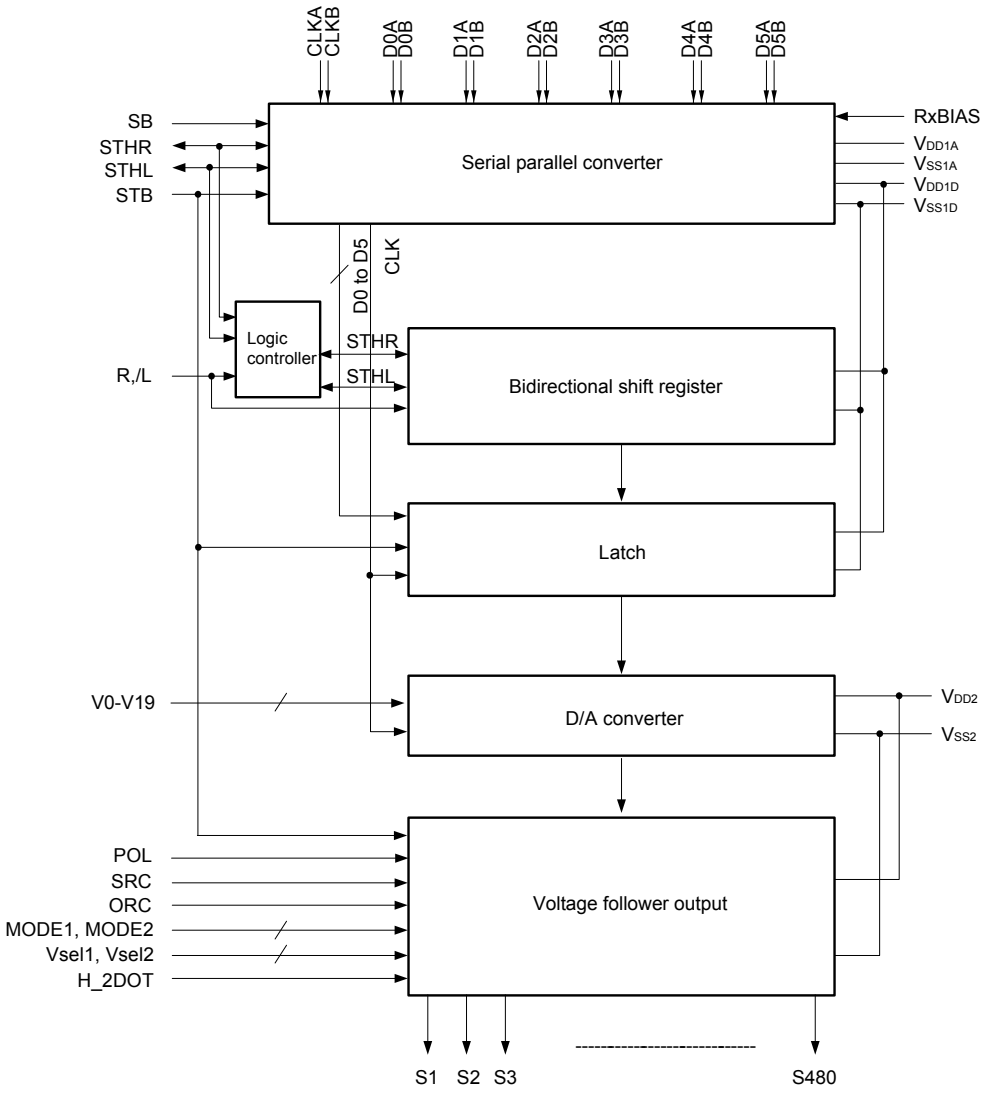
The mark <R> shows major revised points.

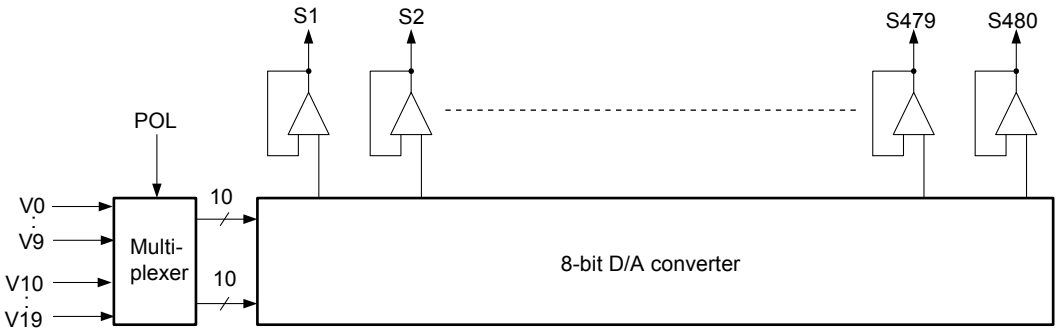
The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.

1. BLOCK DIAGRAM

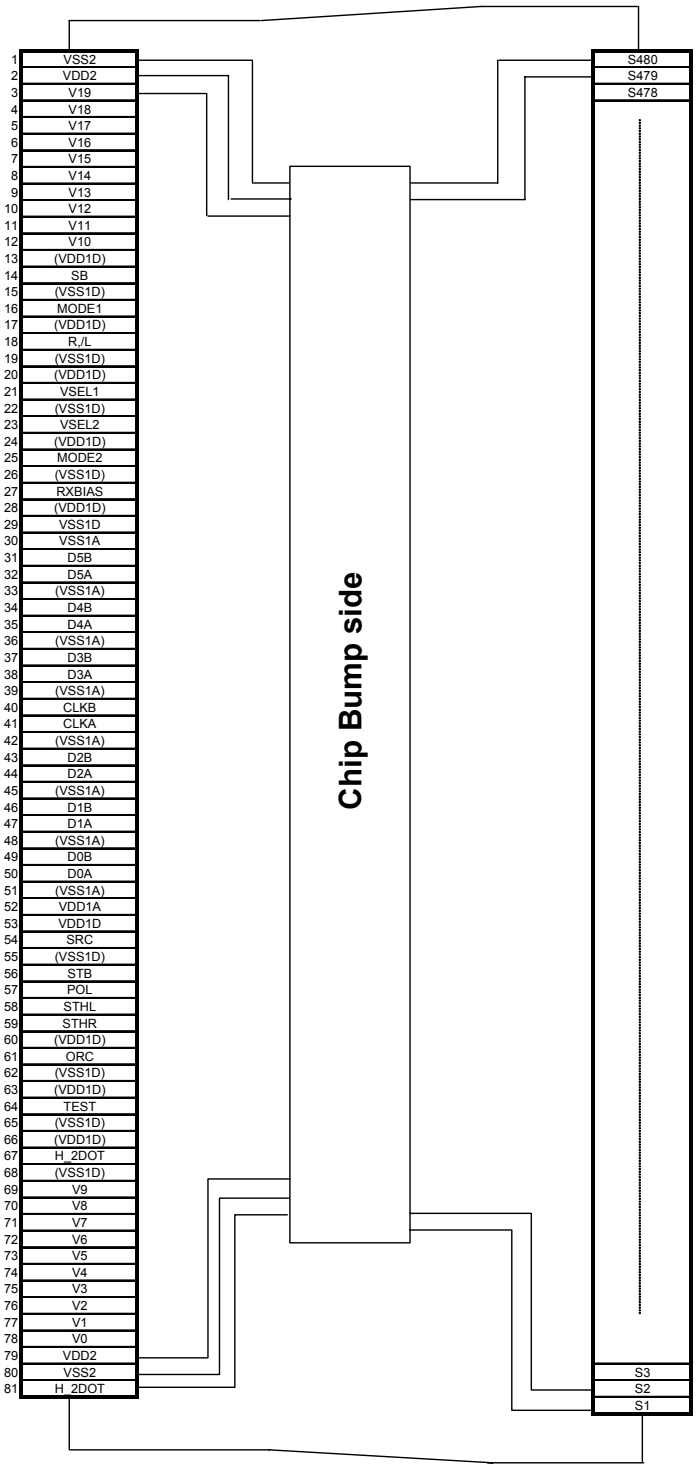


Remark /xxx indicates active low signals.

2. RELATIONSHIP BETWEEN OUTPUT CIRCUIT AND D/A CONVERTER



<R> 3. PIN CONFIGURATION (μPD160032AN-xxx: TCP (TAB package), Copper Foil Surface, Face-up)



Remark This figure does not specify the TCP package.

(V_{DD1D}) and (V_{SS1D}) are available for supply to logic input pin. Please don't use these pins for power supply pin with dynamic current. In addition, (V_{DD1D}) and (V_{SS1D}) can be left open. It recommends connecting (V_{SS1A}) to the low-pressure analog GND on PWB.

<R> 4. PIN FUNCTIONS

(1/2)

<table>
<tr><th>Pin Symbol</th><th>Pin Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>S1 to S480</td><td>Driver</td><td>Output</td><td>The D/A converted 256-gray-scale analog voltage is output.</td></tr>
<tr><td>D0A, D0B
D1A, D1B
D2A, D2B
D3A, D3B
D4A, D4B
D5A, D5B</td><td>Gray scale data</td><td>Input
(mini-LVDS)</td><td>Input pin with gray-scale data.
As for relation with SB signal, refer to Table 4–1.</td></tr>
<tr><td>CLKA,
CLKB</td><td>Shift clock</td><td>Input
(mini-LVDS)</td><td>Shift clock input.</td></tr>
<tr><td>R,/L</td><td>Shift direction control</td><td>Input
(CMOS)</td><td>The shift direction control pin of shift register. The shift directions of the shift registers are as follows.
R,/L = H (right shift): STHR input, S1→S480, STHL output
R,/L = L (left shift): STHL input, S480→S1, STHR output</td></tr>
<tr><td>STHR</td><td>Right shift start pulse</td><td rowspan="2">I/O
(CMOS)</td><td rowspan="2">This is the start pulse I/O pin when connected in cascade. Loading of display data starts when a high level is read.
For right shift, STHR is input and STHL is output.
For left shift, STHL is input and STHR is output.
For details of the timing, refer to 6. FUNCTION DESCRIPTION.</td></tr>
<tr><td>STHL</td><td>Left shift start pulse</td></tr>
<tr><td>STB</td><td>Latch</td><td>Input
(CMOS)</td><td>Change the input mode, latched the registered data and transfer to DAC at the rising edge. And supplied voltage to LCD pixel is output at falling edge.</td></tr>
<tr><td>POL</td><td>Polarity</td><td>Input
(CMOS)</td><td>Control the polarity of the driver output.
Refer to Table 4–3.</td></tr>
<tr><td>SB</td><td>Bus-line set-back</td><td>Input
(CMOS)</td><td>Change the input data order of mini-LVDS.
Refer to Table 4–1.</td></tr>
<tr><td>RxBIAS</td><td>mini-LVDS receiver bias voltage control</td><td>Input
(CMOS)</td><td>This pin controls the bias current of mini-LVDS receiver circuit.
RxBIAS = H: Normal power
RxBIAS = L: Low power</td></tr>
<tr><td>SRC</td><td>Slew-rate control</td><td>Input
(CMOS)</td><td>SRC = H: High-slew-rate mode
Internal analog current becomes higher during STB = H period.
SRC = L: Normal-slew-rate mode</td></tr>
<tr><td>ORC</td><td>Output resistance control</td><td>Input
(CMOS)</td><td>ORC = H: Low output resistance mode
ORC = L: High output resistance mode</td></tr>
<tr><td>MODE1,
MODE2</td><td>Output reset control</td><td>Input
(CMOS)</td><td>This pin controls the output reset function, in other words charge sharing.
<table>
<tr><th>MODE1</th><th>MODE2</th><th>Output Reset</th></tr>
<tr><td>L</td><td>L</td><td>Output reset invalid</td></tr>
<tr><td>L</td><td>H</td><td>Setting prohibited</td></tr>
<tr><td>H</td><td>L</td><td>Output reset only after POL changed in STB input</td></tr>
<tr><td>H</td><td>H</td><td>Output reset, every STB input</td></tr>
</table>
A setup of MODE1 = L and MODE2 = H is setting prohibited (μPD160032A becomes a test mode and does not perform normal specification operation).
Fore more details, refer to 8. OUTPUT RESET FUNCTION (MODE).</td></tr>
</table>

(2/2)

Pin Symbol	Pin Name	I/O	Description
H_2DOT	Horizontal 2 dots/1 dot inversion select	Input (CMOS)	H_2DOT = H: 2 dots inversion in horizontal H_2DOT = L: 1 dot inversion in horizontal Refer to **7. RELATIONSHIP BETWEEN POL AND H_2DOT**.
V_{sel1}	V_{DD2} select	Input (CMOS)	Select the following setting according to the voltage inputted into V_{DD2}. V_{sel1} = L: V_{DD2} = 10.0 to 12.5 V V_{sel1} = H: V_{DD2} = 12.5 to 16.5 V
V_{sel2}	Output amp. capability setting	Input (CMOS)	This pin can change the drive capability of output amplifier. V_{sel2} = L: Low power mode (drive capability: Small) V_{sel2} = H: Normal power mode (driver capability: Large)
V_0-V_{19}	γ -corrected power supplies	–	Input the γ -corrected power supplies from outside. Make sure to maintain the following relationships. During the gray scale voltage output, be sure to keep the gray scale level power supply at a constant level. $V_{DD2} - 0.2\ V \geq V_0 > V_1 > V_2 > V_3 > V_4 > V_5 > V_6 > V_7 > V_8 > V_9 \geq 0.5\ V_{DD2}$ $0.5\ V_{DD2} \geq V_{10} > V_{11} > V_{12} > V_{13} > V_{14} > V_{15} > V_{16} > V_{17} > V_{18} > V_{19} \geq V_{SS2} + 0.2\ V$
V_{DD1D}	Low-voltage logic power supply	–	2.7 to 3.6 V V_{DD1D} and V_{DD1A} should be same electric potential.
V_{DD1A}	Low-voltage analog power supply	–	2.7 to 3.6 V V_{DD1D} and V_{DD1A} should be same electric potential.
V_{DD2}	Driver power supply	–	10.0 to 16.5 V
V_{SS1D}	Low-voltage logic ground	–	Ground for internal logic circuit. Please wire V_{SS1D} and V_{SS1A} in external circuit boards.
V_{SS1A}	Low-voltage analog ground	–	Ground for internal mini-LVDS receiver circuit. Please wire V_{SS1D} and V_{SS1A} in external circuit boards.
V_{SS2}	Driver ground	–	Ground for internal high voltage circuit.

Cautions 1. The power start sequence must be [V_{DD1} →logic input →V_{DD2} & V_0-V_{19}] in that order. Reverse this sequence to shut down.

2. To stabilize the supply voltage, please be sure to insert bypass, etc capacitor between V_{DD1}-V_{SS1} and V_{DD2}-V_{SS2}. Furthermore, for increased precision of the D/A converter, insertion of a bypass capacitor is also advised between the γ-corrected power supply pins (V_0, V_1, V_2,....., V_{19}) and V_{SS2}.

Table 4–1. Function (Bus-line Set-Back)

Pin Name	SB = L	SB = H
D0A	D0(+)	D5(–)
D0B	D0(–)	D5(+)
D1A	D1(+)	D4(–)
D1B	D1(–)	D4(+)
D2A	D2(+)	D3(–)
D2B	D2(–)	D3(+)
CLKA	CLK(+)	CLK(–)
CLKB	CLK(–)	CLK(+)
D3A	D3(+)	D2(–)
D3B	D3(–)	D2(+)
D4A	D4(+)	D1(–)
D4B	D4(–)	D1(+)
D5A	D5(+)	D0(–)
D5B	D5(–)	D0(+)

Remark Suffix "+" indicates positive potential and "–" indicates negative potential at each differential signal input pair.

Table 4–2. Function (R,/L and STHR(L))

R,/L	STHR	STHL	Shift Direction
H (Right shift)	IN	OUT	S1 → S480
L (Left shift)	OUT	IN	S480 → S1

<R>

Table 4–3. Function (POL and Reference GAMMA) (H_2DOT = L)

POL	ODD numbered output	EVEN numbered output
H	V_{10}-V_{19}	V_0-V_9
L	V_0-V_9	V_{10}-V_{19}

Table 4–4. Function (POL and Reference GAMMA) (H_2DOT = H)

POL	S4n, S4n–3 numbered output	S4n–1, S4n–2 numbered output
H	V_{10}-V_{19}	V_0-V_9
L	V_0-V_9	V_{10}-V_{19}

5. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT VOLTAGE VALUE

μPD160032A incorporates 8-bit D/A converter whose odd output pins and even output pins output respectively gray scale voltages of differing polarity with respect to the LCD's counter electrode (common electrode) voltage. The D/A converter consists of ladder resistors and switches.

Figure 5–1 shows the relationship between the driving voltages such as liquid-crystal driving voltages V_{DD2}, V_{SS2} and common electrode potential V_{COM}, and γ-corrected voltages V_0 to V_{19} and the input data. Be sure to maintain the voltage relationships of below.

$$V_{DD2} - 0.2\ V \geq V_0 > V_1 > V_2 > V_3 > V_4 > V_5 > V_6 > V_7 > V_8 > V_9 \geq 0.5\ V_{DD2}$$

$$0.5\ V_{DD2} \geq V_{10} > V_{11} > V_{12} > V_{13} > V_{14} > V_{15} > V_{16} > V_{17} > V_{18} > V_{19} \geq V_{SS2} + 0.2\ V$$

Figures 5–2 and 5–3 show the relationship between the input data and the output data.

Figure 5–1. Relationship between Input Data and γ-corrected Power Supplies

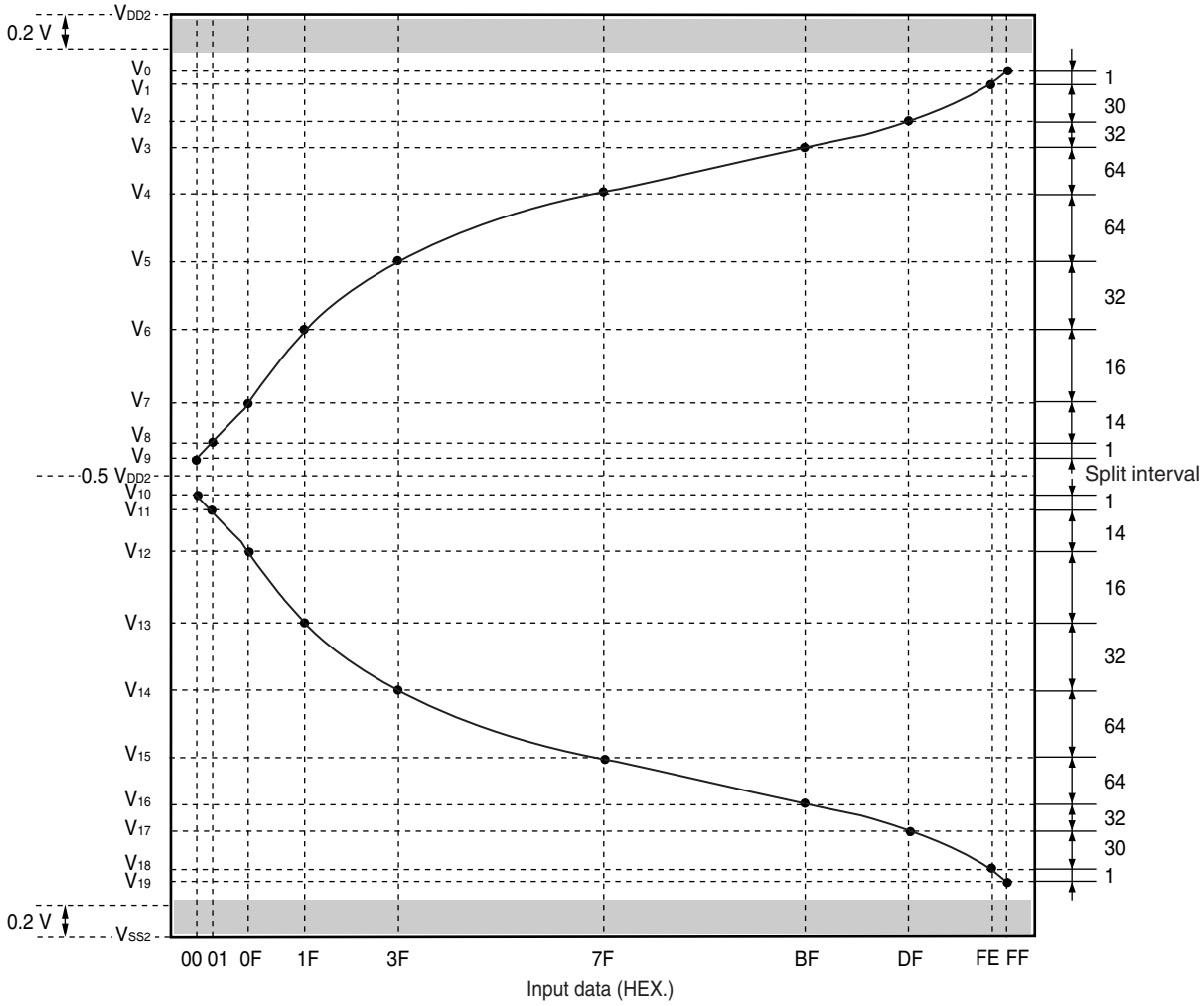
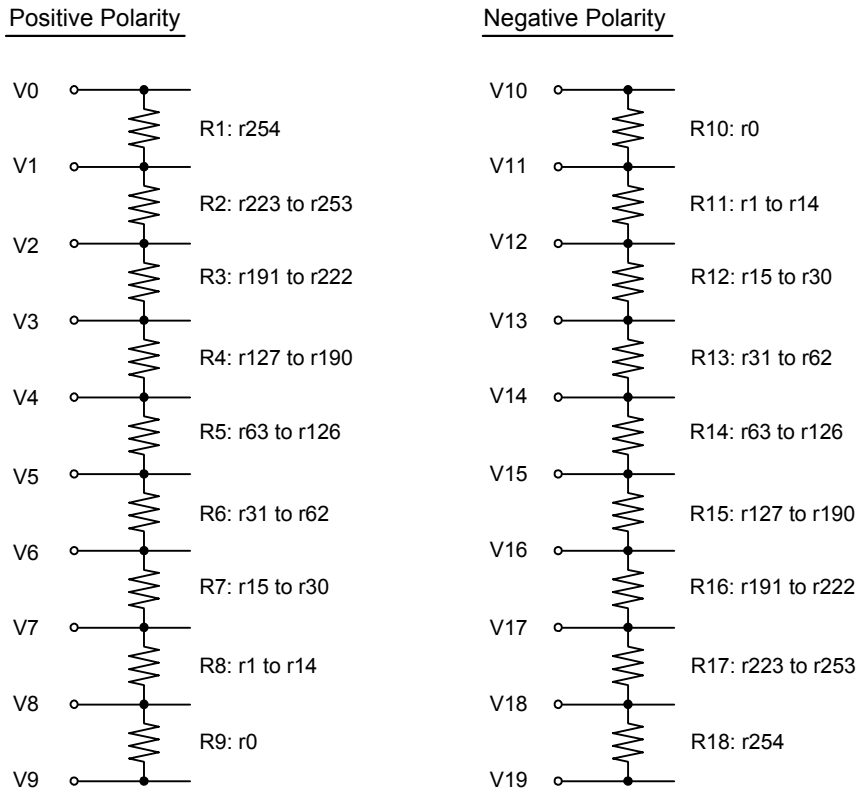


Figure 5–2. γ- corrected Power Supply and Ladder Resistors Ratio (1/2)



Caution It is necessary to supply a reference voltage at least to V0, V9, V10 and V19.
Other pins can be open, but this is a tradeoff with a display quality. Therefore, when using some of these pins open-state, be sure to sufficiently evaluate the display quality.

Figure 5–2. γ- corrected Power Supply and Ladder Resistors Ratio (2/2)

r n	Value (ohm)	r ratio1	r ratio2	r n	Value (ohm)	r ratio1	r ratio2	r n	Value (ohm)	r ratio1	r ratio2	r n	Value (ohm)	r ratio1	r ratio2
r0	10	1.00	0.0007	r64	43	4.42	0.00309	r128	35	3.58	0.00251	r192	44	4.52	0.00316
r1	24	2.49	0.0017	r65	43	4.42	0.00309	r129	35	3.61	0.00253	r193	46	4.67	0.00327
r2	47	4.78	0.0033	r66	43	4.42	0.00309	r130	35	3.61	0.00253	r194	47	4.82	0.00337
r3	70	7.13	0.0050	r67	43	4.42	0.00309	r131	35	3.61	0.00253	r195	48	4.92	0.00344
r4	89	9.13	0.0064	r68	43	4.42	0.00309	r132	35	3.61	0.00253	r196	49	5.02	0.00351
r5	104	10.62	0.00743	r69	43	4.42	0.00309	r133	35	3.61	0.00253	r197	50	5.12	0.00358
r6	112	11.42	0.00799	r70	43	4.42	0.00309	r134	35	3.61	0.00253	r198	51	5.22	0.00365
r7	112	11.42	0.00799	r71	43	4.42	0.00309	r135	36	3.63	0.00254	r199	52	5.32	0.00372
r8	109	11.12	0.00778	r72	43	4.42	0.00309	r136	36	3.65	0.00256	r200	53	5.37	0.00376
r9	104	10.62	0.00743	r73	43	4.42	0.00309	r137	36	3.67	0.00257	r201	53	5.37	0.00376
r10	100	10.22	0.00716	r74	43	4.42	0.00309	r138	36	3.69	0.00259	r202	53	5.37	0.00376
r11	97	9.92	0.00695	r75	43	4.42	0.00309	r139	36	3.71	0.00260	r203	53	5.37	0.00376
r12	95	9.72	0.00681	r76	43	4.42	0.00309	r140	37	3.73	0.00261	r204	53	5.37	0.00376
r13	94	9.62	0.00674	r77	43	4.42	0.00309	r141	37	3.75	0.00263	r205	53	5.42	0.00379
r14	95	9.72	0.00681	r78	43	4.41	0.00308	r142	37	3.77	0.00264	r206	54	5.47	0.00383
r15	96	9.82	0.00688	r79	43	4.36	0.00305	r143	37	3.79	0.00266	r207	54	5.52	0.00386
r16	91	9.28	0.00650	r80	42	4.31	0.00301	r144	37	3.81	0.00267	r208	55	5.57	0.00390
r17	83	8.43	0.00590	r81	42	4.26	0.00298	r145	38	3.83	0.00268	r209	55	5.62	0.00393
r18	75	7.69	0.00538	r82	41	4.21	0.00294	r146	38	3.85	0.00270	r210	56	5.72	0.00400
r19	71	7.29	0.00510	r83	41	4.16	0.00291	r147	38	3.87	0.00271	r211	57	5.82	0.00407
r20	70	7.12	0.00498	r84	40	4.11	0.00288	r148	38	3.89	0.00273	r212	58	5.92	0.00414
r21	71	7.27	0.00509	r85	40	4.06	0.00284	r149	38	3.91	0.00274	r213	59	6.01	0.00421
r22	73	7.47	0.00523	r86	39	4.01	0.00281	r150	39	3.93	0.00275	r214	60	6.11	0.00428
r23	75	7.62	0.00533	r87	39	3.98	0.00278	r151	39	3.95	0.00277	r215	61	6.21	0.00435
r24	75	7.62	0.00533	r88	39	3.95	0.00276	r152	39	3.97	0.00278	r216	62	6.31	0.00442
r25	73	7.42	0.00519	r89	38	3.92	0.00274	r153	39	3.99	0.00280	r217	63	6.41	0.00449
r26	70	7.12	0.00498	r90	38	3.89	0.00272	r154	39	4.01	0.00281	r218	64	6.51	0.00456
r27	67	6.80	0.00476	r91	38	3.86	0.00270	r155	40	4.03	0.00282	r219	64	6.58	0.00461
r28	65	6.58	0.00461	r92	38	3.83	0.00268	r156	40	4.05	0.00284	r220	64	6.58	0.00461
r29	65	6.58	0.00461	r93	37	3.81	0.00267	r157	40	4.07	0.00285	r221	64	6.58	0.00461
r30	65	6.58	0.00461	r94	37	3.79	0.00265	r158	40	4.08	0.00286	r222	64	6.58	0.00461
r31	65	6.58	0.00461	r95	37	3.77	0.00264	r159	40	4.09	0.00286	r223	64	6.58	0.00461
r32	64	6.48	0.00454	r96	37	3.75	0.00262	r160	40	4.10	0.00287	r224	64	6.58	0.00461
r33	62	6.28	0.00440	r97	37	3.73	0.00261	r161	40	4.11	0.00288	r225	65	6.59	0.00461
r34	59	6.06	0.00425	r98	36	3.71	0.00260	r162	40	4.12	0.00289	r226	66	6.69	0.00468
r35	57	5.85	0.00409	r99	36	3.69	0.00258	r163	40	4.13	0.00289	r227	68	6.89	0.00482
r36	55	5.65	0.00395	r100	36	3.67	0.00257	r164	41	4.14	0.00290	r228	70	7.14	0.00500
r37	54	5.52	0.00386	r101	36	3.65	0.00255	r165	41	4.15	0.00291	r229	73	7.44	0.00521
r38	53	5.42	0.00379	r102	36	3.63	0.00254	r166	41	4.16	0.00291	r230	76	7.73	0.00541
r39	53	5.37	0.00376	r103	35	3.60	0.00252	r167	41	4.17	0.00292	r231	79	8.03	0.00562
r40	52	5.35	0.00374	r104	35	3.57	0.00250	r168	41	4.18	0.00293	r232	81	8.28	0.00580
r41	52	5.33	0.00373	r105	35	3.54	0.00248	r169	41	4.19	0.00293	r233	83	8.49	0.00594
r42	52	5.31	0.00372	r106	34	3.51	0.00246	r170	41	4.20	0.00294	r234	84	8.59	0.00601
r43	52	5.29	0.00370	r107	34	3.48	0.00244	r171	41	4.21	0.00295	r235	85	8.69	0.00608
r44	52	5.27	0.00369	r108	34	3.45	0.00242	r172	41	4.22	0.00296	r236	86	8.79	0.00615
r45	51	5.24	0.00367	r109	34	3.42	0.00239	r173	41	4.23	0.00296	r237	87	8.89	0.00622
r46	51	5.18	0.00362	r110	33	3.39	0.00237	r174	42	4.24	0.00297	r238	89	9.09	0.00636
r47	50	5.12	0.00358	r111	33	3.36	0.00235	r175	42	4.25	0.00298	r239	91	9.29	0.00650
r48	49	5.04	0.00353	r112	33	3.33	0.00233	r176	42	4.26	0.00298	r240	93	9.49	0.00664
r49	49	4.96	0.00347	r113	32	3.30	0.00231	r177	42	4.27	0.00299	r241	96	9.79	0.00685
r50	48	4.88	0.00342	r114	32	3.27	0.00229	r178	42	4.28	0.00300	r242	100	10.18	0.00713
r51	47	4.82	0.00337	r115	32	3.24	0.00227	r179	42	4.29	0.00300	r243	105	10.68	0.00748
r52	47	4.76	0.00333	r116	31	3.21	0.00225	r180	42	4.30	0.00301	r244	111	11.28	0.00790
r53	46	4.70	0.00329	r117	31	3.18	0.00223	r181	42	4.31	0.00302	r245	116	11.88	0.00831
r54	46	4.65	0.00326	r118	31	3.15	0.00221	r182	42	4.32	0.00303	r246	122	12.48	0.00873
r55	45	4.60	0.00322	r119	31	3.12	0.00218	r183	42	4.33	0.00303	r247	128	13.07	0.00915
r56	45	4.57	0.00320	r120	30	3.09	0.00216	r184	43	4.34	0.00304	r248	133	13.57	0.00950
r57	44	4.54	0.00318	r121	30	3.06	0.00214	r185	43	4.35	0.00305	r249	138	14.07	0.0098
r58	44	4.51	0.00316	r122	30	3.06	0.00214	r186	43	4.36	0.00305	r250	143	14.57	0.0102
r59	44	4.48	0.00314	r123	30	3.06	0.00214	r187	43	4.38	0.00307	r251	149	15.16	0.0106
r60	44	4.45	0.00312	r124	30	3.11	0.00218	r188	43	4.40	0.00308	r252	156	15.96	0.0112
r61	43	4.42	0.00309	r125	31	3.21	0.00225	r189	43	4.42	0.00309	r253	169	17.26	0.0121
r62	43	4.42	0.00309	r126	33	3.34	0.00234	r190	43	4.42	0.00309	r254	192	19.55	0.0137
r63	43	4.42	0.00309	r127	34	3.47	0.00243	r191	43	4.42	0.00309	r total	14000	1428.57	1.00

Minimum Resistance Value (ohm): 10

Total Resistance Value (ohm): 14,000

Remark The resistance ratio1 is a relative ratio in the case of setting the minimum unit resistance value to 1.
The resistance ratio2 is a relative ratio in the case of setting the total resistance value to 1.

Figure 5–3. Relationship between Input Data and Output Voltage/Positive Side (1/2)

(Output voltage) $V_{DD2} - 0.2\ V \geq V_0 > V_1 > V_2 > V_3 > V_4 > V_5 > V_6 > V_7 > V_8 > V_9 \geq 0.5\ V_{DD2}$

Data	Output Voltage		Data	Output Voltage	
00H	V0'	V9	40H	V64'	V5+(V4-V5) X 43 / 2389
01H	V1'	V8	41H	V65'	V5+(V4-V5) X 87 / 2389
02H	V2'	V8+(V7-V8) X 24 / 1254	42H	V66'	V5+(V4-V5) X 130 / 2389
03H	V3'	V8+(V7-V8) X 71 / 1254	43H	V67'	V5+(V4-V5) X 173 / 2389
04H	V4'	V8+(V7-V8) X 141 / 1254	44H	V68'	V5+(V4-V5) X 217 / 2389
05H	V5'	V8+(V7-V8) X 231 / 1254	45H	V69'	V5+(V4-V5) X 260 / 2389
06H	V6'	V8+(V7-V8) X 335 / 1254	46H	V70'	V5+(V4-V5) X 303 / 2389
07H	V7'	V8+(V7-V8) X 447 / 1254	47H	V71'	V5+(V4-V5) X 347 / 2389
08H	V8'	V8+(V7-V8) X 558 / 1254	48H	V72'	V5+(V4-V5) X 390 / 2389
09H	V9'	V8+(V7-V8) X 667 / 1254	49H	V73'	V5+(V4-V5) X 433 / 2389
0AH	V10'	V8+(V7-V8) X 772 / 1254	4AH	V74'	V5+(V4-V5) X 477 / 2389
0BH	V11'	V8+(V7-V8) X 872 / 1254	4BH	V75'	V5+(V4-V5) X 520 / 2389
0CH	V12'	V8+(V7-V8) X 969 / 1254	4CH	V76'	V5+(V4-V5) X 563 / 2389
0DH	V13'	V8+(V7-V8) X 1064 / 1254	4DH	V77'	V5+(V4-V5) X 607 / 2389
0EH	V14'	V8+(V7-V8) X 1159 / 1254	4EH	V78'	V5+(V4-V5) X 650 / 2389
0FH	V15'	V7	4FH	V79'	V5+(V4-V5) X 693 / 2389
10H	V16'	V7+(V6-V7) X 96 / 1183	50H	V80'	V5+(V4-V5) X 736 / 2389
11H	V17'	V7+(V6-V7) X 187 / 1183	51H	V81'	V5+(V4-V5) X 778 / 2389
12H	V18'	V7+(V6-V7) X 270 / 1183	52H	V82'	V5+(V4-V5) X 820 / 2389
13H	V19'	V7+(V6-V7) X 345 / 1183	53H	V83'	V5+(V4-V5) X 861 / 2389
14H	V20'	V7+(V6-V7) X 417 / 1183	54H	V84'	V5+(V4-V5) X 902 / 2389
15H	V21'	V7+(V6-V7) X 486 / 1183	55H	V85'	V5+(V4-V5) X 942 / 2389
16H	V22'	V7+(V6-V7) X 558 / 1183	56H	V86'	V5+(V4-V5) X 982 / 2389
17H	V23'	V7+(V6-V7) X 631 / 1183	57H	V87'	V5+(V4-V5) X 1021 / 2389
18H	V24'	V7+(V6-V7) X 706 / 1183	58H	V88'	V5+(V4-V5) X 1060 / 2389
19H	V25'	V7+(V6-V7) X 780 / 1183	59H	V89'	V5+(V4-V5) X 1099 / 2389
1AH	V26'	V7+(V6-V7) X 853 / 1183	5AH	V90'	V5+(V4-V5) X 1137 / 2389
1BH	V27'	V7+(V6-V7) X 923 / 1183	5BH	V91'	V5+(V4-V5) X 1175 / 2389
1CH	V28'	V7+(V6-V7) X 989 / 1183	5CH	V92'	V5+(V4-V5) X 1213 / 2389
1DH	V29'	V7+(V6-V7) X 1054 / 1183	5DH	V93'	V5+(V4-V5) X 1250 / 2389
1EH	V30'	V7+(V6-V7) X 1118 / 1183	5EH	V94'	V5+(V4-V5) X 1288 / 2389
1FH	V31'	V6	5FH	V95'	V5+(V4-V5) X 1325 / 2389
20H	V32'	V6+(V5-V6) X 65 / 1618	60H	V96'	V5+(V4-V5) X 1362 / 2389
21H	V33'	V6+(V5-V6) X 128 / 1618	61H	V97'	V5+(V4-V5) X 1399 / 2389
22H	V34'	V6+(V5-V6) X 190 / 1618	62H	V98'	V5+(V4-V5) X 1435 / 2389
23H	V35'	V6+(V5-V6) X 249 / 1618	63H	V99'	V5+(V4-V5) X 1471 / 2389
24H	V36'	V6+(V5-V6) X 306 / 1618	64H	V100'	V5+(V4-V5) X 1508 / 2389
25H	V37'	V6+(V5-V6) X 362 / 1618	65H	V101'	V5+(V4-V5) X 1544 / 2389
26H	V38'	V6+(V5-V6) X 416 / 1618	66H	V102'	V5+(V4-V5) X 1579 / 2389
27H	V39'	V6+(V5-V6) X 469 / 1618	67H	V103'	V5+(V4-V5) X 1615 / 2389
28H	V40'	V6+(V5-V6) X 521 / 1618	68H	V104'	V5+(V4-V5) X 1650 / 2389
29H	V41'	V6+(V5-V6) X 574 / 1618	69H	V105'	V5+(V4-V5) X 1685 / 2389
2AH	V42'	V6+(V5-V6) X 626 / 1618	6AH	V106'	V5+(V4-V5) X 1720 / 2389
2BH	V43'	V6+(V5-V6) X 678 / 1618	6BH	V107'	V5+(V4-V5) X 1754 / 2389
2CH	V44'	V6+(V5-V6) X 730 / 1618	6CH	V108'	V5+(V4-V5) X 1788 / 2389
2DH	V45'	V6+(V5-V6) X 781 / 1618	6DH	V109'	V5+(V4-V5) X 1822 / 2389
2EH	V46'	V6+(V5-V6) X 833 / 1618	6EH	V110'	V5+(V4-V5) X 1856 / 2389
2FH	V47'	V6+(V5-V6) X 884 / 1618	6FH	V111'	V5+(V4-V5) X 1889 / 2389
30H	V48'	V6+(V5-V6) X 934 / 1618	70H	V112'	V5+(V4-V5) X 1922 / 2389
31H	V49'	V6+(V5-V6) X 983 / 1618	71H	V113'	V5+(V4-V5) X 1955 / 2389
32H	V50'	V6+(V5-V6) X 1032 / 1618	72H	V114'	V5+(V4-V5) X 1987 / 2389
33H	V51'	V6+(V5-V6) X 1080 / 1618	73H	V115'	V5+(V4-V5) X 2019 / 2389
34H	V52'	V6+(V5-V6) X 1127 / 1618	74H	V116'	V5+(V4-V5) X 2051 / 2389
35H	V53'	V6+(V5-V6) X 1173 / 1618	75H	V117'	V5+(V4-V5) X 2082 / 2389
36H	V54'	V6+(V5-V6) X 1219 / 1618	76H	V118'	V5+(V4-V5) X 2113 / 2389
37H	V55'	V6+(V5-V6) X 1265 / 1618	77H	V119'	V5+(V4-V5) X 2144 / 2389
38H	V56'	V6+(V5-V6) X 1310 / 1618	78H	V120'	V5+(V4-V5) X 2175 / 2389
39H	V57'	V6+(V5-V6) X 1355 / 1618	79H	V121'	V5+(V4-V5) X 2205 / 2389
3AH	V58'	V6+(V5-V6) X 1399 / 1618	7AH	V122'	V5+(V4-V5) X 2235 / 2389
3BH	V59'	V6+(V5-V6) X 1444 / 1618	7BH	V123'	V5+(V4-V5) X 2265 / 2389
3CH	V60'	V6+(V5-V6) X 1488 / 1618	7CH	V124'	V5+(V4-V5) X 2295 / 2389
3DH	V61'	V6+(V5-V6) X 1531 / 1618	7DH	V125'	V5+(V4-V5) X 2326 / 2389
3EH	V62'	V6+(V5-V6) X 1574 / 1618	7EH	V126'	V5+(V4-V5) X 2357 / 2389
3FH	V63'	V5	7FH	V127'	V4

Figure 5–3. Relationship between Input Data and Output Voltage/Positive Side (2/2)

(Output voltage) V_{DD2} – 0.2 V ≥ V_0 > V_1 > V_2 > V_3 > V_4 > V_5 > V_6 > V_7 > V_8 > V_9 ≥ 0.5 V_{DD2}

Data	Output Voltage		Data	Output Voltage	
80H	V128'	V4+(V3-V4) X 34 / 2523	C0H	V192'	V3+(V2-V3) X 43 / 1760
81H	V129'	V4+(V3-V4) X 69 / 2523	C1H	V193'	V3+(V2-V3) X 88 / 1760
82H	V130'	V4+(V3-V4) X 104 / 2523	C2H	V194'	V3+(V2-V3) X 133 / 1760
83H	V131'	V4+(V3-V4) X 140 / 2523	C3H	V195'	V3+(V2-V3) X 181 / 1760
84H	V132'	V4+(V3-V4) X 175 / 2523	C4H	V196'	V3+(V2-V3) X 229 / 1760
85H	V133'	V4+(V3-V4) X 211 / 2523	C5H	V197'	V3+(V2-V3) X 278 / 1760
86H	V134'	V4+(V3-V4) X 246 / 2523	C6H	V198'	V3+(V2-V3) X 328 / 1760
87H	V135'	V4+(V3-V4) X 282 / 2523	C7H	V199'	V3+(V2-V3) X 379 / 1760
88H	V136'	V4+(V3-V4) X 317 / 2523	C8H	V200'	V3+(V2-V3) X 431 / 1760
89H	V137'	V4+(V3-V4) X 353 / 2523	C9H	V201'	V3+(V2-V3) X 484 / 1760
8AH	V138'	V4+(V3-V4) X 389 / 2523	CAH	V202'	V3+(V2-V3) X 537 / 1760
8BH	V139'	V4+(V3-V4) X 425 / 2523	CBH	V203'	V3+(V2-V3) X 589 / 1760
8CH	V140'	V4+(V3-V4) X 462 / 2523	CCH	V204'	V3+(V2-V3) X 642 / 1760
8DH	V141'	V4+(V3-V4) X 498 / 2523	CDH	V205'	V3+(V2-V3) X 694 / 1760
8EH	V142'	V4+(V3-V4) X 535 / 2523	CEH	V206'	V3+(V2-V3) X 748 / 1760
8FH	V143'	V4+(V3-V4) X 572 / 2523	CFH	V207'	V3+(V2-V3) X 801 / 1760
90H	V144'	V4+(V3-V4) X 609 / 2523	D0H	V208'	V3+(V2-V3) X 855 / 1760
91H	V145'	V4+(V3-V4) X 647 / 2523	D1H	V209'	V3+(V2-V3) X 910 / 1760
92H	V146'	V4+(V3-V4) X 684 / 2523	D2H	V210'	V3+(V2-V3) X 965 / 1760
93H	V147'	V4+(V3-V4) X 722 / 2523	D3H	V211'	V3+(V2-V3) X 1021 / 1760
94H	V148'	V4+(V3-V4) X 760 / 2523	D4H	V212'	V3+(V2-V3) X 1078 / 1760
95H	V149'	V4+(V3-V4) X 798 / 2523	D5H	V213'	V3+(V2-V3) X 1136 / 1760
96H	V150'	V4+(V3-V4) X 836 / 2523	D6H	V214'	V3+(V2-V3) X 1195 / 1760
97H	V151'	V4+(V3-V4) X 875 / 2523	D7H	V215'	V3+(V2-V3) X 1255 / 1760
98H	V152'	V4+(V3-V4) X 914 / 2523	D8H	V216'	V3+(V2-V3) X 1315 / 1760
99H	V153'	V4+(V3-V4) X 953 / 2523	D9H	V217'	V3+(V2-V3) X 1377 / 1760
9AH	V154'	V4+(V3-V4) X 992 / 2523	DAH	V218'	V3+(V2-V3) X 1440 / 1760
9BH	V155'	V4+(V3-V4) X 1031 / 2523	DBH	V219'	V3+(V2-V3) X 1504 / 1760
9CH	V156'	V4+(V3-V4) X 1071 / 2523	DCH	V220'	V3+(V2-V3) X 1569 / 1760
9DH	V157'	V4+(V3-V4) X 1110 / 2523	DDH	V221'	V3+(V2-V3) X 1633 / 1760
9EH	V158'	V4+(V3-V4) X 1150 / 2523	DEH	V222'	V3+(V2-V3) X 1698 / 1760
9FH	V159'	V4+(V3-V4) X 1190 / 2523	DFH	V223'	V2
A0H	V160'	V4+(V3-V4) X 1230 / 2523	E0H	V224'	V2+(V1-V2) X 64 / 3070
A1H	V161'	V4+(V3-V4) X 1270 / 2523	E1H	V225'	V2+(V1-V2) X 129 / 3070
A2H	V162'	V4+(V3-V4) X 1311 / 2523	E2H	V226'	V2+(V1-V2) X 194 / 3070
A3H	V163'	V4+(V3-V4) X 1351 / 2523	E3H	V227'	V2+(V1-V2) X 259 / 3070
A4H	V164'	V4+(V3-V4) X 1392 / 2523	E4H	V228'	V2+(V1-V2) X 327 / 3070
A5H	V165'	V4+(V3-V4) X 1432 / 2523	E5H	V229'	V2+(V1-V2) X 397 / 3070
A6H	V166'	V4+(V3-V4) X 1473 / 2523	E6H	V230'	V2+(V1-V2) X 469 / 3070
A7H	V167'	V4+(V3-V4) X 1514 / 2523	E7H	V231'	V2+(V1-V2) X 545 / 3070
A8H	V168'	V4+(V3-V4) X 1555 / 2523	E8H	V232'	V2+(V1-V2) X 624 / 3070
A9H	V169'	V4+(V3-V4) X 1596 / 2523	E9H	V233'	V2+(V1-V2) X 705 / 3070
AAH	V170'	V4+(V3-V4) X 1637 / 2523	EAH	V234'	V2+(V1-V2) X 788 / 3070
ABH	V171'	V4+(V3-V4) X 1678 / 2523	EBH	V235'	V2+(V1-V2) X 873 / 3070
ACH	V172'	V4+(V3-V4) X 1719 / 2523	ECH	V236'	V2+(V1-V2) X 958 / 3070
ADH	V173'	V4+(V3-V4) X 1761 / 2523	EDH	V237'	V2+(V1-V2) X 1044 / 3070
AEH	V174'	V4+(V3-V4) X 1802 / 2523	EEH	V238'	V2+(V1-V2) X 1131 / 3070
AFH	V175'	V4+(V3-V4) X 1844 / 2523	EFH	V239'	V2+(V1-V2) X 1220 / 3070
B0H	V176'	V4+(V3-V4) X 1885 / 2523	F0H	V240'	V2+(V1-V2) X 1311 / 3070
B1H	V177'	V4+(V3-V4) X 1927 / 2523	F1H	V241'	V2+(V1-V2) X 1404 / 3070
B2H	V178'	V4+(V3-V4) X 1969 / 2523	F2H	V242'	V2+(V1-V2) X 1500 / 3070
B3H	V179'	V4+(V3-V4) X 2011 / 2523	F3H	V243'	V2+(V1-V2) X 1600 / 3070
B4H	V180'	V4+(V3-V4) X 2053 / 2523	F4H	V244'	V2+(V1-V2) X 1705 / 3070
B5H	V181'	V4+(V3-V4) X 2095 / 2523	F5H	V245'	V2+(V1-V2) X 1815 / 3070
B6H	V182'	V4+(V3-V4) X 2137 / 2523	F6H	V246'	V2+(V1-V2) X 1931 / 3070
B7H	V183'	V4+(V3-V4) X 2180 / 2523	F7H	V247'	V2+(V1-V2) X 2054 / 3070
B8H	V184'	V4+(V3-V4) X 2222 / 2523	F8H	V248'	V2+(V1-V2) X 2182 / 3070
B9H	V185'	V4+(V3-V4) X 2265 / 2523	F9H	V249'	V2+(V1-V2) X 2315 / 3070
BAH	V186'	V4+(V3-V4) X 2307 / 2523	FAH	V250'	V2+(V1-V2) X 2453 / 3070
BBH	V187'	V4+(V3-V4) X 2350 / 2523	FBH	V251'	V2+(V1-V2) X 2595 / 3070
BCH	V188'	V4+(V3-V4) X 2393 / 2523	FCH	V252'	V2+(V1-V2) X 2744 / 3070
BDH	V189'	V4+(V3-V4) X 2436 / 2523	FDH	V253'	V2+(V1-V2) X 2901 / 3070
BEH	V190'	V4+(V3-V4) X 2479 / 2523	FEH	V254'	V1
BFH	V191'	V3	FFH	V255'	V0

Figure 5–3. Relationship between Input Data and Output Voltage/Negative Side (1/2)

(Output voltage) 0.5 $V_{DD2} \geq V_{10} > V_{11} > V_{12} > V_{13} > V_{14} > V_{15} > V_{16} > V_{17} > V_{18} > V_{19} \geq V_{SS2}$ + 0.2 V

Data	Output Voltage		Data	Output Voltage	
00H	V0"	V10	40H	V64"	V14-(V14-V15) X 43 / 2389
01H	V1"	V11	41H	V65"	V14-(V14-V15) X 87 / 2389
02H	V2"	V11-(V11-V12) X 24 / 1254	42H	V66"	V14-(V14-V15) X 130 / 2389
03H	V3"	V11-(V11-V12) X 71 / 1254	43H	V67"	V14-(V14-V15) X 173 / 2389
04H	V4"	V11-(V11-V12) X 141 / 1254	44H	V68"	V14-(V14-V15) X 217 / 2389
05H	V5"	V11-(V11-V12) X 231 / 1254	45H	V69"	V14-(V14-V15) X 260 / 2389
06H	V6"	V11-(V11-V12) X 335 / 1254	46H	V70"	V14-(V14-V15) X 303 / 2389
07H	V7"	V11-(V11-V12) X 447 / 1254	47H	V71"	V14-(V14-V15) X 347 / 2389
08H	V8"	V11-(V11-V12) X 558 / 1254	48H	V72"	V14-(V14-V15) X 390 / 2389
09H	V9"	V11-(V11-V12) X 667 / 1254	49H	V73"	V14-(V14-V15) X 433 / 2389
0AH	V10"	V11-(V11-V12) X 772 / 1254	4AH	V74"	V14-(V14-V15) X 477 / 2389
0BH	V11"	V11-(V11-V12) X 872 / 1254	4BH	V75"	V14-(V14-V15) X 520 / 2389
0CH	V12"	V11-(V11-V12) X 969 / 1254	4CH	V76"	V14-(V14-V15) X 563 / 2389
0DH	V13"	V11-(V11-V12) X 1064 / 1254	4DH	V77"	V14-(V14-V15) X 607 / 2389
0EH	V14"	V11-(V11-V12) X 1159 / 1254	4EH	V78"	V14-(V14-V15) X 650 / 2389
0FH	V15"	V12	4FH	V79"	V14-(V14-V15) X 693 / 2389
10H	V16"	V12-(V12-V13) X 96 / 1183	50H	V80"	V14-(V14-V15) X 736 / 2389
11H	V17"	V12-(V12-V13) X 187 / 1183	51H	V81"	V14-(V14-V15) X 778 / 2389
12H	V18"	V12-(V12-V13) X 270 / 1183	52H	V82"	V14-(V14-V15) X 820 / 2389
13H	V19"	V12-(V12-V13) X 345 / 1183	53H	V83"	V14-(V14-V15) X 861 / 2389
14H	V20"	V12-(V12-V13) X 417 / 1183	54H	V84"	V14-(V14-V15) X 902 / 2389
15H	V21"	V12-(V12-V13) X 486 / 1183	55H	V85"	V14-(V14-V15) X 942 / 2389
16H	V22"	V12-(V12-V13) X 558 / 1183	56H	V86"	V14-(V14-V15) X 982 / 2389
17H	V23"	V12-(V12-V13) X 631 / 1183	57H	V87"	V14-(V14-V15) X 1021 / 2389
18H	V24"	V12-(V12-V13) X 706 / 1183	58H	V88"	V14-(V14-V15) X 1060 / 2389
19H	V25"	V12-(V12-V13) X 780 / 1183	59H	V89"	V14-(V14-V15) X 1099 / 2389
1AH	V26"	V12-(V12-V13) X 853 / 1183	5AH	V90"	V14-(V14-V15) X 1137 / 2389
1BH	V27"	V12-(V12-V13) X 923 / 1183	5BH	V91"	V14-(V14-V15) X 1175 / 2389
1CH	V28"	V12-(V12-V13) X 989 / 1183	5CH	V92"	V14-(V14-V15) X 1213 / 2389
1DH	V29"	V12-(V12-V13) X 1054 / 1183	5DH	V93"	V14-(V14-V15) X 1250 / 2389
1EH	V30"	V12-(V12-V13) X 1118 / 1183	5EH	V94"	V14-(V14-V15) X 1288 / 2389
1FH	V31"	V13	5FH	V95"	V14-(V14-V15) X 1325 / 2389
20H	V32"	V13-(V13-V14) X 65 / 1618	60H	V96"	V14-(V14-V15) X 1362 / 2389
21H	V33"	V13-(V13-V14) X 128 / 1618	61H	V97"	V14-(V14-V15) X 1399 / 2389
22H	V34"	V13-(V13-V14) X 190 / 1618	62H	V98"	V14-(V14-V15) X 1435 / 2389
23H	V35"	V13-(V13-V14) X 249 / 1618	63H	V99"	V14-(V14-V15) X 1471 / 2389
24H	V36"	V13-(V13-V14) X 306 / 1618	64H	V100"	V14-(V14-V15) X 1508 / 2389
25H	V37"	V13-(V13-V14) X 362 / 1618	65H	V101"	V14-(V14-V15) X 1544 / 2389
26H	V38"	V13-(V13-V14) X 416 / 1618	66H	V102"	V14-(V14-V15) X 1579 / 2389
27H	V39"	V13-(V13-V14) X 469 / 1618	67H	V103"	V14-(V14-V15) X 1615 / 2389
28H	V40"	V13-(V13-V14) X 521 / 1618	68H	V104"	V14-(V14-V15) X 1650 / 2389
29H	V41"	V13-(V13-V14) X 574 / 1618	69H	V105"	V14-(V14-V15) X 1685 / 2389
2AH	V42"	V13-(V13-V14) X 626 / 1618	6AH	V106"	V14-(V14-V15) X 1720 / 2389
2BH	V43"	V13-(V13-V14) X 678 / 1618	6BH	V107"	V14-(V14-V15) X 1754 / 2389
2CH	V44"	V13-(V13-V14) X 730 / 1618	6CH	V108"	V14-(V14-V15) X 1788 / 2389
2DH	V45"	V13-(V13-V14) X 781 / 1618	6DH	V109"	V14-(V14-V15) X 1822 / 2389
2EH	V46"	V13-(V13-V14) X 833 / 1618	6EH	V110"	V14-(V14-V15) X 1856 / 2389
2FH	V47"	V13-(V13-V14) X 884 / 1618	6FH	V111"	V14-(V14-V15) X 1889 / 2389
30H	V48"	V13-(V13-V14) X 934 / 1618	70H	V112"	V14-(V14-V15) X 1922 / 2389
31H	V49"	V13-(V13-V14) X 983 / 1618	71H	V113"	V14-(V14-V15) X 1955 / 2389
32H	V50"	V13-(V13-V14) X 1032 / 1618	72H	V114"	V14-(V14-V15) X 1987 / 2389
33H	V51"	V13-(V13-V14) X 1080 / 1618	73H	V115"	V14-(V14-V15) X 2019 / 2389
34H	V52"	V13-(V13-V14) X 1127 / 1618	74H	V116"	V14-(V14-V15) X 2051 / 2389
35H	V53"	V13-(V13-V14) X 1173 / 1618	75H	V117"	V14-(V14-V15) X 2082 / 2389
36H	V54"	V13-(V13-V14) X 1219 / 1618	76H	V118"	V14-(V14-V15) X 2113 / 2389
37H	V55"	V13-(V13-V14) X 1265 / 1618	77H	V119"	V14-(V14-V15) X 2144 / 2389
38H	V56"	V13-(V13-V14) X 1310 / 1618	78H	V120"	V14-(V14-V15) X 2175 / 2389
39H	V57"	V13-(V13-V14) X 1355 / 1618	79H	V121"	V14-(V14-V15) X 2205 / 2389
3AH	V58"	V13-(V13-V14) X 1399 / 1618	7AH	V122"	V14-(V14-V15) X 2235 / 2389
3BH	V59"	V13-(V13-V14) X 1444 / 1618	7BH	V123"	V14-(V14-V15) X 2265 / 2389
3CH	V60"	V13-(V13-V14) X 1488 / 1618	7CH	V124"	V14-(V14-V15) X 2295 / 2389
3DH	V61"	V13-(V13-V14) X 1531 / 1618	7DH	V125"	V14-(V14-V15) X 2326 / 2389
3EH	V62"	V13-(V13-V14) X 1574 / 1618	7EH	V126"	V14-(V14-V15) X 2357 / 2389
3FH	V63"	V14	7FH	V127"	V15

Figure 5–3. Relationship between Input Data and Output Voltage/Negative Side (2/2)

(Output voltage) 0.5 $V_{DD2} \geq V_{10} > V_{11} > V_{12} > V_{13} > V_{14} > V_{15} > V_{16} > V_{17} > V_{18} > V_{19} \geq V_{SS2}$ + 0.2 V

Data	Output Voltage		Data	Output Voltage	
80H	V128"	V15-(V15-V16) X 34 / 2523	C0H	V192"	V16-(V16-V17) X 43 / 1760
81H	V129"	V15-(V15-V16) X 69 / 2523	C1H	V193"	V16-(V16-V17) X 88 / 1760
82H	V130"	V15-(V15-V16) X 104 / 2523	C2H	V194"	V16-(V16-V17) X 133 / 1760
83H	V131"	V15-(V15-V16) X 140 / 2523	C3H	V195"	V16-(V16-V17) X 181 / 1760
84H	V132"	V15-(V15-V16) X 175 / 2523	C4H	V196"	V16-(V16-V17) X 229 / 1760
85H	V133"	V15-(V15-V16) X 211 / 2523	C5H	V197"	V16-(V16-V17) X 278 / 1760
86H	V134"	V15-(V15-V16) X 246 / 2523	C6H	V198"	V16-(V16-V17) X 328 / 1760
87H	V135"	V15-(V15-V16) X 282 / 2523	C7H	V199"	V16-(V16-V17) X 379 / 1760
88H	V136"	V15-(V15-V16) X 317 / 2523	C8H	V200"	V16-(V16-V17) X 431 / 1760
89H	V137"	V15-(V15-V16) X 353 / 2523	C9H	V201"	V16-(V16-V17) X 484 / 1760
8AH	V138"	V15-(V15-V16) X 389 / 2523	CAH	V202"	V16-(V16-V17) X 537 / 1760
8BH	V139"	V15-(V15-V16) X 425 / 2523	CBH	V203"	V16-(V16-V17) X 589 / 1760
8CH	V140"	V15-(V15-V16) X 462 / 2523	CCH	V204"	V16-(V16-V17) X 642 / 1760
8DH	V141"	V15-(V15-V16) X 498 / 2523	CDH	V205"	V16-(V16-V17) X 694 / 1760
8EH	V142"	V15-(V15-V16) X 535 / 2523	CEH	V206"	V16-(V16-V17) X 748 / 1760
8FH	V143"	V15-(V15-V16) X 572 / 2523	CFH	V207"	V16-(V16-V17) X 801 / 1760
90H	V144"	V15-(V15-V16) X 609 / 2523	D0H	V208"	V16-(V16-V17) X 855 / 1760
91H	V145"	V15-(V15-V16) X 647 / 2523	D1H	V209"	V16-(V16-V17) X 910 / 1760
92H	V146"	V15-(V15-V16) X 684 / 2523	D2H	V210"	V16-(V16-V17) X 965 / 1760
93H	V147"	V15-(V15-V16) X 722 / 2523	D3H	V211"	V16-(V16-V17) X 1021 / 1760
94H	V148"	V15-(V15-V16) X 760 / 2523	D4H	V212"	V16-(V16-V17) X 1078 / 1760
95H	V149"	V15-(V15-V16) X 798 / 2523	D5H	V213"	V16-(V16-V17) X 1136 / 1760
96H	V150"	V15-(V15-V16) X 836 / 2523	D6H	V214"	V16-(V16-V17) X 1195 / 1760
97H	V151"	V15-(V15-V16) X 875 / 2523	D7H	V215"	V16-(V16-V17) X 1255 / 1760
98H	V152"	V15-(V15-V16) X 914 / 2523	D8H	V216"	V16-(V16-V17) X 1315 / 1760
99H	V153"	V15-(V15-V16) X 953 / 2523	D9H	V217"	V16-(V16-V17) X 1377 / 1760
9AH	V154"	V15-(V15-V16) X 992 / 2523	DAH	V218"	V16-(V16-V17) X 1440 / 1760
9BH	V155"	V15-(V15-V16) X 1031 / 2523	DBH	V219"	V16-(V16-V17) X 1504 / 1760
9CH	V156"	V15-(V15-V16) X 1071 / 2523	DCH	V220"	V16-(V16-V17) X 1569 / 1760
9DH	V157"	V15-(V15-V16) X 1110 / 2523	DDH	V221"	V16-(V16-V17) X 1633 / 1760
9EH	V158"	V15-(V15-V16) X 1150 / 2523	DEH	V222"	V16-(V16-V17) X 1698 / 1760
9FH	V159"	V15-(V15-V16) X 1190 / 2523	DFH	V223"	V17
A0H	V160"	V15-(V15-V16) X 1230 / 2523	E0H	V224"	V17-(V17-V18) X 64 / 3070
A1H	V161"	V15-(V15-V16) X 1270 / 2523	E1H	V225"	V17-(V17-V18) X 129 / 3070
A2H	V162"	V15-(V15-V16) X 1311 / 2523	E2H	V226"	V17-(V17-V18) X 194 / 3070
A3H	V163"	V15-(V15-V16) X 1351 / 2523	E3H	V227"	V17-(V17-V18) X 259 / 3070
A4H	V164"	V15-(V15-V16) X 1392 / 2523	E4H	V228"	V17-(V17-V18) X 327 / 3070
A5H	V165"	V15-(V15-V16) X 1432 / 2523	E5H	V229"	V17-(V17-V18) X 397 / 3070
A6H	V166"	V15-(V15-V16) X 1473 / 2523	E6H	V230"	V17-(V17-V18) X 469 / 3070
A7H	V167"	V15-(V15-V16) X 1514 / 2523	E7H	V231"	V17-(V17-V18) X 545 / 3070
A8H	V168"	V15-(V15-V16) X 1555 / 2523	E8H	V232"	V17-(V17-V18) X 624 / 3070
A9H	V169"	V15-(V15-V16) X 1596 / 2523	E9H	V233"	V17-(V17-V18) X 705 / 3070
AAH	V170"	V15-(V15-V16) X 1637 / 2523	EAH	V234"	V17-(V17-V18) X 788 / 3070
ABH	V171"	V15-(V15-V16) X 1678 / 2523	EBH	V235"	V17-(V17-V18) X 873 / 3070
ACH	V172"	V15-(V15-V16) X 1719 / 2523	ECH	V236"	V17-(V17-V18) X 958 / 3070
ADH	V173"	V15-(V15-V16) X 1761 / 2523	EDH	V237"	V17-(V17-V18) X 1044 / 3070
AEH	V174"	V15-(V15-V16) X 1802 / 2523	EEH	V238"	V17-(V17-V18) X 1131 / 3070
AFH	V175"	V15-(V15-V16) X 1844 / 2523	EFH	V239"	V17-(V17-V18) X 1220 / 3070
B0H	V176"	V15-(V15-V16) X 1885 / 2523	F0H	V240"	V17-(V17-V18) X 1311 / 3070
B1H	V177"	V15-(V15-V16) X 1927 / 2523	F1H	V241"	V17-(V17-V18) X 1404 / 3070
B2H	V178"	V15-(V15-V16) X 1969 / 2523	F2H	V242"	V17-(V17-V18) X 1500 / 3070
B3H	V179"	V15-(V15-V16) X 2011 / 2523	F3H	V243"	V17-(V17-V18) X 1600 / 3070
B4H	V180"	V15-(V15-V16) X 2053 / 2523	F4H	V244"	V17-(V17-V18) X 1705 / 3070
B5H	V181"	V15-(V15-V16) X 2095 / 2523	F5H	V245"	V17-(V17-V18) X 1815 / 3070
B6H	V182"	V15-(V15-V16) X 2137 / 2523	F6H	V246"	V17-(V17-V18) X 1931 / 3070
B7H	V183"	V15-(V15-V16) X 2180 / 2523	F7H	V247"	V17-(V17-V18) X 2054 / 3070
B8H	V184"	V15-(V15-V16) X 2222 / 2523	F8H	V248"	V17-(V17-V18) X 2182 / 3070
B9H	V185"	V15-(V15-V16) X 2265 / 2523	F9H	V249"	V17-(V17-V18) X 2315 / 3070
BAH	V186"	V15-(V15-V16) X 2307 / 2523	FAH	V250"	V17-(V17-V18) X 2453 / 3070
BBH	V187"	V15-(V15-V16) X 2350 / 2523	FBH	V251"	V17-(V17-V18) X 2595 / 3070
BCH	V188"	V15-(V15-V16) X 2393 / 2523	FCH	V252"	V17-(V17-V18) X 2744 / 3070
BDH	V189"	V15-(V15-V16) X 2436 / 2523	FDH	V253"	V17-(V17-V18) X 2901 / 3070
BEH	V190"	V15-(V15-V16) X 2479 / 2523	FEH	V254"	V18
BFH	V191"	V16	FFH	V255"	V19

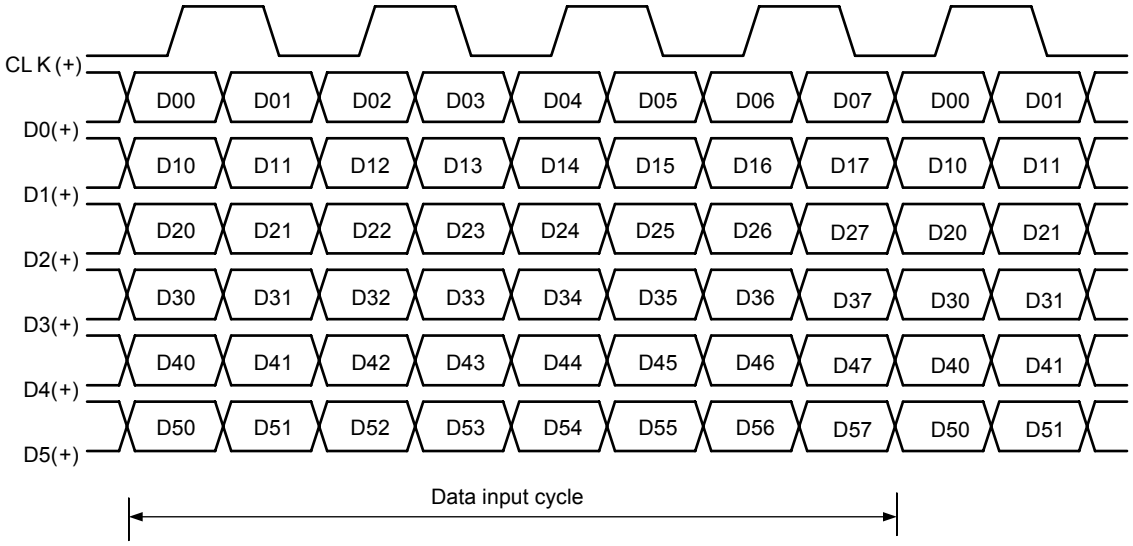
6. FUNCTION DESCRIPTION

6.1 Data Mapping

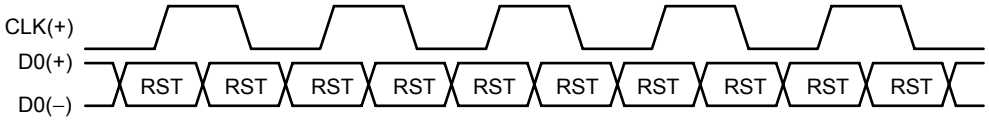
Display data and control data (RST) are input to D0(+/–) to D5(+/–).

Data mapping is changed in response to the mode.

<Data Input Mode>



<Control Signal Input Mode>



6.2 Output Timing and Polarity are controlled by STB and POL Signals

Refer to **4. PIN FUNCTIONS**.

6.3 Composition of Display Data

MSB LSB

Dn7	Dn6	Dn5	Dn4	Dn3	Dn2	Dn1	Dn0

Remark n = 0 to 5

6.4 Relation between Display Data and Output Number

This relationship is irrespective of R,/L condition.

(1) Right shift (R,/L = H)

Output	S1	S2	S3	→	S478	S479	S480
Display Data	D00 to D07	D10 to D17	D20 to D27	→	D30 to D37	D40 to D47	D50 to D57

(2) Left shift (R,/L = L)

Output	S480	S479	S478	→	S3	S2	S1
Display Data	D50 to D57	D40 to D47	D30 to D37	→	D20 to D27	D10 to D17	D00 to D07

<R> **6.5 Cascade**

Multiple chips can be used in a cascade connection.

- Input STHR(L) at lead (head) chip is fixed to H.
- Input STHR(L) after secondary chips are connected from output STHL(R) at foregoing chip.

<R> **6.6 Loading the Display Data**

(1) The head IC that STHR(L) is H is set as a control signal input mode (control mode) by the rising edge of STB.
Also, the receivers at D0(+/–) and CLK(+/–) of all IC are activated by rising edge of STB.

↓

(2) This D0(+/–) should be kept over 200 ns L after rising of STB.

↓

(3) RST is recognized by setting D0 (+/–) to H. And H width should be over 50 ns and also over 3 CLK cycles.

↓

(4) RST is released by rising edge of CLK after setting D0 (+/–) to L and shifts to data input mode function.
By the way, input STB again when a second RST is necessary.

↓

(5) Data sampling starts at the next rising edge of CLK of the rising edge of CLK which released RST by (4).

↓

(6) At the same time data sampling starts, internal counter starts counting the data cycle for STHR(L) signal generation.
Therefore, STHL(R) H is outputted to the following stage chip from rising edge of CLK of 315 CLK shot.

↓

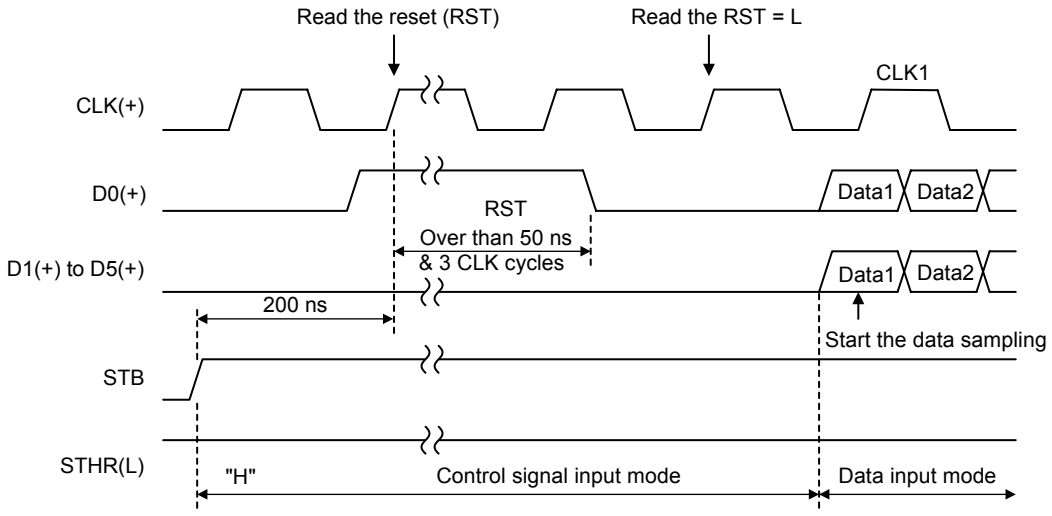
(7) After data sampling is finished, the receivers turn OFF.

↓

(8) After the receivers turn OFF, keep the timing for more than 5 CLK cycles until STB is inputted (the sequence from the above (1) is repeated by the next STB being inputted).

(9) Figure 6–1 shows the rough timing chart from application of STB to the start of data sampling.

Figure 6–1 Timing from start to sampling (reference)



7. RELATIONSHIP BETWEEN POL AND H_2DOT

This driver IC can change the relation between analog output channel and its polarity, dot inversion, 2-dot inversion or square inversion, by controlling POL and H_2DOT pins. Please refer to the following table for more detail.

7.1 Dot Inversion (H_2DOT = L)

POL	S1	S2	S3	S4	S5	S6	S7	---
H	–	+	–	+	–	+	–	---
L	+	–	+	–	+	–	+	---
H	–	+	–	+	–	+	–	---
L	+	–	+	–	+	–	+	---
H	–	+	–	+	–	+	–	---
∣	∣	∣	∣	∣	∣	∣	∣	

7.2 Vertical 2-dot Inversion (H_2DOT = L)

POL	S1	S2	S3	S4	S5	S6	S7	---
H	–	+	–	+	–	+	–	---
H	–	+	–	+	–	+	–	---
L	+	–	+	–	+	–	+	---
L	+	–	+	–	+	–	+	---
H	–	+	–	+	–	+	–	---
∣	∣	∣	∣	∣	∣	∣	∣	

7.3 Horizontal 2-dot Inversion (H_2DOT = H)

POL	S1	S2	S3	S4	S5	S6	S7	---
L	+	–	–	+	+	–	–	---
H	–	+	+	–	–	+	+	---
L	+	–	–	+	+	–	–	---
H	–	+	+	–	–	+	+	---
L	+	–	–	+	+	–	–	---
∣	∣	∣	∣	∣	∣	∣	∣	

7.4 Square Inversion (H_2DOT = H)

POL	S1	S2	S3	S4	S5	S6	S7	---
L	+	–	–	+	+	–	–	---
L	+	–	–	+	+	–	–	---
H	–	+	+	–	–	+	+	---
H	–	+	+	–	–	+	+	---
L	+	–	–	+	+	–	–	---
∣	∣	∣	∣	∣	∣	∣	∣	

<R> 8. OUTPUT RESET FUNCTION (MODE)

This driver IC has an output reset function controlled by MODE1 and MODE2 pin.

MODE1 = L and MODE2 = L:

Output Reset function doesn't work, so the output terminal becomes Hi-Z condition during STB = H and gray-scale voltage output to the LCD start at the falling edge of STB.

MODE1 = H and MODE2 = L:

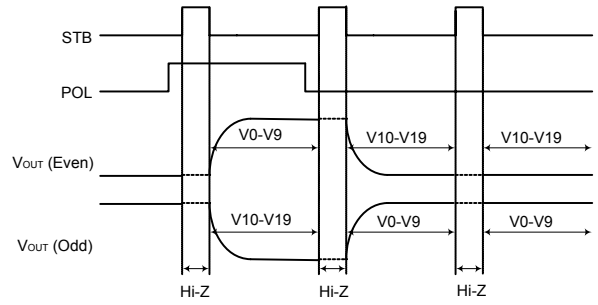
Output Reset function works during STB = H period.

But when POL signal is not changed from previous line, output becomes Hi-Z condition during STB = H, in other words output reset doesn't work.

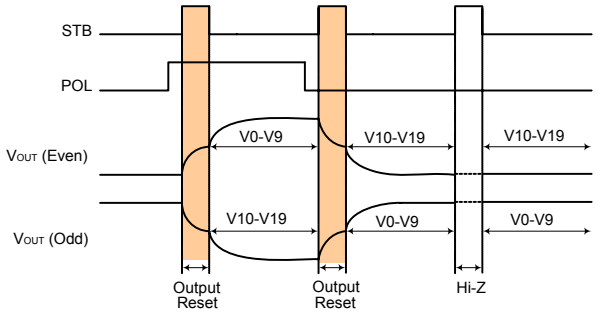
MODE1 = H and MODE2 = H:

Output Reset function work during STB = H period whether POL signal is changed or not.

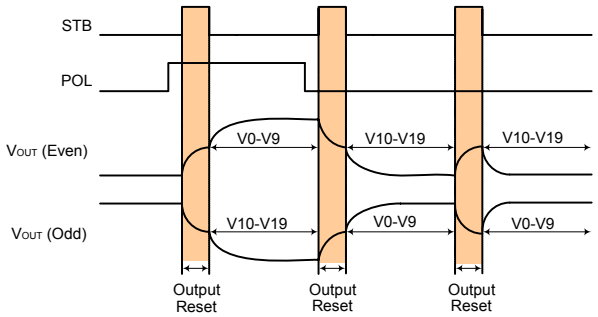
< MODE1 = L, MODE2 = L>



< MODE1 = H, MODE2 = L>



< MODE1 = H, MODE2 = H>



Caution A setup of MODE1 = L and MODE2 = H is setting prohibited (μPD160032A becomes a test mode and does not perform normal specification operation).

9. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C, V_{SS1} = V_{SS2} = 0 V)

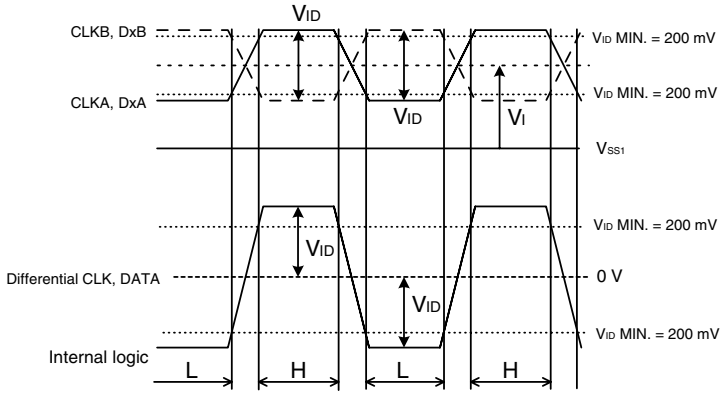
Parameter	Symbol	Ratings	Unit
Logic power supply voltage	V_{DD1}	–0.5 to +4.0	V
Driver power supply voltage	V_{DD2}	–0.5 to +18.0	V
Logic input voltage	V_{I1}	–0.5 to V_{DD1} + 0.5	V
Logic output voltage	V_{O1}	–0.5 to V_{DD1} + 0.5	V
Logic output current	I_O	±10	mA
Driver input voltage	V_{I2}	–0.5 to V_{DD2} + 0.5	V
Driver output voltage	V_{O2}	–0.5 to V_{DD2} + 0.5	V
Operating ambient temperature	T_A	–10 to +75	°C
Storage temperature	T_{stg}	–55 to +125	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Range (T_A = –10 to +75°C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Logic power supply voltage	V_{DD1}		2.7	3.0	3.6	V
Driver power supply voltage	V_{DD2}		10	15.4	16.5	V
CMOS high-level input voltage	V_{IH}	STHR(L), R,/L, STB, SRC, SB, POL, RxBIAS, MODE1, MODE2, ORC, V_{sel1}, V_{sel2}, H_2DOT	0.7 V_{DD1}		V_{DD1}	V
CMOS low-level input voltage	V_{IL}		0		0.3 V_{DD1}	V
mini-LVDS input voltage (Center)	V_I	CLKA, CLKB, D0A, D0B to D5A, D5B	0.3 + (V_{ID}/2)		(V_{DD1} –1.2) – V_{ID} /2	V
mini-LVDS differential voltage range (Amplitude)	V_{ID}		200		600	mV
γ- corrected voltage	V_0-V_9		0.5 V_{DD2}		V_{DD2} – 0.2	V
	V_{10}-V_{19}		0.2		0.5 V_{DD2}	V
Driver output voltage	V_{OUT}		0.2		V_{DD2} – 0.2	V
Clock frequency	f_{CLK}	CLKA, CLKB		162	172	MHz

<R>



<R> **Electrical Characteristics (T_A = –10 to +75°C, V_{DD1} = 2.7 to 3.6 V, V_{DD2} = 10.0 to 16.5 V, V_{SS1} = V_{SS2} = 0 V)**

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input leakage current	I_{IL}	STHR(L), R,/L, STB, SB, POL, RxBIAS, SRC, ORC, MODE1, MODE2, V_{sel1}, V_{sel2}, H_2DOT, CLKA, CLKB, D0A/B to D5A/B			±1.0	μA
High level output voltage	V_{OH}	STHR(STHL), I_{OH} = 0 mA	V_{DD1} – 0.4		V_{DD1}	V
Low level output voltage	V_{OL}	STHR(STHL), I_{OL} = 0 mA	V_{SS1}		V_{SS1} + 0.4	V
γ-corrected resistor value	Rγ	V_0-V_9 = V_{10} -V_{19}	9.8	14.0	18.2	kΩ
Driver output current	I_{VOH}	V_X = V_{DD2} – 0.2 V, V_{OUT} = V_X – 1.0 V Note1			–60	μA
	I_{VOL}	V_X = V_{SS2} + 0.2 V, V_{OUT} = V_X +1.0V Note1	60			μA
Output voltage deviation	ΔV_o	T_A = 25°C, V_O = V_{SS2} + 1.0 V～ V_{DD2} – 1.0 V		±10	±20	mV
Output swing voltage difference deviation	ΔV_{P-P1}	T_A = 25°C, V_1 = 3.3 V, V_{DD2} = 15 V, V_{OUT} = 7.0 to 8.0 V Note2		±5	±10	mV
	ΔV_{P-P2}	T_A = 25°C, V_1 = 3.3 V, V_{DD2} = 15 V, V_{OUT} = 4.0 to 11.0 V Note2		±7	±15	mV
	ΔV_{P-P3}	T_A = 25°C, V_1 = 3.3 V, V_{DD2} = 15 V, V_{OUT} = 1.0 to 14.0 V Note2		±10	±20	mV
Output swing voltage average deviation	AV_O	T_A = 25°C, V_1 = 3.3 V, V_{DD2} = 15 V, V_{OUT} = 8.0 V Note3		±8	±10	mV
Logic dynamic current consumption	I_{DD11}	Checkered, f_{STB} = 75 kHz (PW = 500 ns), f_{CLK} = 162 MHz, RxBIAS = H		3.2	6.0	mA
Logic static current consumption	I_{DD12}	No CLK & Input, RxBIAS = H		2.9	5.0	mA
Driver dynamic current consumption	I_{DD21}	Raster pattern, V_{DD2} = 16.5 V, f_{STB} =75 kHz (PW = 500 ns) with no load		14.0	30.0	mA
Driver static current consumption	I_{DD22}	Raster pattern, V_{DD2} = 16.5 V with no load		11.0	20.0	mA

Notes 1. V_X refers to the output voltage of analog output pins S1 to S480.
V_{OUT} refers to the voltage applied to analog output pins S1 to S480.

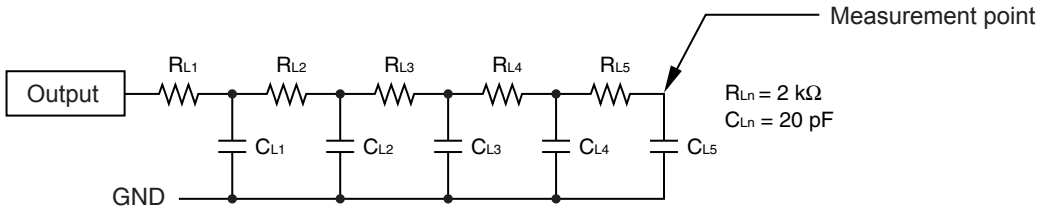
2. Amplitude offset when all of output ports out same data.

3. Deviation of averaged amplitude offset value between chips.

<R> **Switching Characteristics (T_A = –10 to +75°C, V_{DD1} = 2.7 to 3.6 V, V_{DD2} = 10.0 to 16.5 V, V_{SS1} = V_{SS2} = 0 V)**

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Start pulse delay time	t_1	C_L = 50 pF	6	15	22	ns
Driver output delay time	t_2	R_L = 10 kΩ, C_L = 100 pF		2	5	μs
	t_3	SRC = H, V_{sel2} = H, ORC = H,		4	10	μs
	t_4	refer to <Test Condition >		2	5	μs
	t_5			4	10	μs
Input capacitance	C_{I1}	STHR(L), T_A = 25°C		5		pF
	C_{I2}	Except STHR(L), T_A = 25°C		4		pF

<Test Condition>



Timing Requirements (T_A = –10 to +75°C, V_{DD1} = 2.7 to 3.6 V, V_{SS1} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock pulse width	t_6		5.8			ns
Clock pulse high period	t_7		2.2			ns
Clock pulse low period	t_8		2.2			ns
Data setup time	t_9		1.0			ns
Data hold time	t_{10}		1.0			ns
Start pulse setup time	t_{11}		–1.0			ns
Start pulse hold time	t_{12}		3.0			ns
STB pulse width	t_{13}		200			ns
POL setup time	t_{14}		–5.0			ns
POL hold time	t_{15}		6.0			ns
RST high period	t_{16}		50.0			ns
			3			CLK
Receiver OFF to STB timing	t_{17}		5			CLK
STB to RST input time	t_{18}		200			ns
RST Low to STB setup time	t_{19}		0			ns
Signal rising time	t_{20}	mini-LVDS signal			0.5	ns
Signal fall time	t_{21}	mini-LVDS signal			0.5	ns

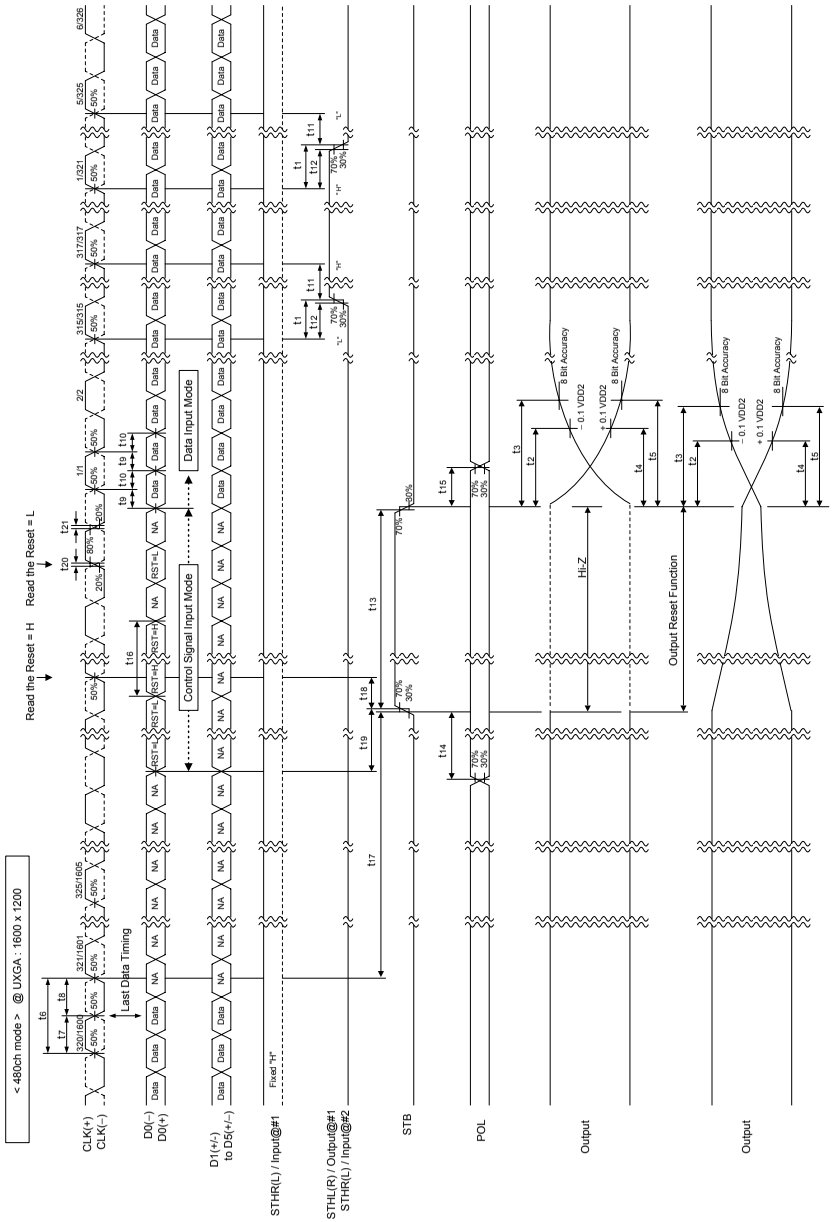
Remark Unless otherwise specified, V_{IH} and V_{IL} of the CMOS signals are defined as V_{IH} = 0.7 V_{DD1}, V_{IL} = 0.3 V_{DD1}.

<R> **Switching Characteristic Waveform (R,/L = H)**

Unless otherwise specified, V_{IH} and V_{IL} of the CMOS signals are defined as V_{IH} = 0.7 V_{DD1}, V_{IL} = 0.3 V_{DD1}.

Also, unless otherwise specified, V_{IH} and V_{IL} of the mini-LVDS signals are defined as V_{IH} = V_{IL} = V_I (Center of V_{ID}).

(Clock and display data numbers are examples when UXGA is used.)



10. RECOMMENDED MOUNTING CONDITIONS

The following conditions must be met for mounting conditions of the μPD160032A.

For more details, refer to the **Semiconductor Device Mount Manual (http://www.necel.com/pkg/en/mount/index.html).**

Please consult with our sales offices in case other mounting process is used, or in case the mounting is done under different conditions.

μPD160032AN-xxx: TCP (TAB package)

Mounting Condition	Mounting Method	Condition
Thermocompression	Soldering	Heating tool 300 to 350°C, heating for 2 to 3 sec, pressure 100 g (per solder).
	ACF (Adhesive Conductive Film)	Temporary bonding 70 to 100°C, pressure 3 to 8 kg/cm^2, time 3 to 5 sec. Real bonding 165 to 180°C, pressure 25 to 45 kg/cm^2, time 30 to 40 sec (When using the anisotropy conductive film SUMIZAC1003 of Sumitomo Bakelite, Ltd).

Caution To find out the detailed conditions for mounting the ACF part, please contact the ACF manufacturing company. Be sure to avoid using two or more mounting methods at a time.

Revision History

Version	Date	Page	Revised Item
1.0	August 6, 2003		1st edition
1.1	August 22, 2003	8	**Figure 5–1**
1.2	November 4, 2003	1	Document No.

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

Reference Documents

NEC Semiconductor Device Reliability/Quality Control System (C10983E)

Quality Grades On NEC Semiconductor Devices (C11531E)

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