NEC
ELECTRON DEVICE

MOS INTEGRATED CIRCUIT

μPD17P401

ONE-TIME PROM VERSION 4-BIT SINGLE CHIP MICROCONTROLLER WITH DEDICATED ON-CHIP VCR CAMERA HARDWARE

The μPD17P401 is a version of the μPD17401, incorporating various kinds of hardware ideally suited to VCR camera use, in which the on-chip mask ROM is replaced by one-time PROM.

Since the μPD17P401 can be programmed by the user, it is suitable for pre-production use in μPD17401 system development and for limited production.

This data sheet should be read in conjunction with documentation on the μPD17401.

The electrical specifications of the μPD17P401 differ in some respects from those of the μPD17401 (supply current, etc.). Please note these differences before undertaking volume design of an application set.

FEATURES

- μPD17401 compatible (except electrical specifications)
- On-chip one-time PROM: 12288 x 16 bits
- Operating voltage range: 5 V ±10 %

ORDERING INFORMATION

Order Code	Package	Quality Grade
μPD17P401GC-xxx-3B9	80-pin plastic QFP (14 x 14 mm)	Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

The information in this document is subject to change without notice.

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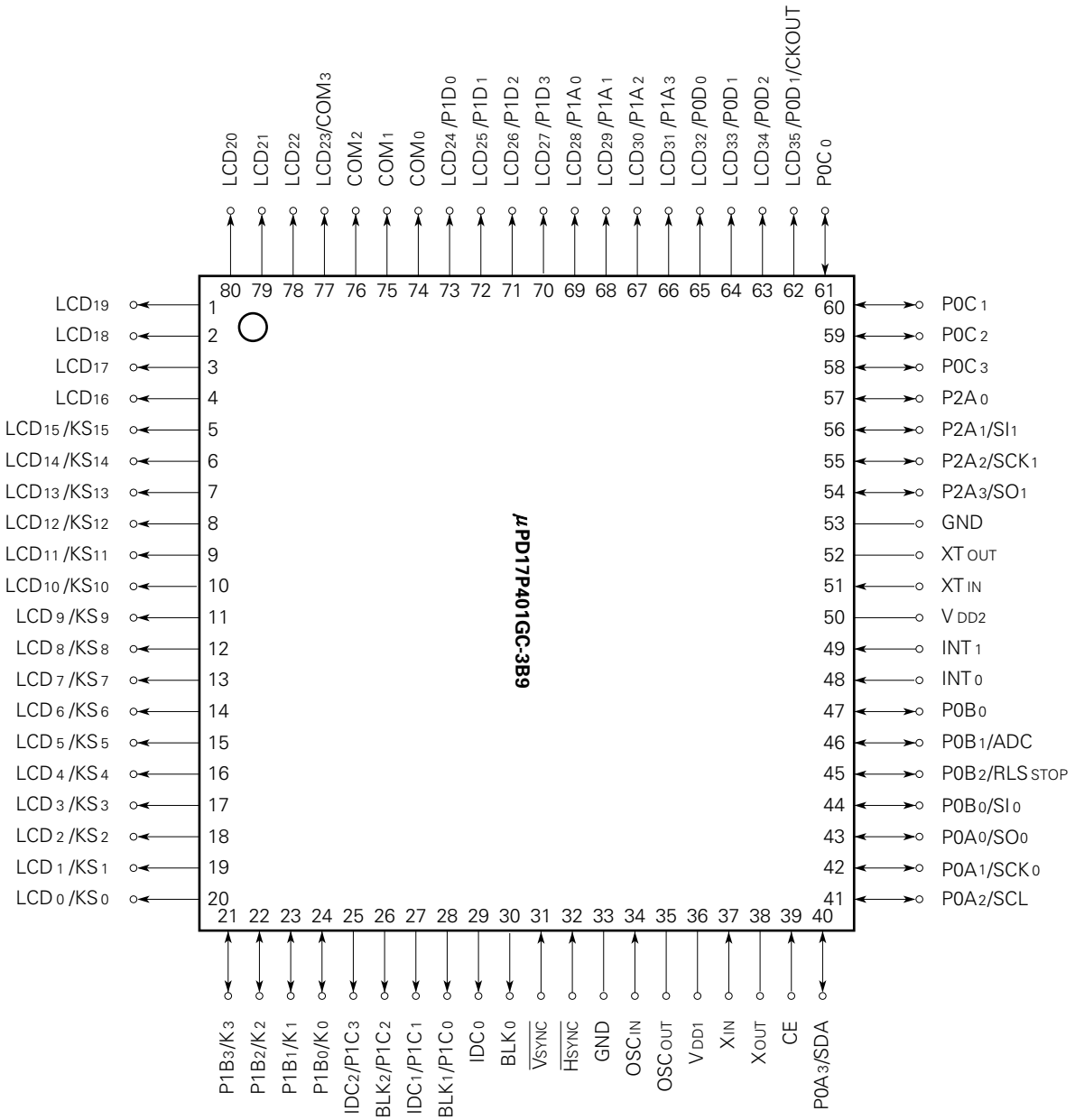
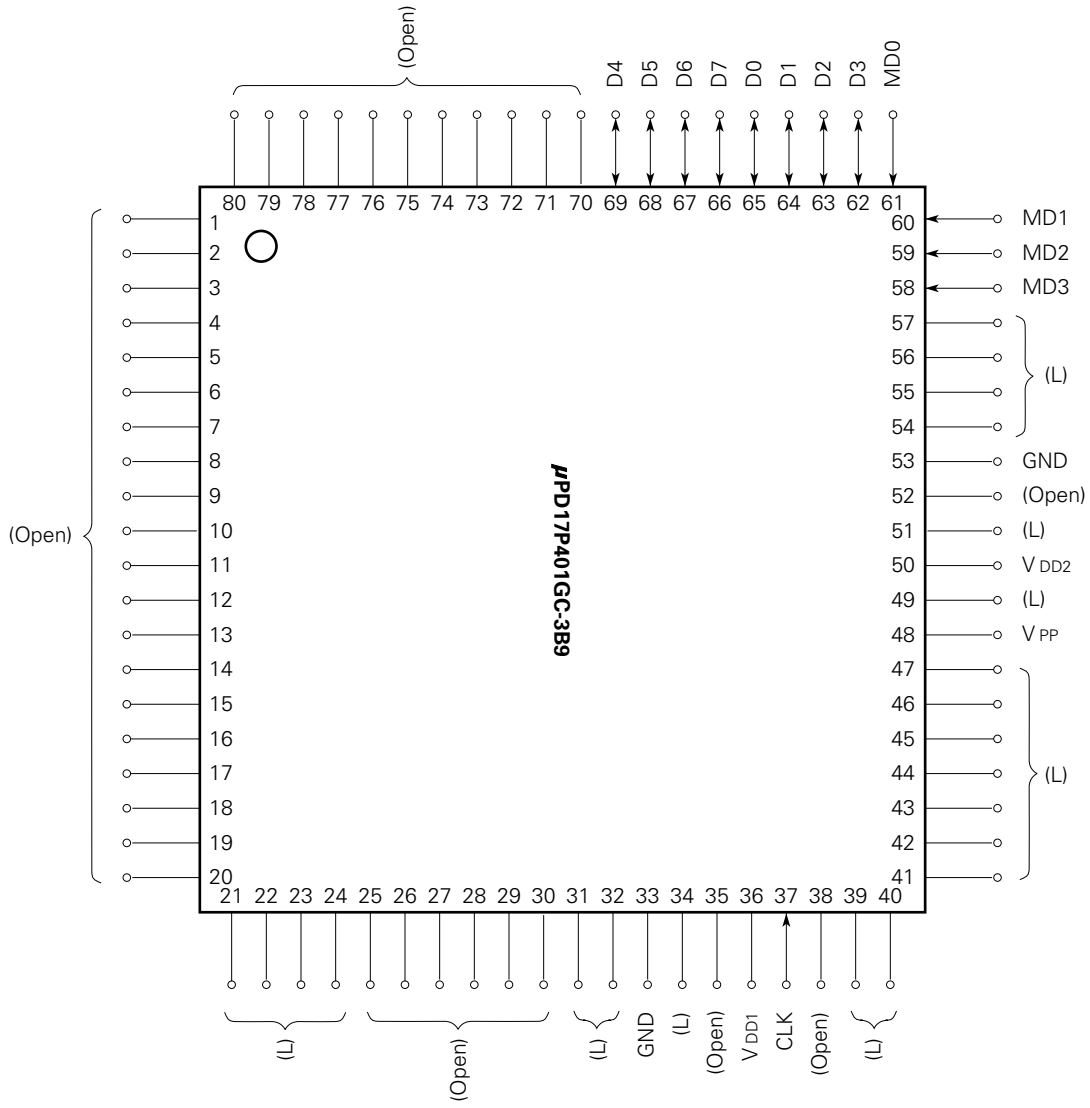
PIN CONFIGURATION (Top View)

(1) Normal operating mode



(2) PROM programming mode



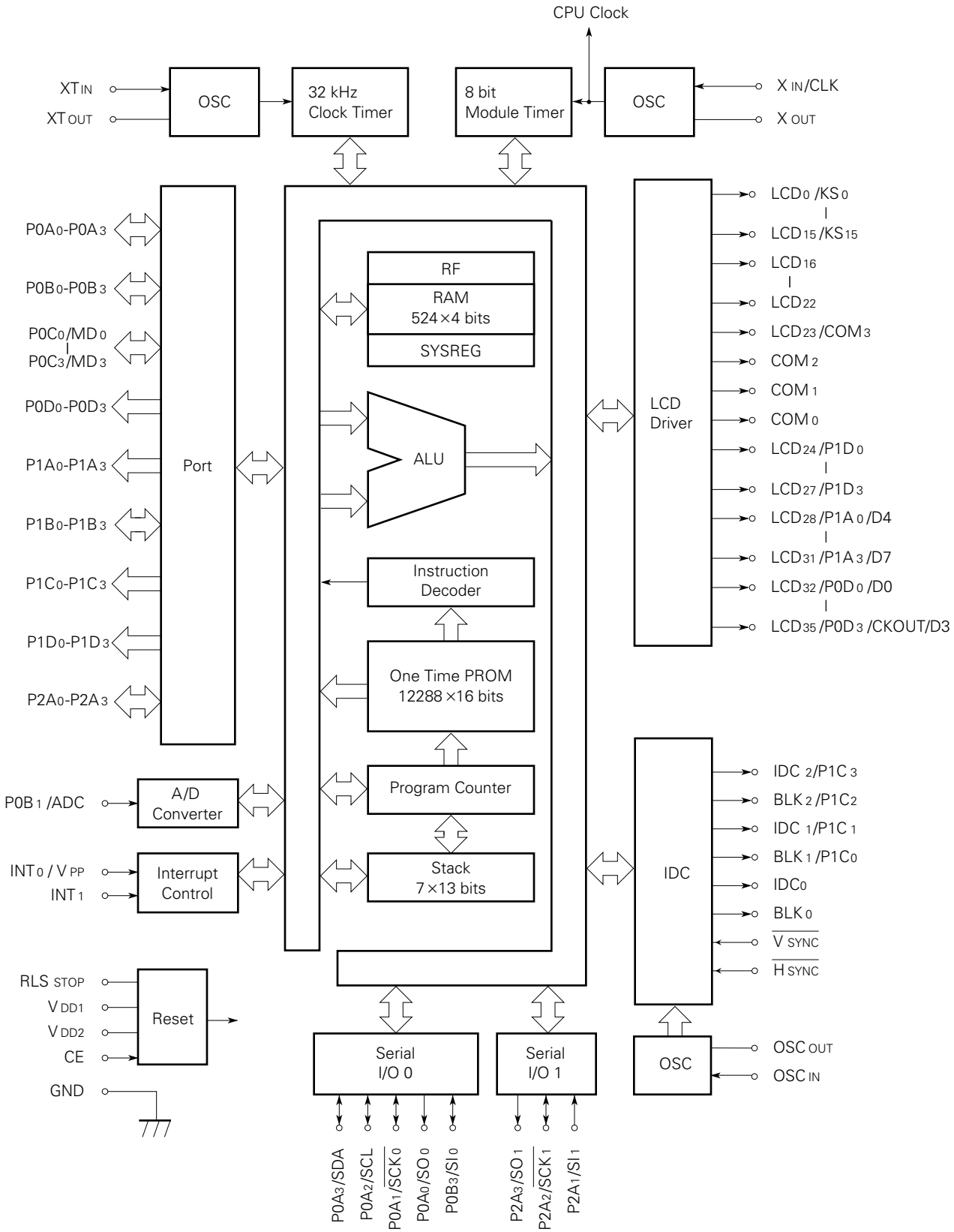
Note Items in parentheses indicate disposition of unused pins in the PROM programming mode.

L : Connect to GND via an individual resistor (470 Ω).

Open: Leave open.

$P0A_0$ to $P0A_3$: Input/output ports
$P0B_0$ to $P0B_3$: Input/output ports
$P0C_0$ to $P0C_3$: Input/output ports
$P0D_0$ to $P0D_3$: Output ports
$P1A_0$ to $P1A_3$: Output ports
$P1B_0$ to $P1B_3$: Input/output ports
$P1C_0$ to $P1C_3$: Output ports
$P1D_0$ to $P1D_3$: Output ports
$P2A_0$ to $P2A_3$: Input/output ports
KS_0 to KS_{15} : Key source signal outputs
K_0 to K_3 : Key source signal return inputs
LCD_0 to LCD_{35} : LCD segment signal outputs
COM_0 to COM_3 : LCD common signal outputs
CKOUT : Sub-clock output
RLS_{STOP} : Stop mode release input
CE : Chip enable input
INT_0, INT_1 : External interrupt inputs
ADC : A/D converter input
SDA : Serial data input/output
SCL : Serial clock input/output
SI_0, SI_1 : Serial data inputs
SO_0, SO_1 : Serial data outputs
$\overline{SCK}_0$, $\overline{SCK}_1$: Serial clock input/outputs
X_{IN}, X_{OUT} : Main clock oscillator
XT_{IN}, XT_{OUT} : Sub-clock oscillator
OSC_{IN}, OSC_{OUT} : IDC oscillator
IDC_0 to IDC_2 : IDC display signal outputs
BLK_0 to BLK_2 : Blanking signal outputs
$\overline{H_{SYNC}}$: Horizontal synchronization signal input
$\overline{V_{SYNC}}$: Vertical synchronization signal input
CLK : PROM clock input
MD_0 to MD_3 : PROM mode selection inputs
D0 to D7 : PROM data input/outputs
V_{PP} : PROM power supply
V_{DD1}, V_{DD2} : Power supply
GND : Ground

BLOCK DIAGARAM



CONTENTS

1. PIN FUNCTIONS

1.1 NORMAL OPERATING MODE

PIN NO.	SYMBOL	FUNCTION	OUTPUT TYPE	AFTER POWER-ON RESET
62 | 65 66 | 69 70 | 73 74 | 76 77 78 | 80 1 | 4 5 | 20	$LCD_{35}/P0D_3/CKOUT$ | $LCD_{32}/P0D_0$ $LCD_{31}/P1A_3$ | $LCD_{28}/P1A_0$ $LCD_{27}/P1D_3$ | $LCD_{24}/P1D_0$ COM_0 | COM_2 LCD_{23}/COM_3 LCD_{22} | LCD_{20} LCD_{19} | LCD_{16} LCD_{15}/KS_{15} | LCD_0/KS_0	LCD controller/driver segment signal, LCD controller/driver common signal, key matrix key source signal, port 0D, port 1A, port 1D and watchdog timer 32 kHz crystal resonator oscillation signal outputs. • LCD_{35} to LCD_0 ・ LCD controller/driver segment signal outputs • COM_0 to COM_3 ・ LCD controller/driver common signal outputs • KS_{15} to KS_0 ・ Key matrix key source signal outputs • $P0D_3$ to $P0D_0$ ・ 4-bit CMOS output port • $P1A_3$ to $P1A_0$ ・ 4-bit CMOS output port • $P1D_3$ to $P1D_0$ ・ 4-bit CMOS output port • CKOUT ・ Watchdog timer 32 kHz oscillation signal output ・ Watchdog timer 32 kHz crystal resonator (XT_{IN}, XT_{OUT}) oscillation frequency adjustment	CMOS	Low-level output (LCD_{35} to LCD_0, COM_0 to COM_3)
21 | 24	$P1B_3/K_3$ | $P1B_0/K_0$	Port 1B and LCD segment key source signal return inputs. • $P1B_3$ to $P1B_0$ ・ 4-bit input/output port ・ Input/output set capability as a 4-bit unit ・ Internal pull-up resistor OFF • K_3 to K_0 ・ Key source signal return inputs ・ Internal pull-up resistor ON	Inputs with pull-up resistor	Input ($P1B_3$ to $P1B_0$)
25 26 27 28 29 30	$IDC_2/P1C_3$ $BLK_2/P1C_2$ $IDC_1/P1C_1$ $BLK_1/P1C_0$ IDC_0 BLK_0	IDC (Image Display Controller) character display signal and blanking signal, and port 1C outputs. • IDC_2 to IDC_0 ・ Character display signal outputs • BLK_2 to BLK_0 ・ Character dispaly blanking signal outputs • $P1C_3$ to $P1C_0$ ・ 4-bit CMOS output port	CMOS push-pull	Low-level output (IDC_2 to IDC_0, BLK_2 to BLK_0)

PIN NO.	SYMBOL	FUNCTION	OUTPUT TYPE	AFTER POWER-ON RESET
31	$\overline{\text{VSYNC}}$	Inputs the IDC (Image Display Controller) vertical synchronization signal. Controls timing for output of the IDC character display signal and blanking signal. Should be made an active-low input. Either the rising edge or falling edge may be selected as the valid edge for an interrupt request.	—	Input
32	$\overline{\text{HSYNC}}$	Inputs the IDC (Image Display Controller) horizontal synchronization signal. Controls timing for output of the IDC character display signal and blanking signal. Should be made an active-low input.	—	Input
33	GND	Pins for ground. Pins 33 and 53 are connected within the chip, but should also be connected to the same potential externally taking into consideration the characteristics of the IDC (Image Display Controller).	—	—
34 35	OSCIN OSCOUT	Connect the IDC (Image Display Controller) LC oscillator. This oscillation frequency is used to generate the character display signal. The oscillator is stopped when CE is low.	— CMOS push-pull	—
36	VDD1	Positive power supply. Applies 5 V ±10 % in normal operation mode.	—	—
37 38	XIN XOUT	Connect the system clock oscillator. A 10 MHz crystal resonator or ceramic resonator should be connected.	— CMOS push-pull	—
39	CE	μPD17P401 operation selection signal and reset signal input	—	Input

PIN NO.	SYMBOL	FUNCTION	OUTPUT TYPE	AFTER POWER-ON RESET
40 41 42 43 44 45 46 47	P0A3/SDA P0A2/SCL P0A1/$\overline{SCK0}$ P0A0/SO0 P0B3/SI0 P0B2/RLSSTOP P0B1/ADC P0B0	Port 0A, port 0B, serial interface, clock stop release and A/D converter input/outputs. • P0A3 to P0A0 · 4-bit input/output port · Input/output settable bit-wise • P0B3 to P0B0 · 4-bit CMOS input/output port · Input/output settable bit-wise • SDA, SCL · SDA : Serial data input/output · SCL : Serial clock input/output • $\overline{SCK0}$, SO0, SI0 · $\overline{SCK0}$: Serial clock input/output · SO0 : Serial data output · SI0 : Serial data input • RLSSTOP · Clock stop release • ADC · Analog input to 6-bit resolution A/D converter	N-ch open-drain VDD withstand voltage (P0A3/SDA, P0A2/SCL) CMOS push-pull (P0A1/$\overline{SCK0}$, P0A0/SO0, P0B3, P0B2/RLSSTOP, P0B1, P0B0)	Input (P0A3 to P0A0, P0B3 to P0B0)
48 49	INT0 INT1	Input external interrupt request signal. Either the rising edge or falling edge may be selected as the effective edge for an interrupt request.	—	Input
50	VDD2	Watchdog 32 kHz oscillator power supply.	—	—
51 52	XTIN XTOUT	Connects watchdog 32 kHz oscillator. A 32 kHz crystal resonator should be connected.	— COMS push-pull	—
53	GND	Pin for ground. Pins 33 and 53 are connected within the chip, but should also be connected to the same potential externally taking into condideration the characteristics of the IDC (Image Display Controller).	—	—
54 55 57 58	P2A3/SO1 P2A2/$\overline{SCK1}$ P2A1/SI1 P2A0	Port 2A and serial interface input/outputs. • P2A3 to P2A0 · 4-bit input/output port · Input/output set capability as bit-wise • SO1, $\overline{SCK1}$, SI1 · SO1 : Serial data output · $\overline{SCK1}$: Serial clock input/output · SI1 : Serial data input	N-ch open-drain 16 V withstand voltage (P2A3/SO1, P2A2/$\overline{SCK1}$, P2A1, P2A0)	Input (P2A3 to P2A0)
58 | 61	P0C3 | P0C0	4-bit CMOS input/output port. Input/output set capability as bit-wise.	CMOS push-pull	Input

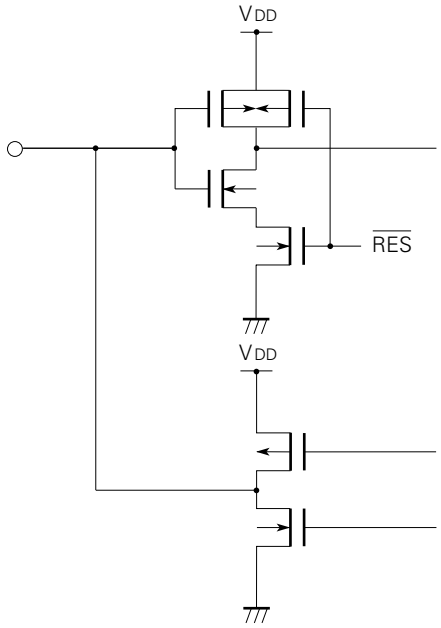
1.2 PROM PROGRAMMING MODE

PIN NO.	SYMBOL	FUNCTION	OUTPUT TYPE
33	GND	Ground. Pins 33 and 53 are connected within the chip, but should also be connected to the same potential externally.	—
36	V_{DD1}	Positive power supply. Applies 6 V in grogram memory write, read and verify operations.	—
37	CLK	PROM programming clock input.	—
48	V_{PP}	Positive power supply for PROM programming. Applies 12.5 V as program voltage in program memory write, read and verify operations.	—
50	V_{DD2}	Positive power supply. Applies 6 V in program memory write, read and verify operations.	—
53	GND	Ground. Pins 33 and 53 are connected within the chip, but should also be connected to the same potential externally.	—
58 | 61	MD3 | MD0	Operating mode selection inputs for PROM programming.	—
62 | 65 66 | 69	D3 | D0 D7 | D4	PROM programming 8-bit data input/output.	CMOS push-pull

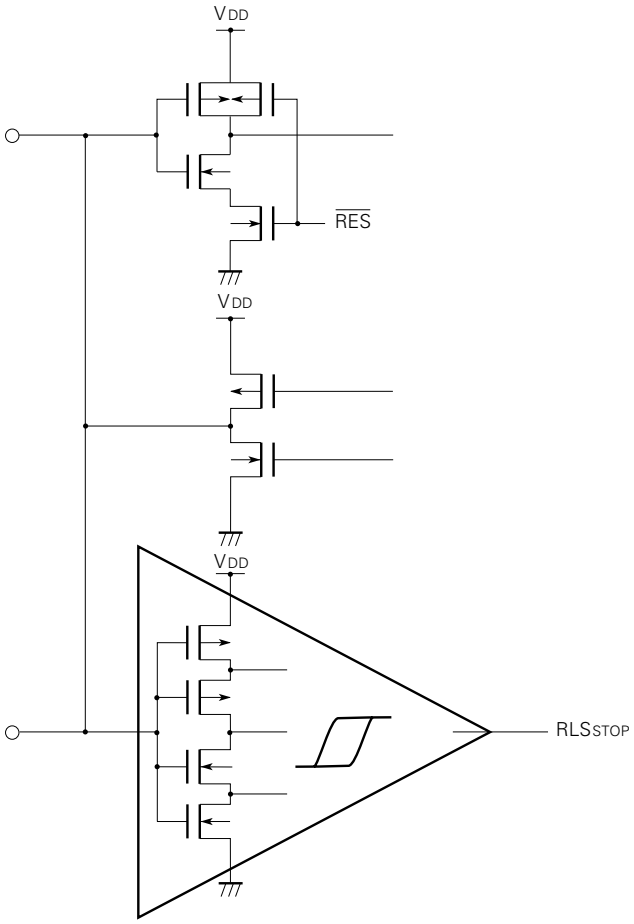
Remarks Pins other than the above are not used in the PROM programming mode. See **"PIN CONFIGURATION (2) PROM PROGRAMMING MODE"** for the disposition of unused pins.

1.3 PIN EQUIVALENT CIRCUITS

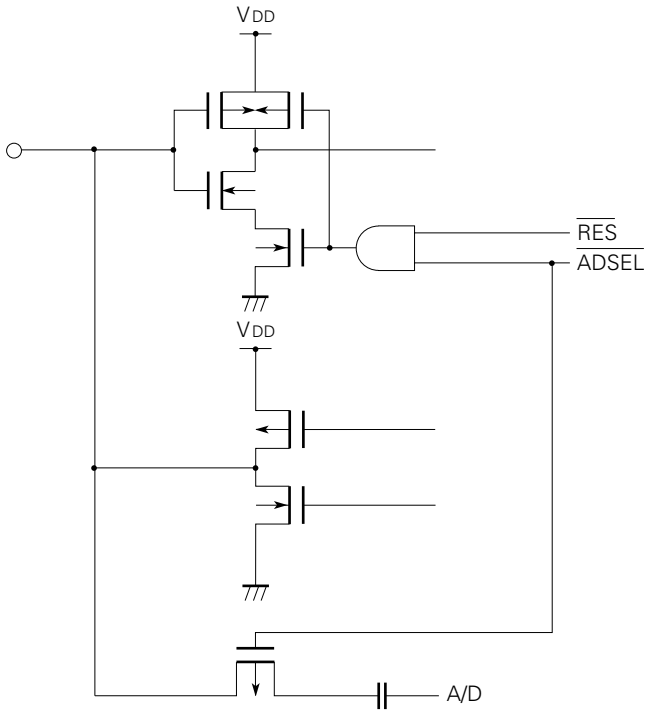
1.3.1 P0A (P0A1/$\overline{SCK0}$, P0A0/SO0) P0B (P0B3/SI0, P0B0) P0C (P0C3, P0C2, P0C1, P0C0) (Input/output)



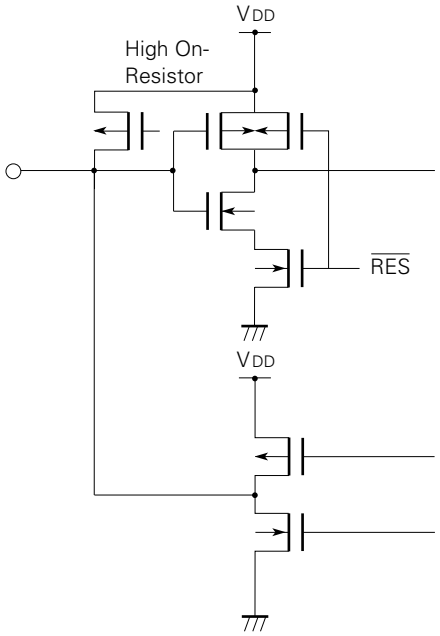
1.3.2 P0B (P0B2/RLSSTOP) Input/output



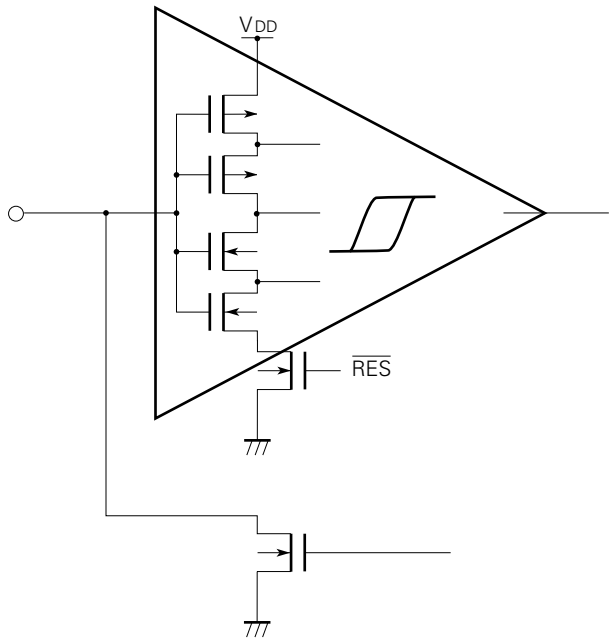
1.3.3 P0B (P0B1/ADC) (Input/output)



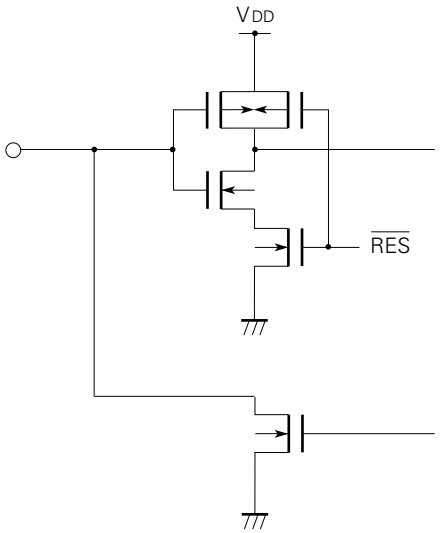
1.3.4 P1B (P1B3, P1B2, P1B1, P1B0) (Input/output)



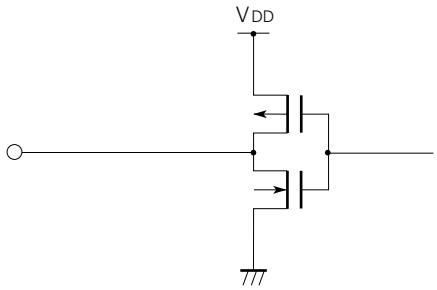
1.3.5 P0A (P0A3/SDA, P0A2/SCL) (Input/output)



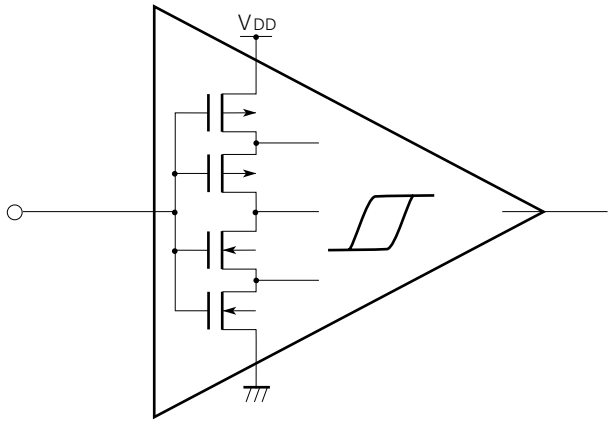
1.3.6 P2A (P2A3/SO1, P2A2/$\overline{SCK_1}$, P2A1/SI1, P2A0) (Input/output)



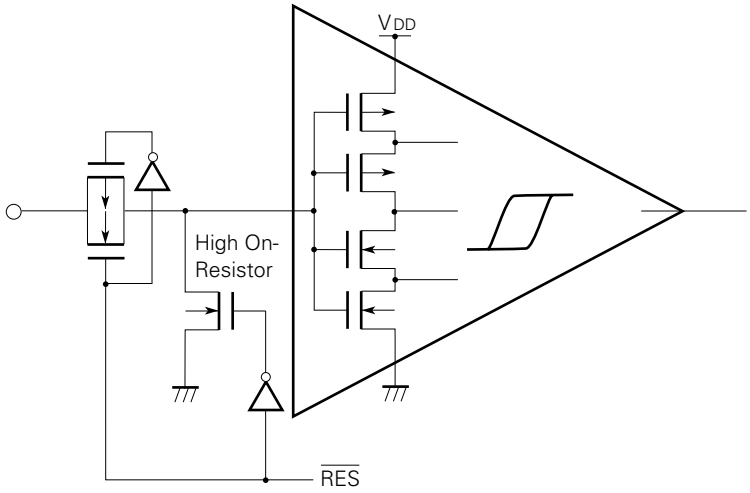
1.3.7 P1C (IDC2/P1C3, BLK2/P1C2, IDC1/P1C1, BLK1/P1C0) IDC0, BLK0 } (Output)



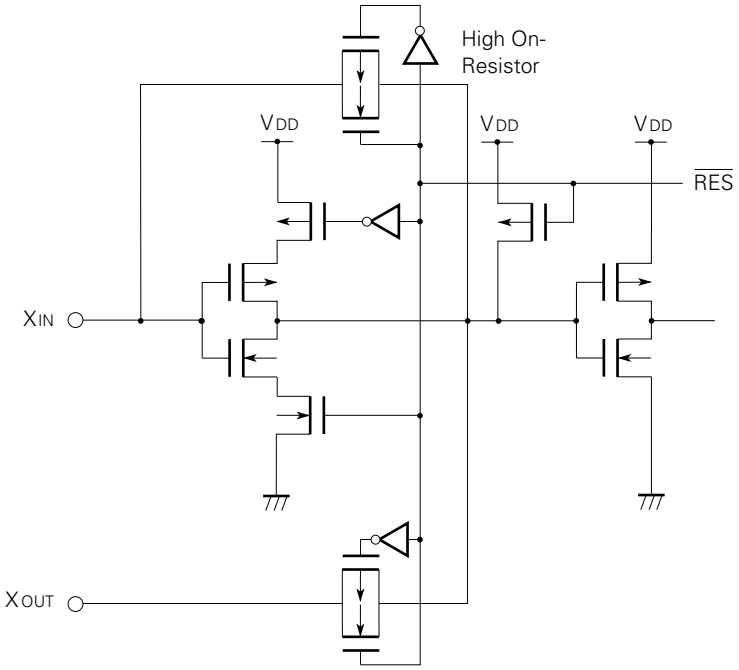
1.3.8 CE, INT1, INT0 (Input)



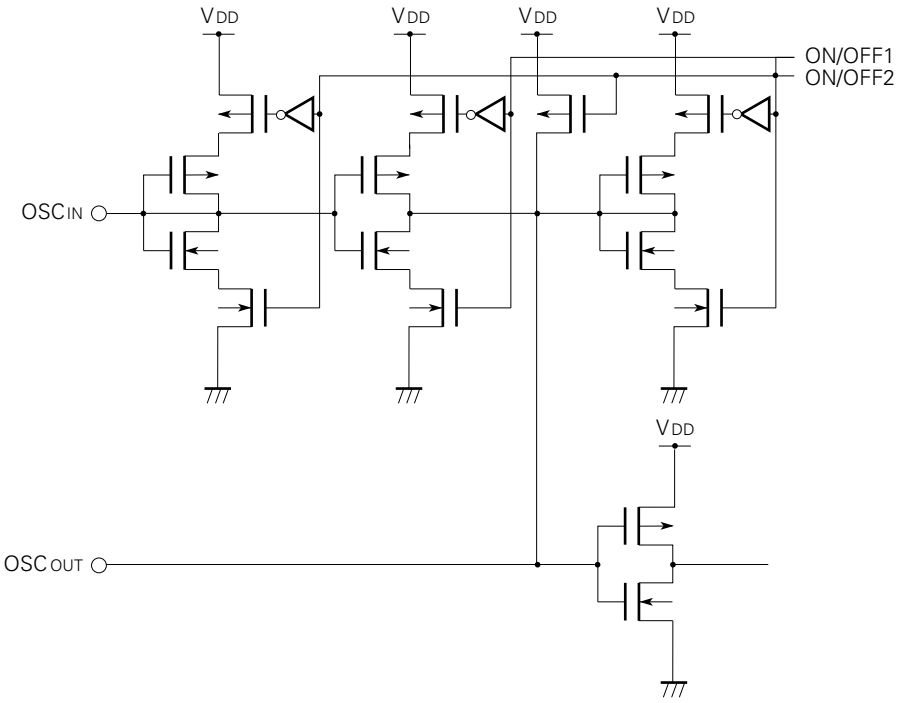
1.3.9 $\overline{\text{VSYNC}}$, $\overline{\text{HSYNC}}$ (Input)



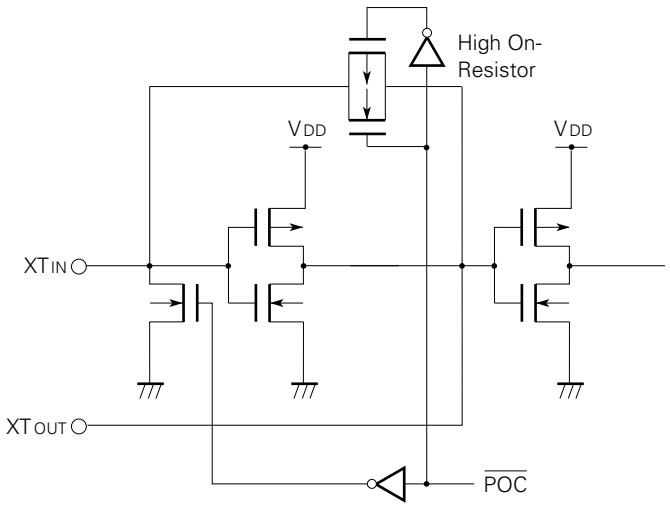
1.3.10 XIN (Input), XOUT (Output)



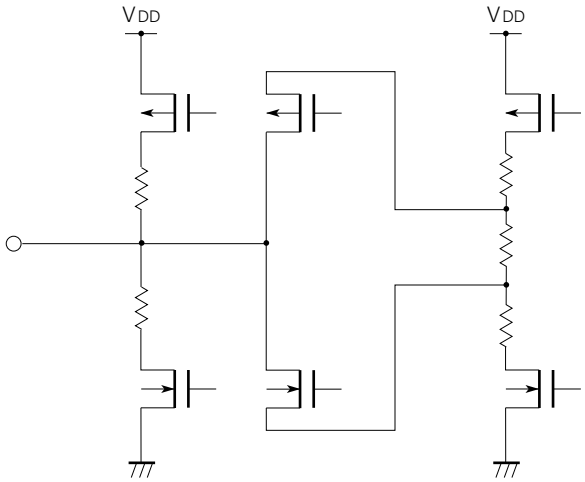
1.3.11 OSCIN (Input), OSCOUT (Output)



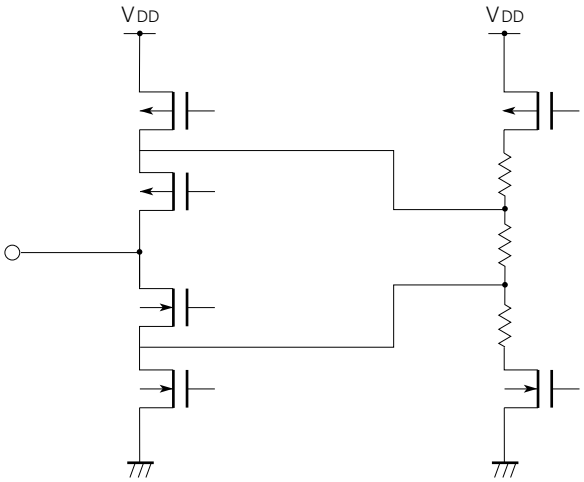
1.3.12 XTIN (Input), XTOUT (Output)



1.3.13 LCD23/COM3, COM2, COM1, COM0 (Output)



1.3.14 LCD35/P0D3/CKOUT-LDC0/KS0* (Output)



* Except LCD23/COM3, COM2, COM1, COM0

2. LIST OF FUNCTIONS

Item \ Product Name		μPD17401	μPD17P401
ROM		12288 × 16 bits (Mask ROM)	12288 × 16 bits (PROM)
	Table reference area	12288 × 16 bits	
RAM		524 × 4 bits	
	Data buffers	4 × 4 bits	
	General registers	16 × 4 bits	
System registers		12 × 4 bits	
Register file		45 × 4 bits	
General-purpose port registers		45 × 4 bits	
	Port registers	9 × 4 bits	
	LCD registers	36 × 4 bits	
Instruction execution time		1.6 μs (with 10 MHz crystal resonator connected)	
Stack levels		7 levels (stack manipulation capability)	
General-purpose ports	Input/output ports	20	
	Input ports	0	
	Output ports	16 (Segment dual-function: 12)	
Image display controller (IDC)		• Display characters: Max. 155 characters on one screen • Display positions : 14 lines × 24 columns • Character set : 255 characters (user-programmable) • Character format : 10 × 15 dots (2-dot space settable between characters) • Character size : Vertical/horizontal size independently settable Vertical (14, 28, 42, 56H) Horizontal (2, 4, 6, 8 μs) • Output pins : Blanking signal independently settable	
LCD controller/driver		• At 1/3 duty, 1/3 bias: 36 segments, 3 common • At 1/4 duty, 1/3 bias: 35 segments, 4 common Frame frequency : 250/n Hz (n = duty) Drive voltage : V_{DD} Key source dual-function pins: 16 pins 12 pins usable as output port (4/4/4/4 pins independently settable)	
Serial interface		• 2 systems (3 channels) 8-bit 3-wire: 2 channels 8-bit 2-wire: 1 channel	
A/D converter		• 6 bits x 1 (successive approximation by software)	
Interrupts		• 5 channels (maskable interrupts) External interrupts: 3 channels (INT_0, INT_1, $\overline{VSYNC}$ pins) Internal interrupts: 2 channels (modulo timer, serial interface 0)	
Timer		• 3 systems Timer carry F/F (100 ms) 8-bit modulo timer (1/2/8/80 kHz) Clock 32 kHz counter (week, day, hour, min., sec. count)	

Item \ Product Name	μPD17401	μPD17P401
Reset	• Power-ON reset (when power is turned on) • Reset via CE pin (CE pin: Low → high) • Power failure detection function	
Standby	• HALT mode: Release by CE, timer carry, interrupt, key input • STOP mode: Release by CE or RLSSTOP pin	
Supply voltage	5 V +10 %	
Package	80-pin plastic QFP (14 × 14 mm)	

3. ONE-TIME PROM (PROGRAM MEMORY) WRITE, READ AND VERIFY OPERATIONS

The program memory incorporated in the μPD17P401 is 24576 × 8-bit electrically programmable one-time PROM. In normal operation, this PROM is accessed in a 16-bit word mode, but in program memory write, read and verify operations the memory is accessed in 8-bit word mode. In this case, the high-order 8 bits of the 16-bit word are allocated to an even address, and the low-order 8 bits to an odd address.

For PROM write, read and verify operations, PROM mode is set and the pins shown in Table 3-1 are used.

Address updating is performed by means of clock input from the CLK pin rather than by address input.

Table 3-1 Pins Used in Program Memory Write, Read and Verify

Pin Name	Function
V_{PP}	Program voltage (12.5 V) application
CLK	Address update clock input
MD0 to MD3	Operating mode selection
D0 to D7	8-bit data input/output
V_{DD1}, V_{DD2}	Supply voltage (6 V) application

Writing to the on-chip PROM is performed using a PROM programmer and dedicated program adapter. The following types of PROM programmer and program adapter should be used:

PROM programmer	AF-9703 (Manufactured by Ando Electric, Co., Ltd.)
	AF-9704 (Manufactured by Ando Electric, Co., Ltd.)
Program adapter	AF-9808D (Manufactured by Ando Electric, Co., Ltd.)

3.1 PROGRAM MEMORY WRITE/READ/VERIFY OPERATING MODES

When +6 V is applied to the V_{DD} pin and +12.5 V to the V_{PP} pin, the μPD17P401 enters a program memory write/read/verify mode.

This mode is one of the operating modes shown in Table 3-2 according to the setting of pins MD0 to MD3.

Input pins not used in the program memory write/read/verify mode should be left open or connected to ground via a pull-down resistor (470 Ω) (see **"PIN CONFIGURATION (2) PROM PROGRAMMING MODE"**).

Table 3-2 Program Memory Write/Read/Verify Operating Modes

Operating Mode Specification						Operating Mode
V_{PP}	V_{DD}	MD0	MD1	MD2	MD3	
+12.5 V	+6 V	H	L	H	L	Program memory address zero-clear
		L	H	H	H	Write mode
		L	L	H	H	Read/verify mode
		H	X	H	H	Program inhibit mode

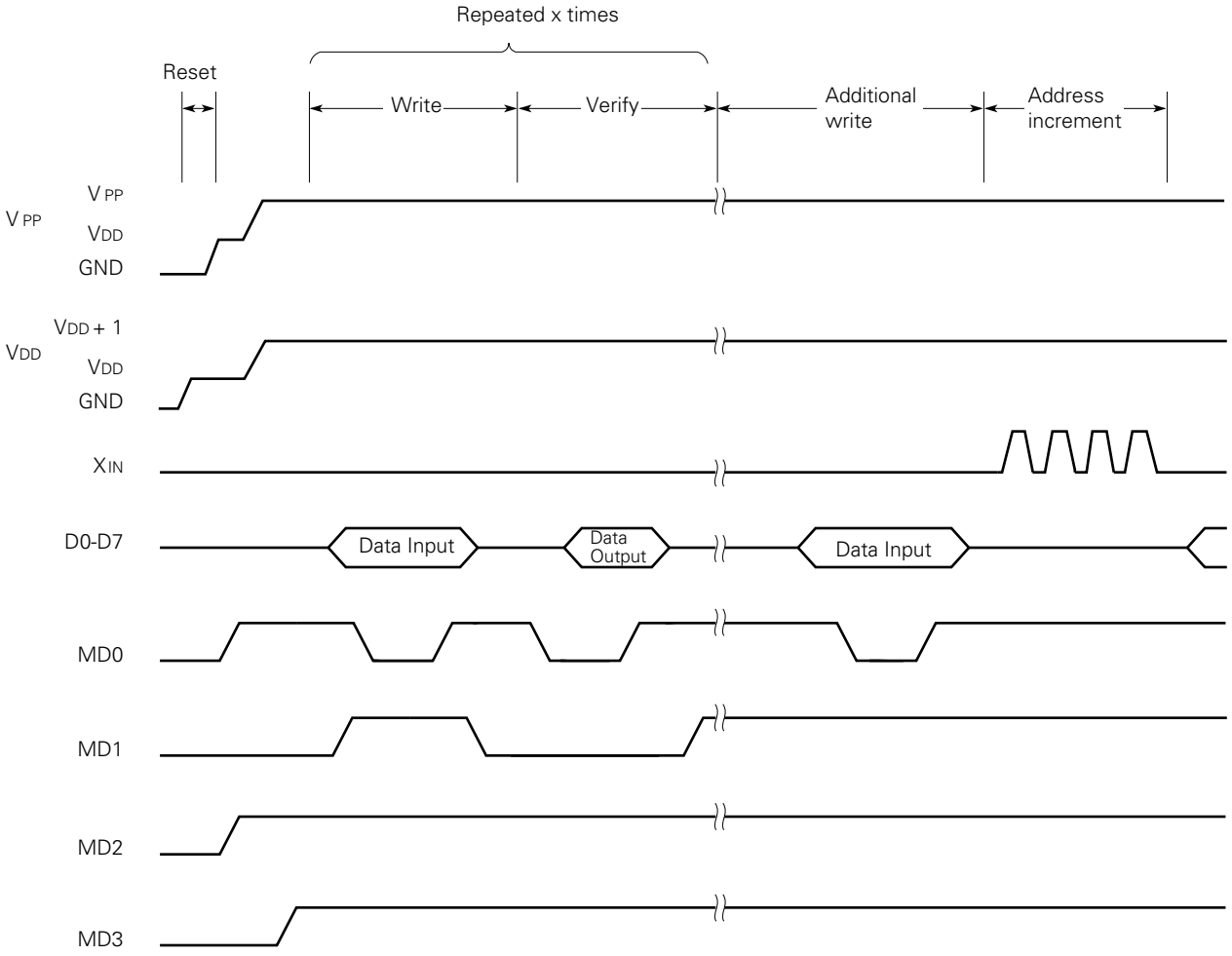
Remarks X: L or H

3.2 PROGRAM MEMORY WRITE PROCEDURE

The procedure for writing to program memory is as shown below, allowing high-speed writing.

(1) Unused pins are connected to GND with a pull-down resistor. The CLK pin is driven low.
(2) 5 V is supplied to the V_{DD} pin. The V_{PP} pin is driven low.
(3) 5 V is supplied to the V_{PP} pin after a 10 μs wait.
(4) The mode setting pin is set to the program memory address zero-clear mode.
(5) 6 V is supplied to V_{DD}, 12.5 V to V_{PP}.
(6) Program inhibit mode.
(7) Data is written in 1 ms write mode.
(8) Program inhibit mode.
(9) Verify mode. If write is successful, go to (10), otherwise repeat (7) to (9).
(10) (Number of times written in (7) to (9): X) × 1 ms additional writes.
(11) Program inhibit mode.
(12) Program memory address is updated (+1) by inputting 4 pulses to the CLK pin.
(13) Steps (7) to (12) are repeated until the last address.
(14) Program memory address zero-clear mode.
(15) V_{DD}/V_{PP} pin voltage is changed to 5 V.
(16) Power OFF.

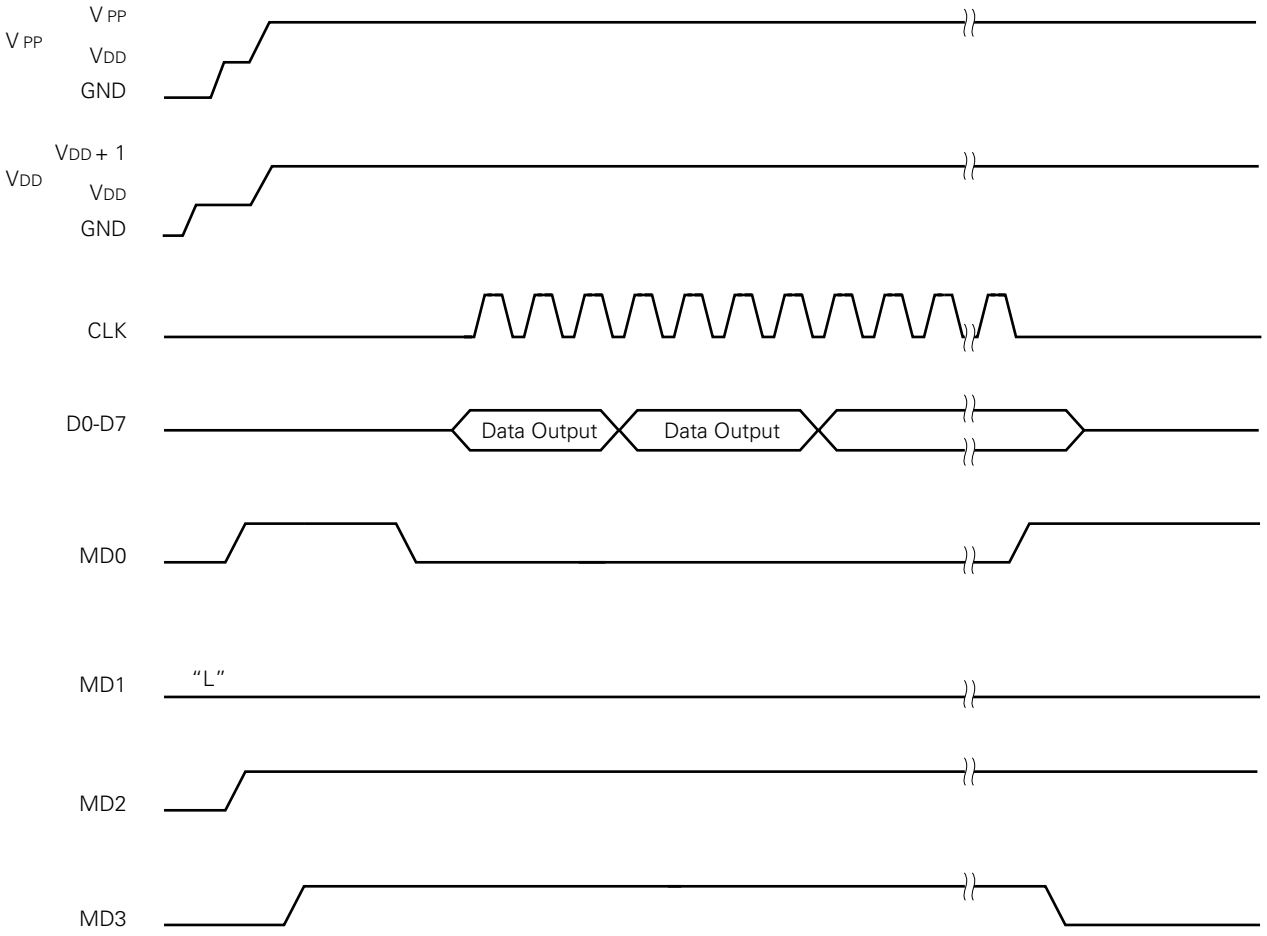
Steps (2) to (12) of this procedure are shown in the following Figure.



3.3 PROGRAM MEMORY READ PROCEDURE

(1) Unused pins are connected to GND with a pull-down resistor. The CLK pin is driven low.
(2) 5 V is supplied to the V_{DD} pin. The V_{PP} pin is driven low.
(3) 5 V is supplied to the V_{PP} pin after a 10 μs wait.
(4) The mode setting pin is set to the program memory address zero-clear mode.
(5) 6 V is supplied to V_{DD}, 12.5 V to V_{PP}.
(6) Program inhibit mode.
(7) Verify mode. When clock pulses are input to the CLK pin, data is output sequentially, one address per 4-input cycle.
(8) Program inhibit mode.
(9) Program memory address zero-clear mode.
(10) V_{DD}/V_{PP} pin voltage is changed to 5 V.
(11) Power OFF.

Steps (2) to (9) of this procedure are shown in the following Figure.



4. ELECTRICAL CHARACTERISTICS (PRELIMINARY)

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Supply Voltage	V_{DD}		–0.3 to +6.0	V
PROM Supply Voltage	V_{PP}		–0.3 to +13.5	V
Input Voltage	V_I		–0.3 to V_{DD} +0.3	V
Output Voltage	V_O	Except $P1A_0$ to $P1A_3$	–0.3 to V_{DD} +0.3	V
Output Withstand Voltage	V_{BDS1}	$P0A_2$, $P0A_3$	V_{DD} +0.3	V
Output Withstand Voltage	V_{BDS2}	$P2A_0$ to $P2A_3$	18.0	V
Output Current High	I_{OH}	1 pin	–10.0	mA
		All pins	–20.0	mA
Output Current Low	I_{OL}	1 pin	10.0	mA
		All pins	20.0	mA
Total Loss	P_T		450	mW
Operating Temperature	T_{opt}		–40 to +85	°C
Storage Temperature	T_{stg}		–55 to +125	°C

RECOMMENDED OPERATING CONDITIONS

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Supply Voltage	V_{DD1}	4.5	5.0	5.5	V	CPU and IDC operating
	V_{DD2}	3.5	5.0	5.5	V	CPU operating, IDC stopped
	V_{DD3}	2.2	5.0	5.5	V	CPU and IDC stopped, clock timer operating
Data Hold Voltage	V_{DDR}	2.2		5.5	V	Crystal oscillation stopped
Supply Voltage Rise Time	t_{RISE}			500	ms	V_{DD} = 0 → 4.5 V
Output Withstand Voltage	V_{BDS}			16.0	V	$P2A_0$ to $P2A_3$
Operating Temperature	T_a	–40		+85	°C	

DC CHARACTERISTICS (T_a = –40 to +85 ˚C, V_{DD} = 4.5 to 5.5 V)

CHARACTERISTICS	SYMBOL	STANDARD VALUES				CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Supply Voltage	V_{DD1}	4.5	5.0	5.5	V	IDC operating
	V_{DD2}	3.5	5.0	5.5	V	CPU operating
	V_{DD3}	3.5	5.0	5.5	V	Clock timer operating
Supply Current	I_{DD1}		2.6		mA	CPU operating, IDC stopped X_{IN} pin sine wavve input (f_{IN} = 10 MHz, V_{IN} = V_{DD}) T_a = 25 ˚C
	I_{DD2}		2.0		mA	CPU operating, IDC stopped, HALT instruction used 20 instruction executed per 1 ms X_{IN} pin sine wave input (f_{IN} = 10 MHz, V_{IN} = V_{DD}) T_a = 25 ˚C
Data Hold Voltage	V_{DDR1}	3.5		5.5	V	Using power failure detection by timer F/F Crystal oscillation
	V_{DDR2}	2.2		5.5	V	Using power failure detection by timer F/F Crystal oscillation stopped
	V_{DDR3}	2.0		5.5	V	Data memory (RAM) hold
Data Hold Current	I_{DDR1}		4	6	μA	Crystal oscillation stopped, clock timer operating T_a = 25 ˚C
	I_{DDR2}		2	6	μA	Crystal oscillation stopped, clock timer operating V_{DD} = 5.0 V, Ta = 25 ˚C
	I_{DDR3}		6	8	μA	Crystal oscillation stopped, clock timer stopped T_a = 25 ˚C
	I_{DDR4}		5	6	μA	Crystal oscillation stopped, clock timer stopped V_{DD} = 5.0 V, T_a = 25 ˚ C
Output Voltage Medium	V_{OMH1}	3.1	3.3	3.5	V	COM_0, COM_1, COM_3 V_{DD} = 5 V
	V_{OMM1}	2.3	2.5	2.7	V	COM_0, COM_1, COM_3 V_{DD} = 5 V
	V_{OML1}	1.4	1.6	1.8	V	COM_0, COM_1, COM_3 V_{DD} = 5 V
Input Voltage High	V_{IH1}	0.7 V_{DD}			V	$P0A_0$ to $P0A_3$, $P0B_0$ to $P0B_3$, $P0C_0$ to $P0C_3$, $P2A_0$ to $P2A_3$
	V_{IH2}	0.6 V_{DD}			V	$P1B_0$ to $P1B_3$
	V_{IH3}	0.8 V_{DD}			V	CE, INT_0, INT_1, $\overline{H_{SYNC}}$, $\overline{V_{SYNC}}$

CHARACTERISTICS	SYMBOL	STANDARD VALUES				CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Input Voltage Low	V_{IL1}			0.3 V_{DD}	V	$P0A_0$ to $P0A_3$, $P0B_0$ to $P0B_3$, $P0C_0$ to $P0C_3$, $P2A_0$ to $P2A_3$
	V_{IL2}			0.3 V_{DD}	V	$P1B_0$ to $P1B_3$
	V_{IL3}			0.2 V_{DD}	V	CE, INT_0, INT_1, $\overline{HSYNC}$, $\overline{VSYNC}$
Output Current High	I_{OH1}	–1.0		–5.0	mA	* V_{OH} = V_{DD} – 1 V
	I_{OH2}	–0.5	–1.0	–1.5	mA	LCD_0 to LCD_{35} V_{OH} = V_{DD} – 1 V
	I_{OH3}	–0.1	–0.8		mA	$P1B_0$ to $P1B_3$ pulled high V_{OH} = GND
Output Current Low	I_{OL1}	1.0			mA	* V_{OL} = 1 V
	I_{OL2}	1.0			mA	LCD_0 to LCD_{35} V_{OL} = 1 V
	I_{OL3}	1.0			mA	$P2A_0$ to $P2A_3$ V_{OL} = 1 V
Input Current High	I_{IH1}	0.1	1.3		mA	X_{IN} pulled low V_{IH} = V_{DD}
	I_{IH2}	0.1	1.3		mA	OSC_{IN} pulled low V_{IH} = V_{DD}
Output Off Leak Current	I_{L1}			500		$P0A_2$, $P0A_3$ V_{OH} = V_{DD}
	I_{L2}			500		$P2A_0$ to $P2A_3$ V_{OH} = 12 V
Output Withstand Voltage	V_{BDS}	0		16	V	$P2A_0$ to $P2A_3$

* $P0A_2$, $P0A_3$, $P0B_0$ to $P0B_3$, $P0C_0$ to $P0C_3$, $P1A_2$, $P1A_3$, $P1B_0$ to $P1B_3$, $P1C_0$ to $P1C_3$, $P1D_0$ to $P1D_3$, IDC_0, BLK_0

AC CHARACTERISTICS (T_a = –40 to +85 °C, V_{DD} = 4.5 to 5.5 V)

CHARACTERISTICS	SYMBOL	STANDARD VALUES				CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operating Frequency	f_{IN1}		10.0		MHz	Recommended CPU operation oscillation
	f_{IN2}			1.0	kHz	SCL, $\overline{SCK_0}$, $\overline{SCK_1}$ external clock frequency
A/D Conversion Resolution				4	bit	
A/D Conversion Total Error			±1.0	±1.5	LSB	T_a = –10 to +50 °C
SIO External Clock Frequency			±1.0	1000	kHz	SIO0/SIO1 COM mode T_a = –10 to +50 °C

REFERENCE CHARACTERISTICS

CHARACTERISTICS	SYMBOL	STANDARD VALUES				CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Supply Current	I_{DD3}		5		mA	CPU and IDC operating V_{DD} = 5.0 V, T_a = 25 °C
Output Current High	I_{OH4}		–0.2		mA	COM_0, COM_1, COM_2 $V_{OH} = V_{DD} - 1$ V
Output Current Medium	I_{OM1}		–20		μA	COM_0, COM_1, COM_2 $V_{OM} = V_{DD}$
	I_{OM2}		20		μA	COM_0, COM_1, COM_2 V_{OM} = 0 V
Output Current Low	I_{OL5}		0.2		mA	COM_0, COM_1, COM_2 V_{OL} = 1 V

DC PROGRAMMING CHARACTERISTICS (T_a = 25 °C, V_{DD} = 6.0 ±0.25 V, V_{PP} = 12.5 ±0.5 V)

CHARACTERISTICS	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Input Voltage High	V_{IH1}	0.7 V_{DD}		V_{DD}	V	Except CLK
	V_{IH2}	V_{DD} –0.5		V_{DD}	V	CLK
Input Voltage Low	V_{IL1}	0		0.3 V_{DD}	V	Except CLK
	V_{IL2}	0		0.4	V	CLK
Input Leakage Current	I_{LI}			10	μA	$V_{IN} = V_{IL}$ or V_{IH}
Output Voltage High	V_{OH}	V_{DD} –1.0			V	I_{OH} = –1 mA
Output Voltage Low	V_{OL}			1.0	V	I_{OL} = 1 mA
V_{DD} Supply Current	I_{DD}			30	mA	
V_{PP} Supply Current	I_{PP}			30	mA	MD0 = V_{IL}, MD1 = V_{IH}

Note 1 Ensure that V_{PP} does not exceed +13.5 V including overshoot.

2 Ensure that V_{DD} is applied before V_{PP} and cut off after V_{PP}.

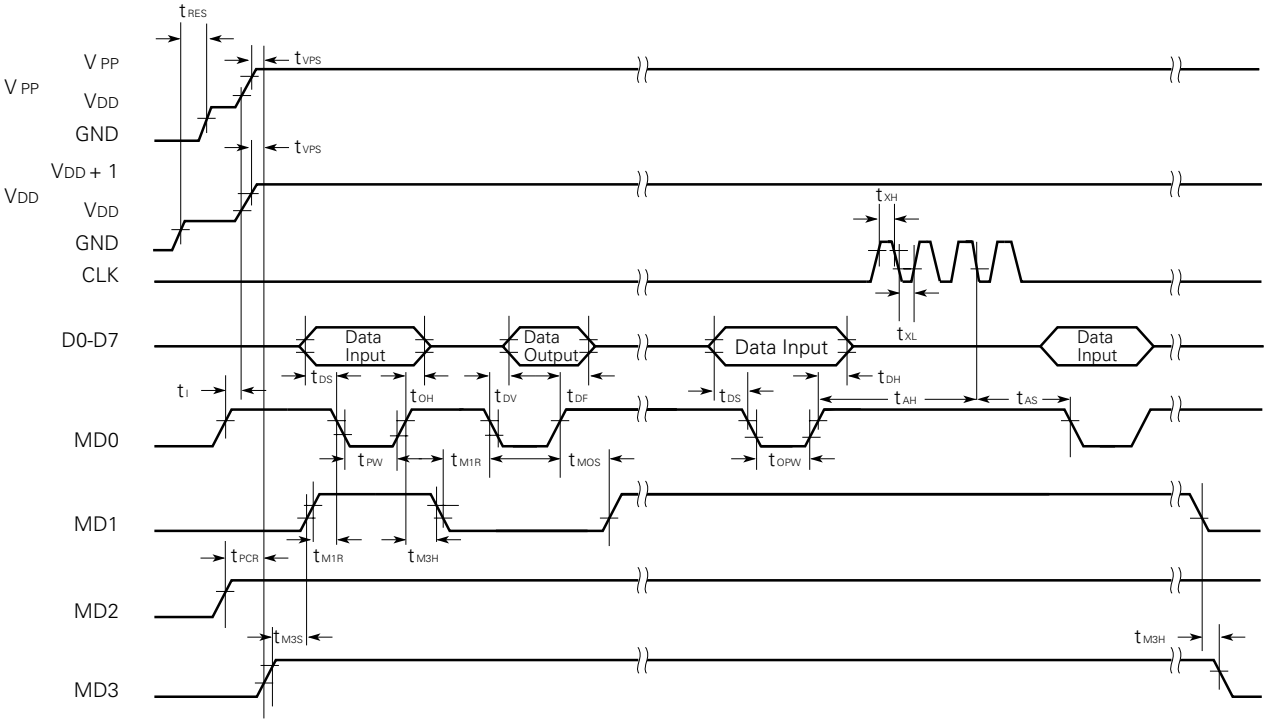
AC PROGRAMMING CHARACTERISTICS (T_a = 25 °C, V_{DD} = 6.0 ±0.25 V, V_{PP} = 12.5 ±0.5 V)

CHARACTERISTICS	SYMBOL	*1	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Address Setup Time *2 (to MD0↓)	t_{AS}	t_{AS}	2			μs	
MD1 Setup Time (to MD0↓)	t_{M1S}	t_{OES}	2			μs	
Data Setup Time (to MD0↓)	t_{DS}	t_{DS}	2			μs	
Address Hold Time *2 (from MD0↑)	t_{AH}	t_{AH}	2			μs	
Data Hold Time (from MD0↑)	t_{DH}	t_{DH}	2			μs	
Data Output Float Delay Time From MD0↑	t_{DF}	t_{DF}	0		130	ns	
V_{PP} Setup Time (to MD3↑)	t_{VPS}	t_{VPS}	2			μs	
V_{DD} Setup Time (to MD3↑)	t_{VDS}	t_{VCS}	2			μs	
Initial Program Pulse Width	t_{PW}	t_{PW}	0.95	1.0	1.05	ms	
Additional Program Pulse Width	t_{OPW}	t_{OPW}	0.95		21.0	ms	
MD0 Setup Time (to MD1↑)	t_{MOS}	t_{CES}	2			μs	
Data Output Delay Time From MD0↓	t_{DV}	t_{DV}			1	μs	MD0 = MD1 = V_{IL}
MD1 Hold Time (from MD0↑)	t_{M1H}	t_{OEH}	2			μs	$t_{M1H} + t_{M1R} \geqq 50$ μs
MD1 Recovery Time (from MD0↓)	t_{M1R}	t_{OR}	2			μs	
Program Counter Reset Time	t_{PCR}	–	10			μs	
CLK Input High/Low-Level Width	t_{XH}, t_{XL}	–	0.125			μs	
CLK Input Frequency	f_X	–			4.19	MHz	
Initial Mode Setting Time	t_I	–	2			μs	
MD3 Setup Time (to MD1↑)	t_{M3S}	–	2			μs	
MD3 Hold Time (from MD1↓)	t_{M3H}	–	2			μs	
MD3 Setup Time (to MD0↓)	t_{M3SR}	–	2			μs	For program memory read
Data Output Delay Time From Address *2	t_{DAD}	t_{ACC}	2			μs	For program memory read
Data Output Hold Time From Address *2	t_{HAD}	t_{OH}	0		130	ns	For program memory read
MD3 Hold Time (from MD0↑)	t_{M3HR}	–	2			μs	For program memory read
Data Output Float Delay Time From MD3↓	t_{DFR}	–	2			μs	For Program memory read
Reset Setup Time	t_{RES}		10			μs	

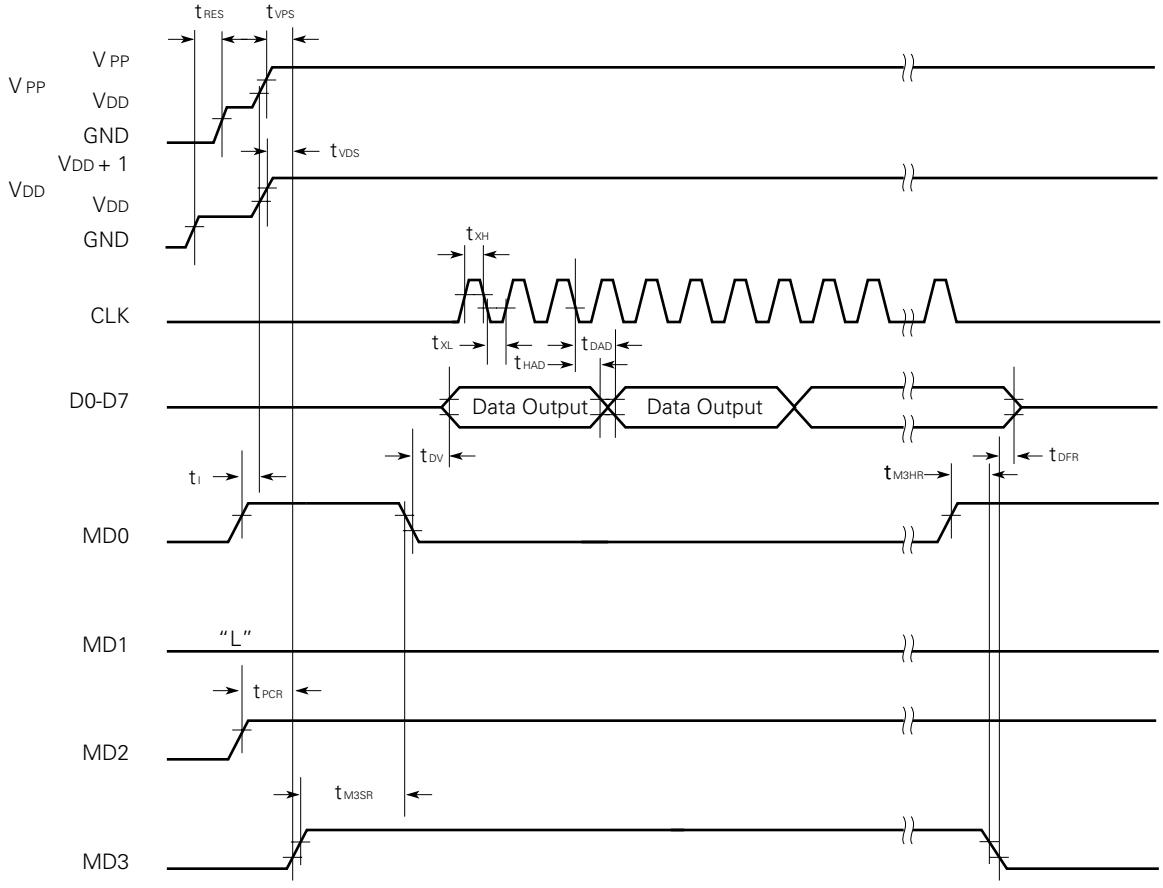
***1** Corresponding μPD27C256 symbol.

2 Internal address incrementing (+1) is performed on the 3rd falling edge of CLK with 4 clock pulses as one cycle. Internal addresses are not connected to pins.

Program Memory Write Timing

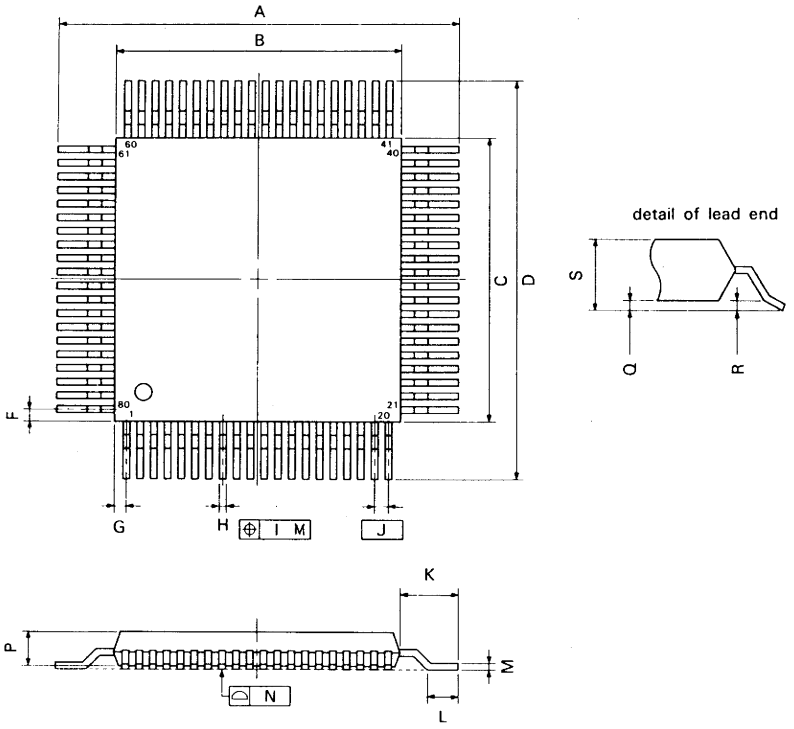


Program Memory Read Timing



5. PACKAGE DIMENSION

80PIN PLASTIC QFP (□14)



S80GC-65-3B9-1

NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	$17.2^{\pm 0.4}$	$0.677^{\pm 0.016}$
B	$14.0^{\pm 0.2}$	$0.551^{+0.009}_{-0.008}$
C	$14.0^{\pm 0.2}$	$0.551^{+0.009}_{-0.008}$
D	$17.2^{\pm 0.4}$	$0.677^{\pm 0.016}$
F	0.8	0.031
G	0.8	0.031
H	$0.30^{\pm 0.10}$	$0.012^{+0.004}_{-0.005}$
I	0.13	0.005
J	0.65 (T.P.)	0.026 (T.P.)
K	$1.6^{\pm 0.2}$	$0.063^{\pm 0.008}$
L	$0.8^{\pm 0.2}$	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.15	0.006
P	2.7	0.106
Q	$0.1^{\pm 0.1}$	$0.004^{\pm 0.004}$
R	$0.1^{\pm 0.1}$	$0.004^{\pm 0.004}$
S	3.0 MAX.	0.119 MAX.

APPENDIX. DEVELOPMENT TOOLS

The following support tools are available for program development using the μPD17P401.

Hardware		
Name	Description	Ordering Code
In-circuit emulator (IE-17K)	The IE-17K is an in-circuit emulator which can be used with all models in the 17K series. For μPD17P401 program development, the IE-17K is used in conjunction with the SE-17401 system evaluation board. As the IE-17K features RAM-based operation, immediate program additions and amendments can be made by connecting a console to the IE-17K. Moreover, use of the SIMPLEHOST™ support software provides a higher-level program development environment.	IE-17K
SE board (SE-17401)	The SE-17401 is a μPD17P401 system evaluation board used together with the IE-17K or by itself.	SE-17401
Probe (EP-17401GC)	The EP-17401GC is a probe for connection of the target system to the SE-17401.	EP-17401GC
Conversion socket (EV-9200G-80)	The EV-9200G-80 is a socket for connection of the target system to the EP-17401GC.	EV-9200G-80
PROM programmer (AF-9703) (AF-9704)	Main PROM programmer unit. For the μPD17P401, the programmer is used in conjunction with the AF-9808D special-purpose program adapter (Ver.5 or later should be used).	AF-9703 AF-9704 (manufactured by Ando Electric, Co., Ltd.)
Program adapter (AF-9808D)	Special-purpose program adapter for the μPD17P401, used in conjunction with the AF-9703 or AF-9704.	AF-9808D (manufactured by Ando Electric, Co., Ltd.)

Remarks Please contact Ando Electric, Co., Ltd. for details of the PROM programmers and program adapter.

Software						
Name	Description	Host Machine	OS		Supply Medium	Ordering Code
17K series assembler (AS17K)	AS17K is the assembler for use with the entire 17K series. For μPD17P401 program development, AS17K is used in conjunction with the device file (AS17401).	PC-9800 series	MS-DOS™ (Ver.3.1 Ver.3.30 Ver.3.30A)		5-inch 2HD	μS5A10AS17K
					3.5-inch 2HD	μS5A13AS17K
		IBM PC/AT™	PC DOS™ (Ver.3.1)		5-inch 2D	μS7B11AS17K
Device file* (AS17401)	AS17401 is the device file for the μPD17401 and μPD17P401, and is used together with the common 17K series assembler (AS17K).	PC-9800 series	MS-DOS (Ver.3.1 Ver.3.30 Ver.3.30A)		5-inch 2HD	μS5A10AS17401
					3.5-inch 2HD	μS5A13AS17401
		IBM PC/AT	PC DOS (Ver.3.1)		5-inch 2D	μS7B11AS17401
Support software (SIMPLE-HOST)	SIMPLEHOST is software which implements the man-machine interface under MS-WINDOWS™ during program development using the IE-17K and a personal computer.	PC-9800 series IBM PC/AT	MS-DOS	MS-WINDOWS (Ver.2.1 Ver.2.11)	5-inch 2HD	μS5A10IE17K
					3.5-inch 2HD	μS5A13IE17K
			PC DOS		5-inch 2D	μS7B11IE17K

* Under development

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[MEMO]