NEC

MOS INTEGRATED CIRCUIT

μPD8891

(5340 × 5340) PIXELS × 3 + 2670 PIXELS × 3 COLOR CCD LINEAR IMAGE SENSOR

DESCRIPTION

The μPD8891 is a color CCD (Charge Coupled Device) linear image sensor which changes optical images to electrical signal and has the function of color separation.

The μPD8891 has 3 rows of (5340+5340) staggered pixels, and each row has a dual-sided readout type of charge transfer register, and has 3 rows of 2670 pixels, and each row has a single-sided readout type of charge transfer register. And it has reset feed-through level clamp circuits and voltage amplifiers. Therefore, it is suitable for 1200 dpi/A4 color image scanners, color facsimiles and so on.

FEATURES

• Valid photocell	: (5340+5340) pixels × 3 + 2670 pixels × 3
• Photocell pitch	: 5.25 μm (1200 dpi), 10.5 μm (300 dpi)
• Photocell size	: 5.25 × 5.25 μm^2 (1200 dpi), 10.5 × 8 μm^2 (300 dpi)
• Line spacing	: [1200 dpi sensor] 52.5 μm (10 lines) Red line - Green line, Green line - Blue line 10.5 μm (2 lines) Odd line – Even line (for each color) [300 dpi sensor] 42 μm (4 lines) Red line - Green line, Green line - Blue line
• Color filter	: Primary colors (red, green and blue), pigment filter (with light resistance 10^7 lx•hour)
• Resolution	: 48 dot/mm A4 (210 × 297 mm) size (shorter side) 1200 dpi US letter (8.5” × 11”) size (shorter side)
• Drive clock level	: CMOS output under 5 V operation
• Data rate	: 5 MHz Max.
• Power supply	: +12 V
• On-chip circuits	: Reset feed-through level clamp circuits Voltage amplifiers

ORDERING INFORMATION

Part Number	Package
μPD8891CY-A	CCD linear image sensor 22-pin plastic DIP (10.16 mm (400))

<R> **Remark** The μPD8891CY-A is a lead-free product.

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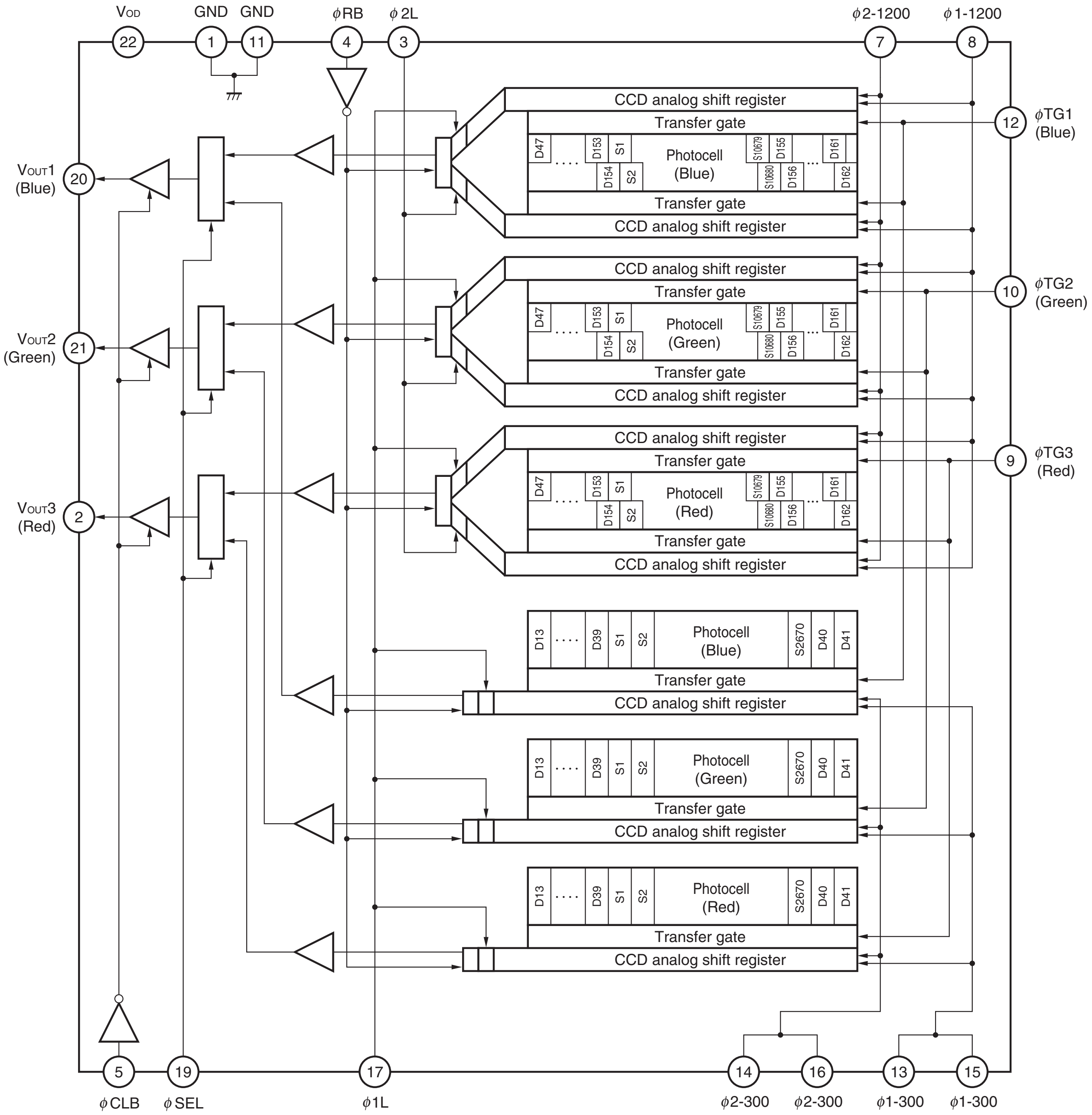
The mark <R> shows major revised points.
The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.

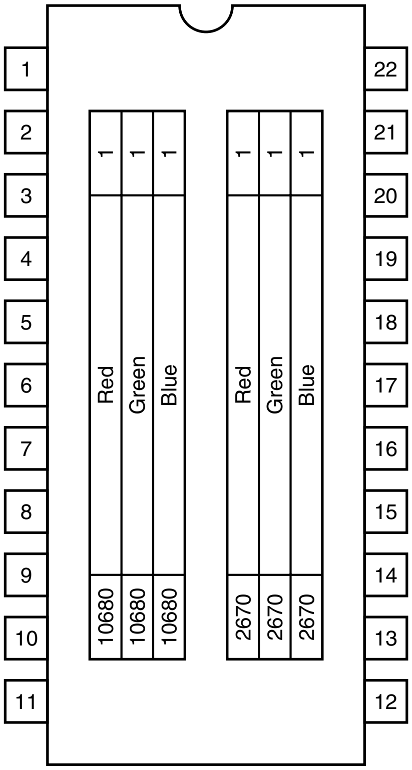
BLOCK DIAGRAM



PIN CONFIGURATION (Top View)

CCD linear image sensor 22-pin plastic DIP (10.16 mm (400))

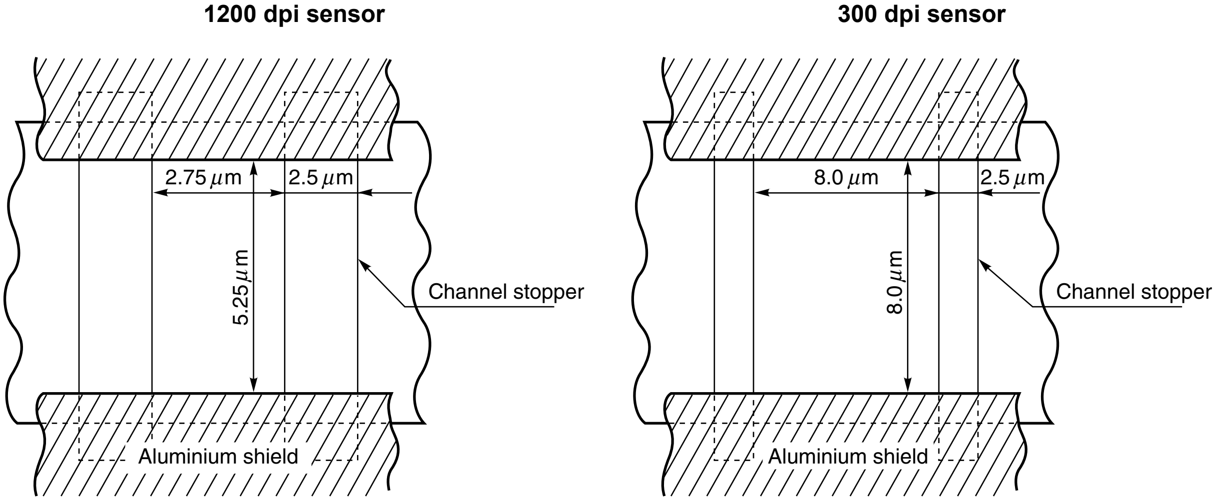
- μPD8891CY-A



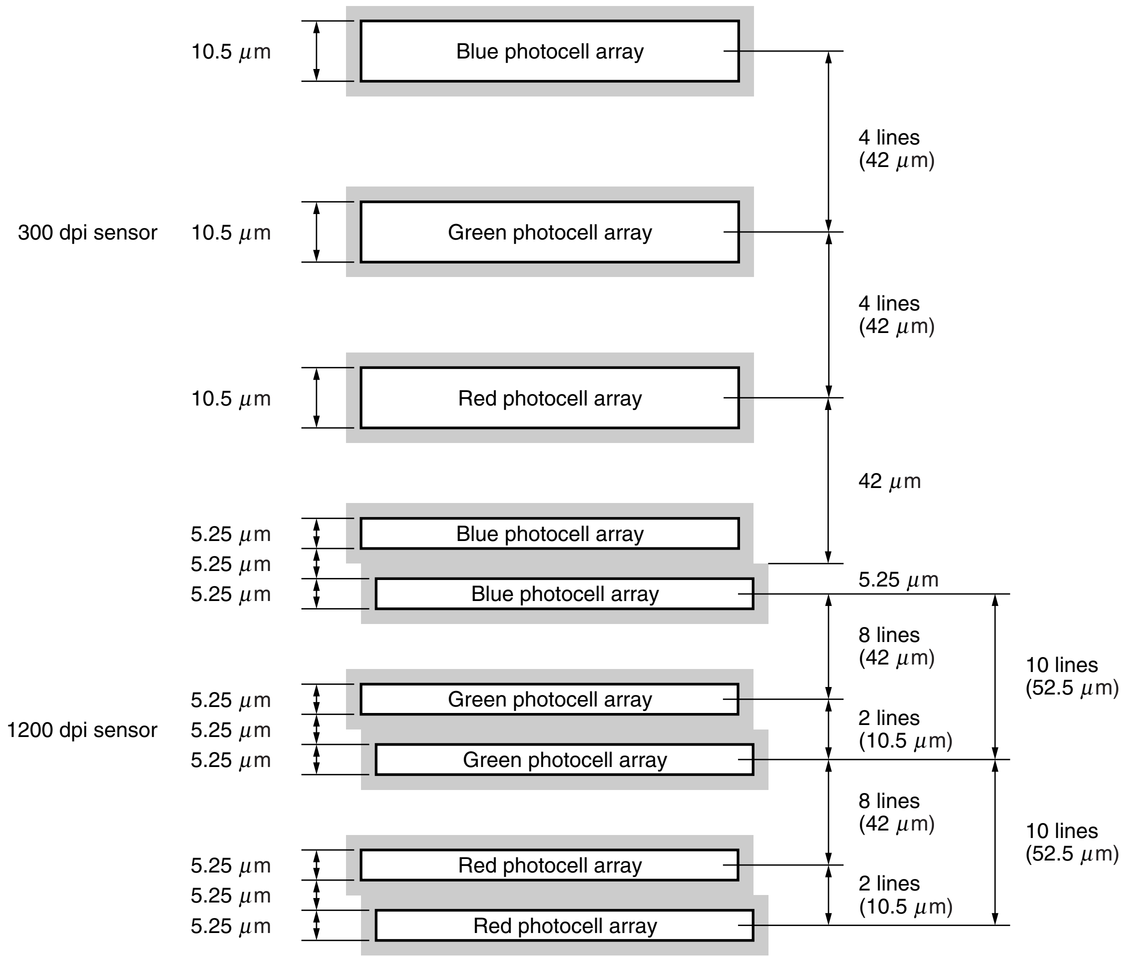
Name	Symbol	Pin	Pin	Symbol	Name
Ground	GND	1	22	V_{OD}	Output drain voltage
Output signal 3 (Red)	$V_{OUT}3$	2	21	$V_{OUT}2$	Output signal 2 (Green)
Last stage shift register clock 2	ϕ2L	3	20	$V_{OUT}1$	Output signal 1 (Blue)
Reset gate clock	ϕRB	4	19	ϕSEL	300/1200 dpi select input
Reset feed-through level level clamp clock	ϕCLB	5	18	NC	No connection
No connection	NC	6	17	ϕ1L	Last stage shift register clock 1
Shift register clock 2 (for 1200 dpi)	ϕ2-1200	7	16	ϕ2-300	Shift register clock 2 (for 300 dpi)
Shift register clock 1 (for 1200 dpi)	ϕ1-1200	8	15	ϕ1-300	Shift register clock 1 (for 300 dpi)
Transfer gate clock 3 (for Red)	ϕTG3	9	14	ϕ2-300	Shift register clock 2 (for 300 dpi)
Transfer gate clock 2 (for Green)	ϕTG2	10	13	ϕ1-300	Shift register clock 1 (for 300 dpi)
Ground	GND	11	12	ϕTG1	Transfer gate clock 1 (for Blue)

Caution Connect the No connection pins (NC) to GND.

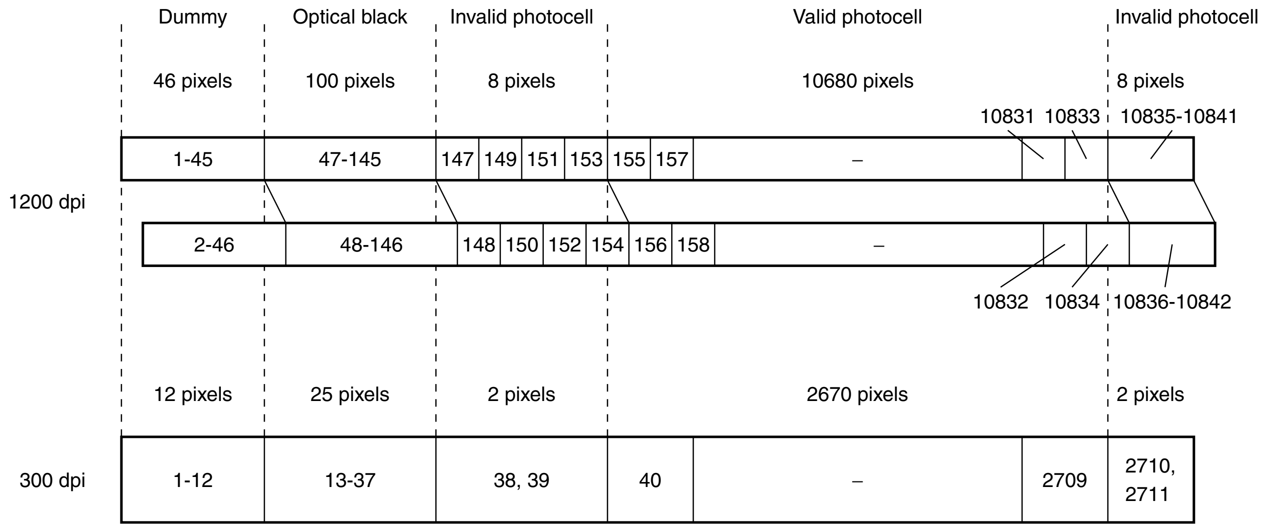
PHOTOCELL STRUCTURE DIAGRAM



PHOTOCELL ARRAY STRUCTURE DIAGRAM 1 (Line Spacing)



PHOTOCELL ARRAY STRUCTURE DIAGRAM 2 (The Relation of the Photocell Array)



ABSOLUTE MAXIMUM RATINGS ($T_A = +25°C$)

Parameter	Symbol	Ratings	Unit
Output drain voltage	V_{OD}	–0.3 to +15	V
Shift register clock voltage	$V_{\phi 1\text{-}300}$, $V_{\phi 1\text{-}1200}$, $V_{\phi 1L}$, $V_{\phi 2\text{-}300}$, $V_{\phi 2\text{-}1200}$, $V_{\phi 2L}$	–0.3 to +8	V
Reset gate clock voltage	$V_{\phi RB}$	–0.3 to +8	V
Reset feed-through level clamp clock voltage	$V_{\phi CLB}$	–0.3 to +8	V
300/1200 dpi select signal voltage	$V_{\phi SEL}$	–0.3 to +8	V
Transfer gate clock voltage	$V_{\phi TG1}$ to $V_{\phi TG3}$	–0.3 to +8	V
Operating ambient temperature Note	T_A	0 to +60	°C
Storage temperature	T_{stg}	–40 to +70	°C

Note Use at the condition without dew condensation.

Caution **Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

RECOMMENDED OPERATING CONDITIONS ($T_A = +25°C$)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Output drain voltage	V_{OD}	11.4	12.0	12.6	V
Shift register clock high level	$V_{\phi 1\text{-}300H}$, $V_{\phi 1\text{-}1200H}$, $V_{\phi 1LH}$, $V_{\phi 2\text{-}300H}$, $V_{\phi 2\text{-}1200H}$, $V_{\phi 2LH}$	4.75	5.0	5.25	V
Shift register clock low level	$V_{\phi 1\text{-}300L}$, $V_{\phi 1\text{-}1200L}$, $V_{\phi 1LL}$, $V_{\phi 2\text{-}300L}$, $V_{\phi 2\text{-}1200L}$, $V_{\phi 2LL}$	–0.3	0	+0.25	V
Reset gate clock high level	$V_{\phi RBH}$	4.5	5.0	5.5	V
Reset gate clock low level	$V_{\phi RBL}$	–0.3	0	+0.5	V
Reset feed-through level clamp clock high level	$V_{\phi CLBH}$	4.5	5.0	5.5	V
Reset feed-through level clamp clock low level	$V_{\phi CLBL}$	–0.3	0	+0.5	V
300/1200 dpi select signal high level	$V_{\phi SELH}$	4.5	5.0	5.5	V
300/1200 dpi select signal low level	$V_{\phi SELL}$	–0.3	0	+0.5	V
Transfer gate clock high level	$V_{\phi TG1H}$ to $V_{\phi TG3H}$	4.75	$V_{\phi 1\text{-}300H}$, $V_{\phi 1\text{-}1200H}$ Note	$V_{\phi 1\text{-}300H}$, $V_{\phi 1\text{-}1200H}$ Note	V
Transfer gate clock low level	$V_{\phi TG1L}$ to $V_{\phi TG3L}$	–0.3	0	+0.15	V
Data rate	$f_{\phi RB}$	–	2.0	5.0	MHz

Note When Transfer gate clock high level ($V_{\phi TG1H}$ to $V_{\phi TG3H}$) is higher than shift register clock high level ($V_{\phi 1\text{-}300H}$, $V_{\phi 1\text{-}1200H}$), image lag can increase.

ELECTRICAL CHARACTERISTICS

(T_A = +25°C, V_{OD} = 12 V, data rate ($f_{\phi RB}$) = 2 MHz, storage time = 11.0 ms, input signal clock = 5 $V_{p\text{-}p}$,
light source : 3200 K halogen lamp + C-500S (infrared cut filter, t = 1 mm) + HA-50 (heat absorbing filter, t = 3 mm))

Parameter		Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Saturation voltage		V_{sat}	300 dpi	2.5	2.7	–	V
			1200 dpi	2.0	2.4	–	V
Saturation exposure	Red	SER	300 dpi	–	0.167	–	lx•s
			1200 dpi	–	0.445	–	lx•s
	Green	SEG	300 dpi	–	0.176	–	lx•s
			1200 dpi	–	0.470	–	lx•s
	Blue	SEB	300 dpi	–	0.274	–	lx•s
			1200 dpi	–	0.732	–	lx•s
Photo response non-uniformity		PRNU	V_{OUT} = 1.0 V	–	6	20	%
Average dark signal		ADS	Light shielding 300 dpi	–	0.4	4.0	mV
			Light shielding 1200 dpi	–	0.2	2.0	mV
Dark signal non-uniformity		DSNU	Light shielding 300 dpi	–	4.0	12.0	mV
			Light shielding 1200 dpi	–	2.0	6.0	mV
Power consumption		P_W		–	300	480	mW
Output impedance		Z_O		–	0.4	1.0	kΩ
Response	Red	R_R	300 dpi	11.32	16.17	21.02	V/lx•s
			1200 dpi	3.77	5.39	7.01	V/lx•s
	Green	R_G	300 dpi	10.73	15.33	19.93	V/lx•s
			1200 dpi	3.58	5.11	6.64	V/lx•s
	Blue	R_B	300 dpi	6.89	9.84	12.79	V/lx•s
			1200 dpi	2.30	3.28	4.26	V/lx•s
Offset level **Note 1**		V_{OS}		4.5	6.0	7.5	V
Image lag		IL	V_{OUT} = 1.0 V	–	3.0	7.0	%
Output fall delay time **Note 2**		t_d	V_{OUT} = 1.0 V	–	25	–	ns
Total transfer efficiency		TTE	V_{OUT} = 1.0 V, data rate = 5 MHz	92	98	–	%
Register imbalance		RI	V_{OUT} = 1.0 V (1200 dpi)	–	1.0	4.0	%
Response peak	Red			–	630	–	nm
	Green			–	540	–	nm
	Blue			–	460	–	nm
Dynamic range		DR1	V_{sat}/DSNU 300 dpi	–	675	–	times
			V_{sat}/DSNU 1200 dpi	–	1200	–	times
		DR2	V_{sat}/σCDS 300 dpi	–	2700	–	times
			V_{sat}/σCDS 1200 dpi	–	2400	–	times
Reset feed-through noise **Note 1**		RFTN	Light shielding	–2000	–500	+1000	mV
Random noise (CDS)		σCDS	Light shielding	–	1.0	–	mV

Notes 1. Refer to **TIMING CHART 2–1 to 2–8**.

2. When the fall time of ϕ1L or ϕ2L (t1', t2') is the Typ. value (refer to **TIMING CHART 2–1 to 2–8**).

INPUT PIN CAPACITANCE (T_A = +25°C, V_{OD} = 12 V)

Parameter	Symbol	Pin name	Pin No.	Min.	Typ.	Max.	Unit
Shift register clock pin capacitance 1	$C_{\phi 1\text{-}300}$	φ1-300	13	–	250	–	pF
			15	–	250	–	pF
	$C_{\phi 1\text{-}1200}$	φ1-1200	8	–	850	–	pF
Shift register clock pin capacitance 2	$C_{\phi 2\text{-}300}$	φ2-300	14	–	300	–	pF
			16	–	300	–	pF
	$C_{\phi 2\text{-}1200}$	φ2-1200	7	–	850	–	pF
Last stage sift reset gate clock pin capacitance 1	$C_{\phi 1L}$	φ1L	17	–	15	–	pF
Last stage sift reset gate clock pin capacitance 2	$C_{\phi 2L}$	φ2L	3	–	15	–	pF
Reset gate clock pin capacitance	$C_{\phi RB}$	φRB	4	–	15	–	pF
Reset feed-through level clamp clock pin capacitance	$C_{\phi CLB}$	φCLB	5	–	15	–	pF
300/1200 dpi select signal pin capacitance	$C_{\phi SEL}$	φSEL	19	–	15	–	pF
Transfer gate clock pin capacitance	$C_{\phi TG}$	φTG1	12	–	200	–	pF
		φTG2	10	–	200	–	pF
		φTG3	9	–	200	–	pF

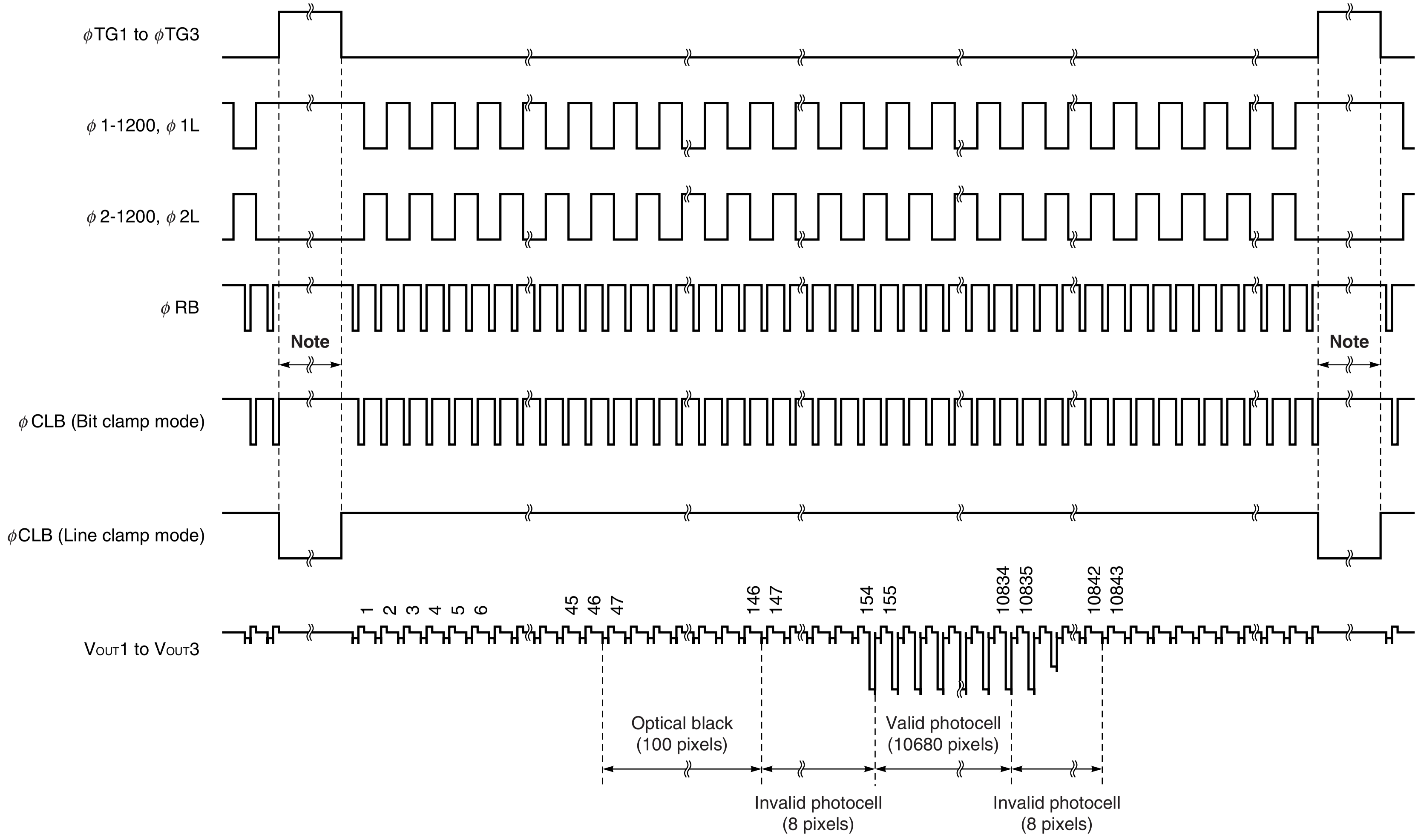
300/600/1200 MODE

Mode	Description	φSEL	300 dpi data	φ1-300, φ2-300	1200 dpi data	φ1-1200, φ2-1200
1	300 dpi only	High	Use	Clocked	Flush $^{\text{Note 2}}$	Clocked
2	600 dpi only $^{\text{Note 1}}$	Low	Flush $^{\text{Note 2}}$	Clocked	Use 1 line	Clocked
3	1200 dpi only	Low	Flush $^{\text{Note 2}}$	Clocked	Use	Clocked

Notes 1. For 600 dpi mode, the reset pulse is extended to allow second line’s charge to dump immediately to DC level.

2. Flush means that data is continuously sunk via reset gate.

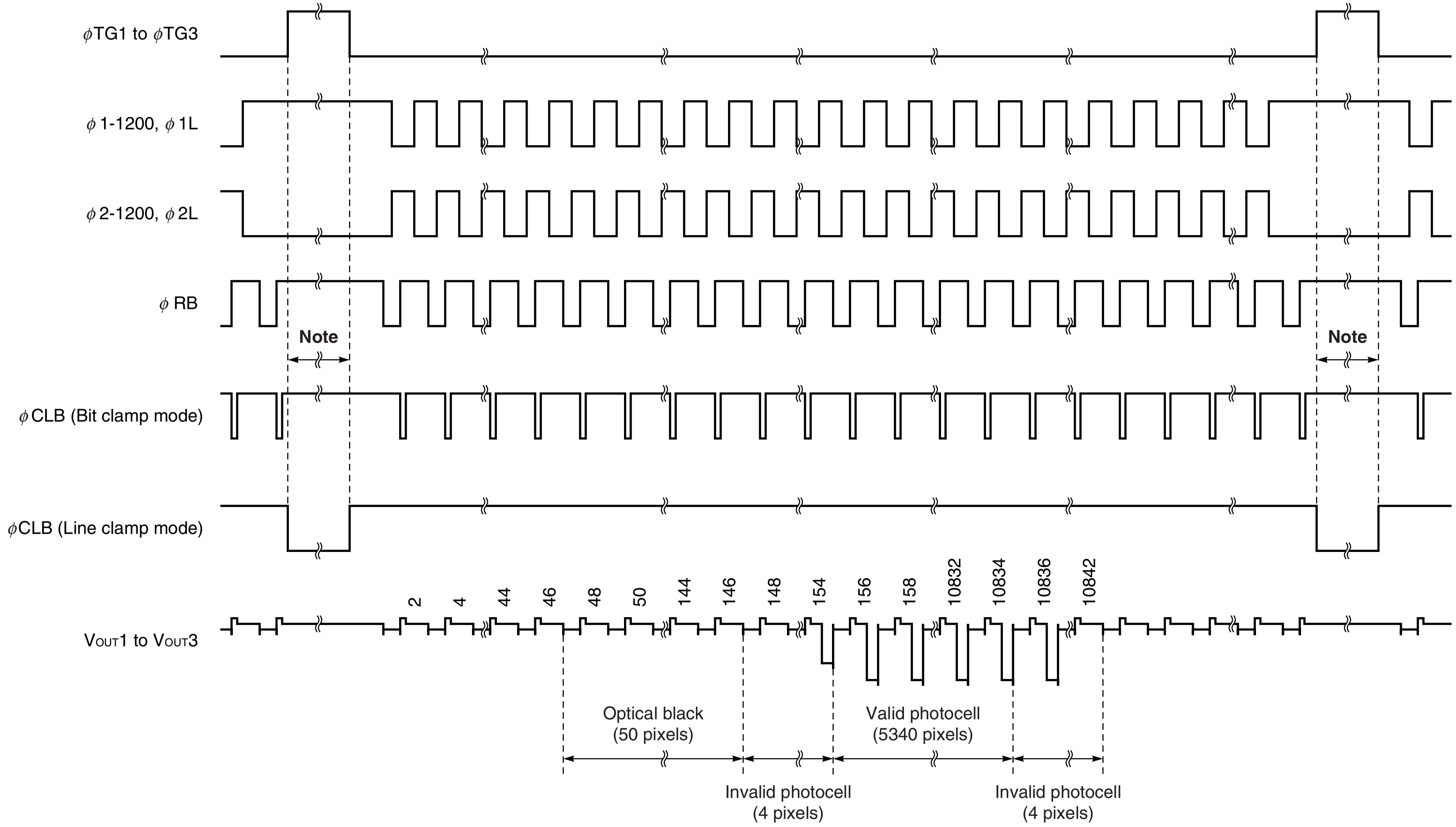
TIMING CHART 1–1 (1200 dpi, for each color)



Note Set the φRB pulse and φCLB pulse (bit clamp mode) to high level during the φTG1 to φTG3 pulse. And set the φRB pulse to high level while the φCLB pulse is low level at line clamp mode.

Remark Inverse pulse of the φTG1 to φTG3 can be used as φCLB at line clamp mode.

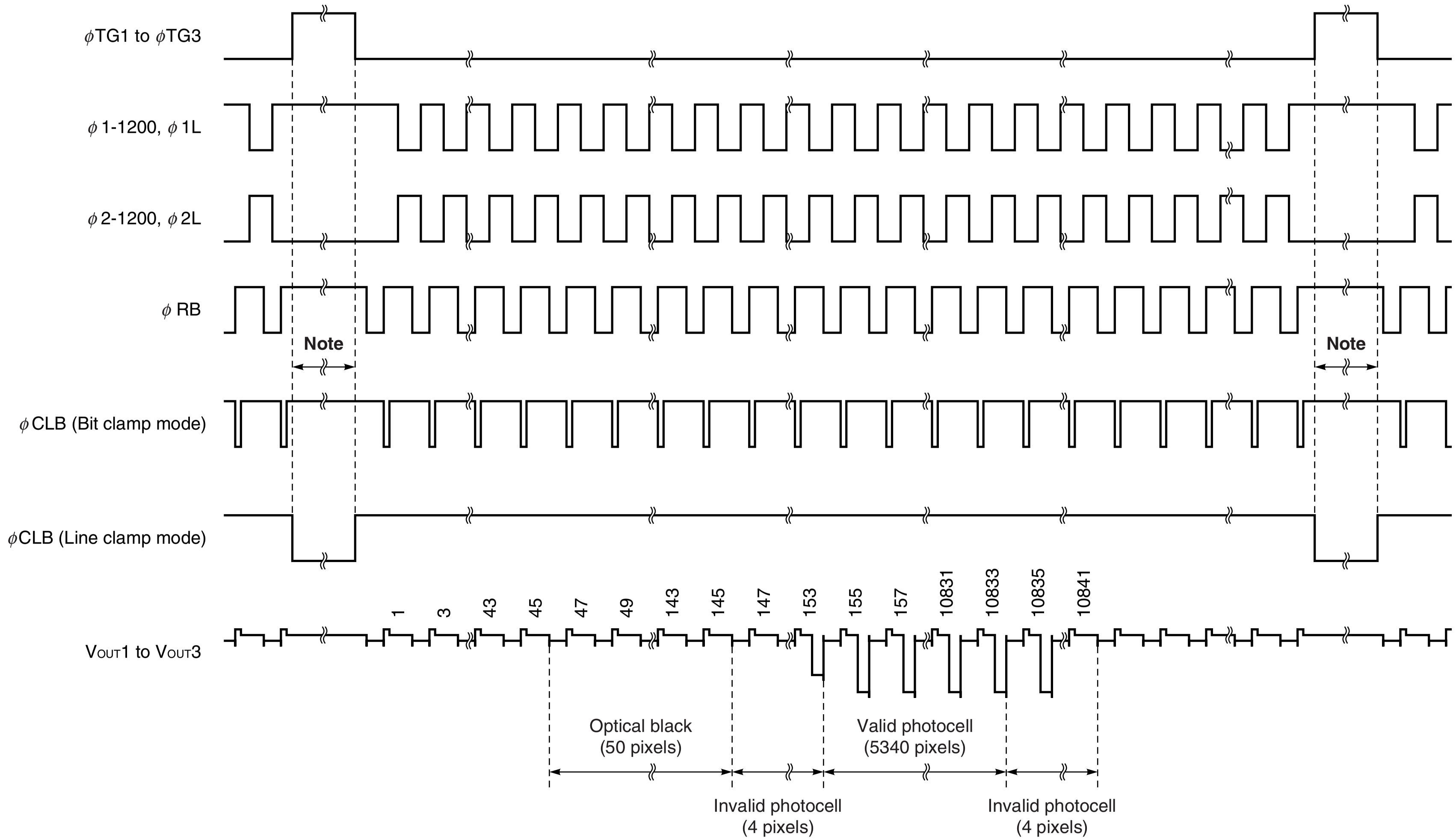
TIMING CHART 1–2 (600 dpi, even pixel, for each color)



Note Set the φRB pulse and φCLB pulse (bit clamp mode) to high level during the φTG1 to φTG3 pulse. And set the φRB pulse to high level while the φCLB pulse is low level at line clamp mode.

Remark Inverse pulse of the φTG1 to φTG3 can be used as φCLB at line clamp mode.

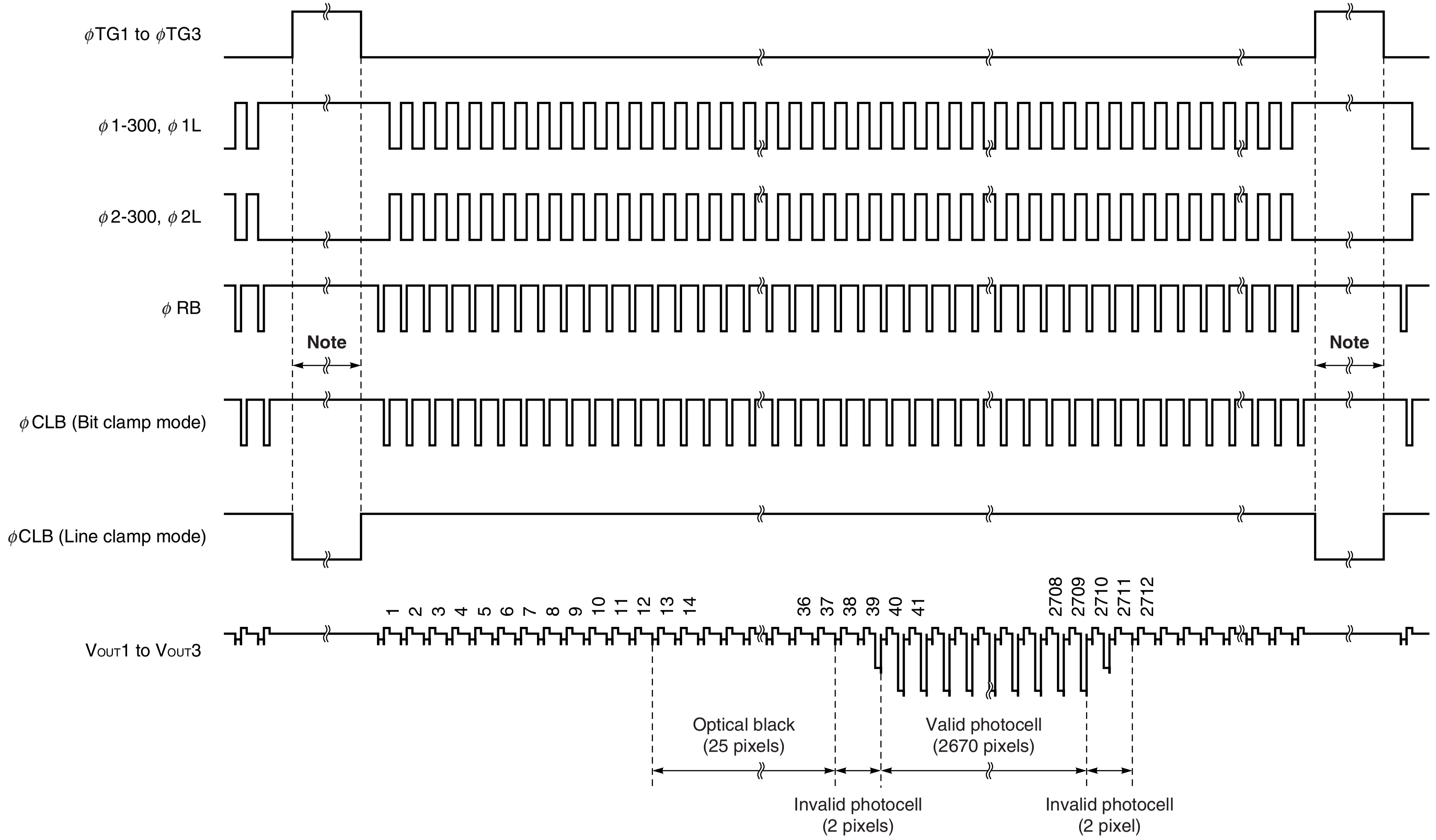
TIMING CHART 1–3 (600 dpi, odd pixel, for each color)



Note Set the φRB pulse and φCLB pulse (bit clamp mode) to high level during the φTG1 to φTG3 pulse. And set the φRB pulse to high level while the φCLB pulse is low level at line clamp mode.

Remark Inverse pulse of the φTG1 to φTG3 can be used as φCLB at line clamp mode.

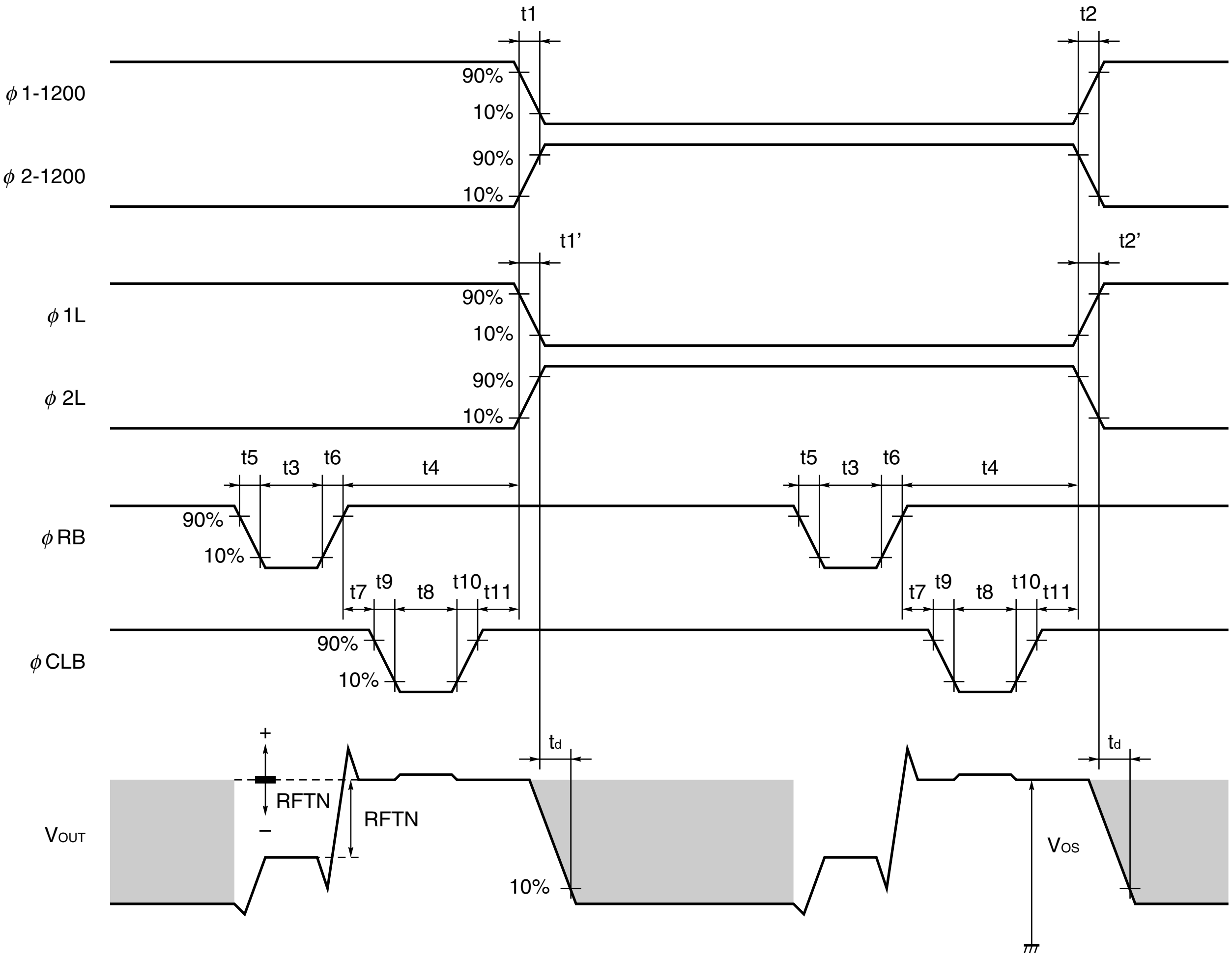
TIMING CHART 1–4 (300 dpi, for each color)



Note Set the φRB pulse and φCLB pulse (bit clamp mode) to high level during the φTG1 to φTG3 pulse. And set the φRB pulse to high level while the φCLB pulse is low level at line clamp mode.

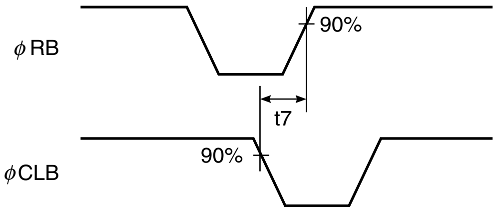
Remark Inverse pulse of the φTG1 to φTG3 can be used as φCLB at line clamp mode.

TIMING CHART 2–1 (1200 dpi, bit clamp mode, for each color)

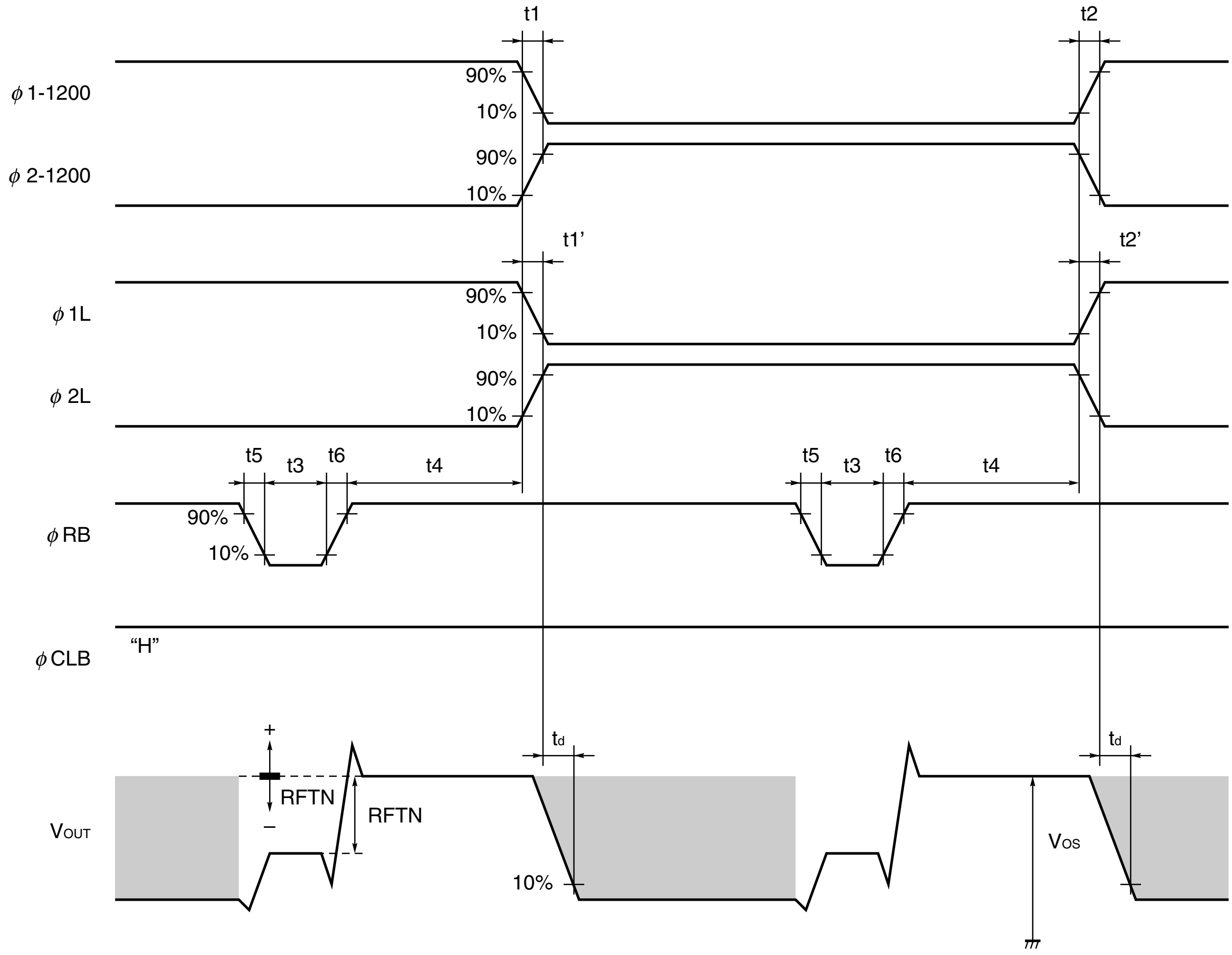


Symbol	Min.	Typ.	Max.	Unit
t1, t2	0	25	–	ns
t1', t2'	0	5	–	ns
t3	20	50	–	ns
t4	50	150	–	ns
t5, t6	0	5	–	ns
t7	–5 Note	+25	–	ns
t8	20	50	–	ns
t9, t10	0	5	–	ns
t11	5	25	–	ns

Note Min. of t7 shows that the φRB and φCLB overlap each other.

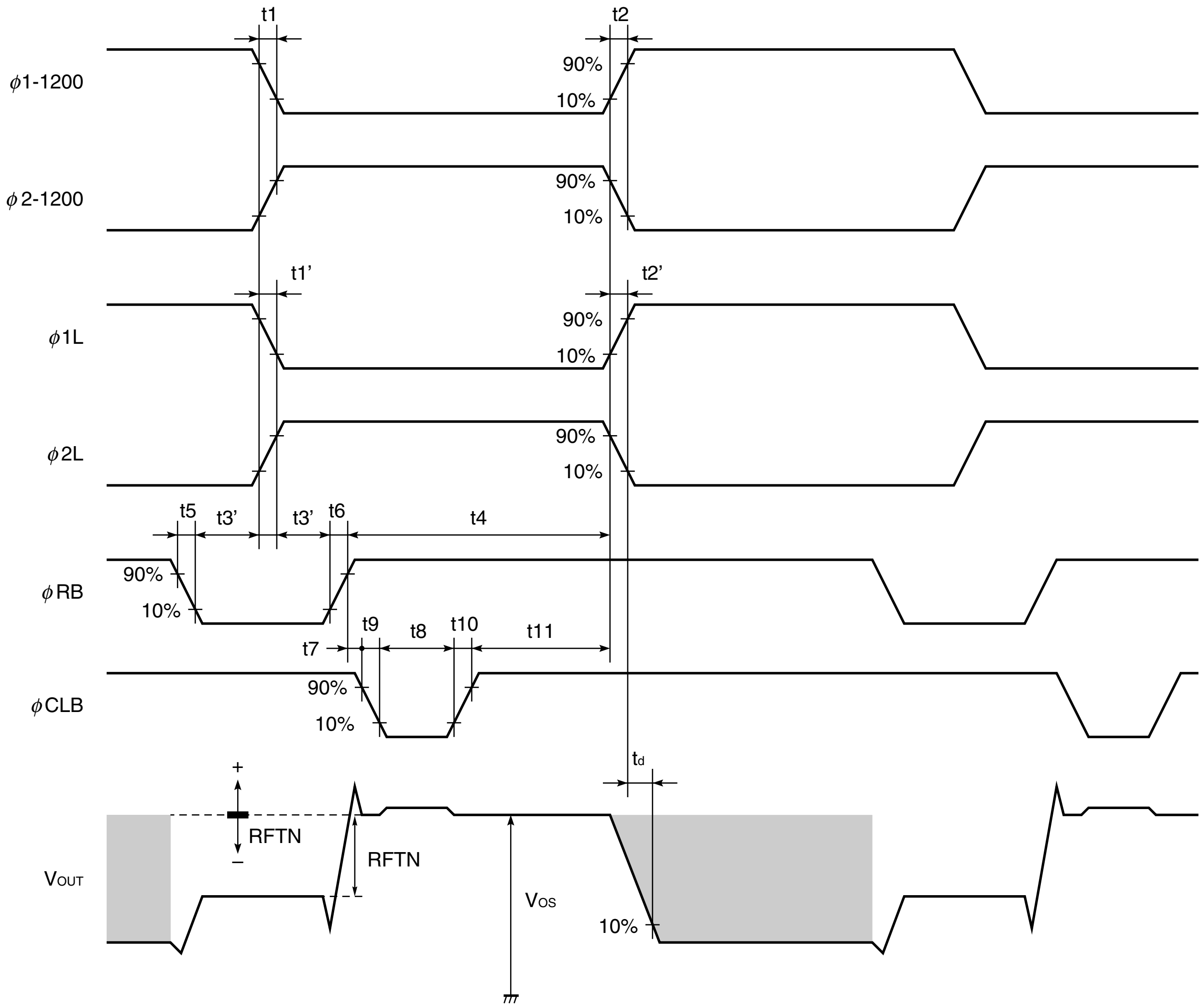


TIMING CHART 2–2 (1200 dpi, line clamp mode, for each color)



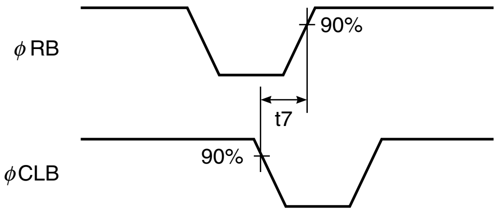
Symbol	Min.	Typ.	Max.	Unit
t1, t2	0	25	–	ns
t1’, t2’	0	5	–	ns
t3	20	50	–	ns
t4	50	150	–	ns
t5, t6	0	5	–	ns

TIMING CHART 2–3 (600 dpi, even pixel, bit clamp mode, for each color)

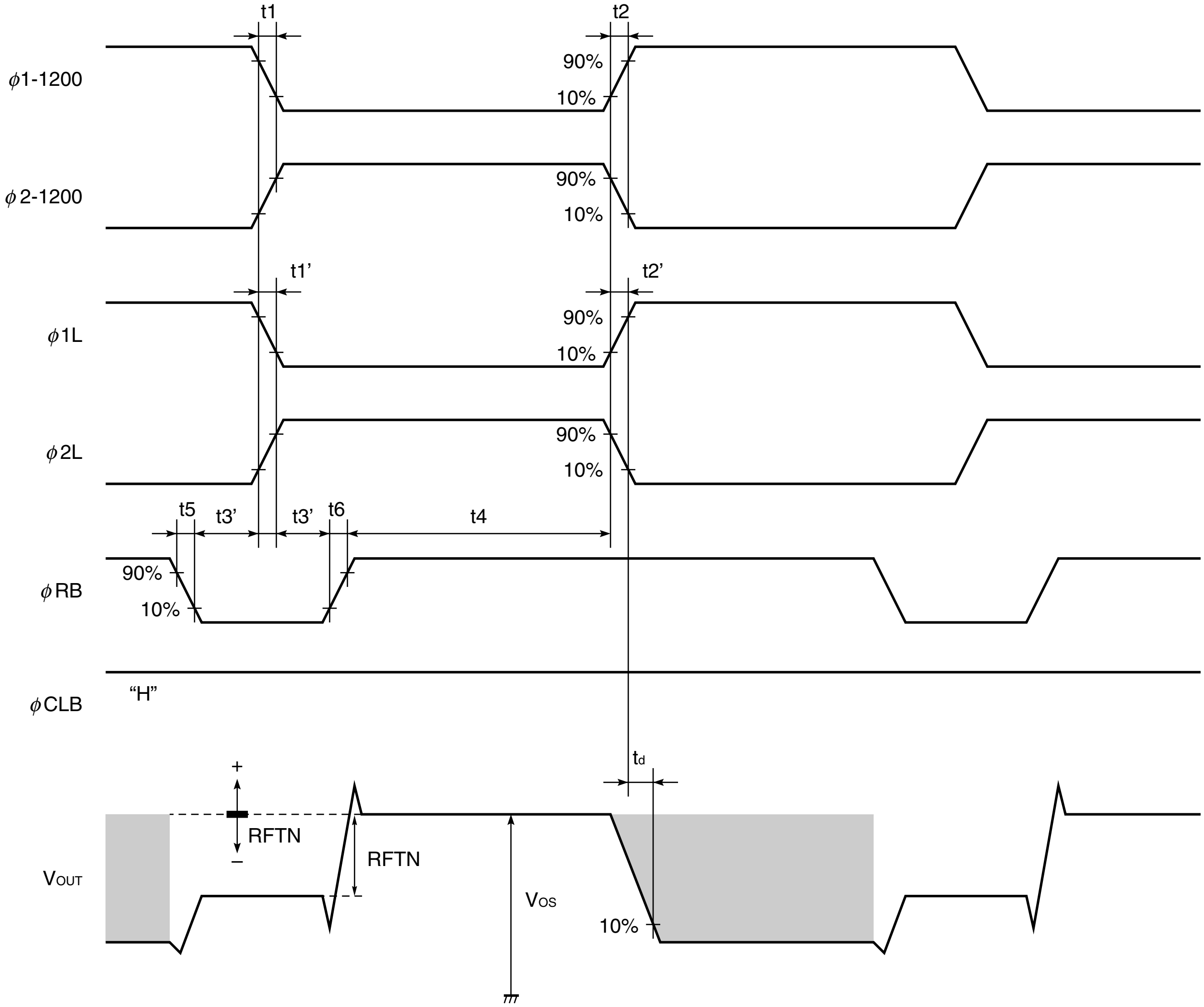


Symbol	Min.	Typ.	Max.	Unit
t1, t2	0	25	–	ns
t1', t2'	0	5	–	ns
t3'	50	100	–	ns
t4	50	370	–	ns
t5, t6	0	5	–	ns
t7	–5 **Note**	+25	–	ns
t8	100	200	–	ns
t9, t10	0	5	–	ns
t11	5	100	–	ns

Note Min. of t7 shows that the φRB and φCLB overlap each other.

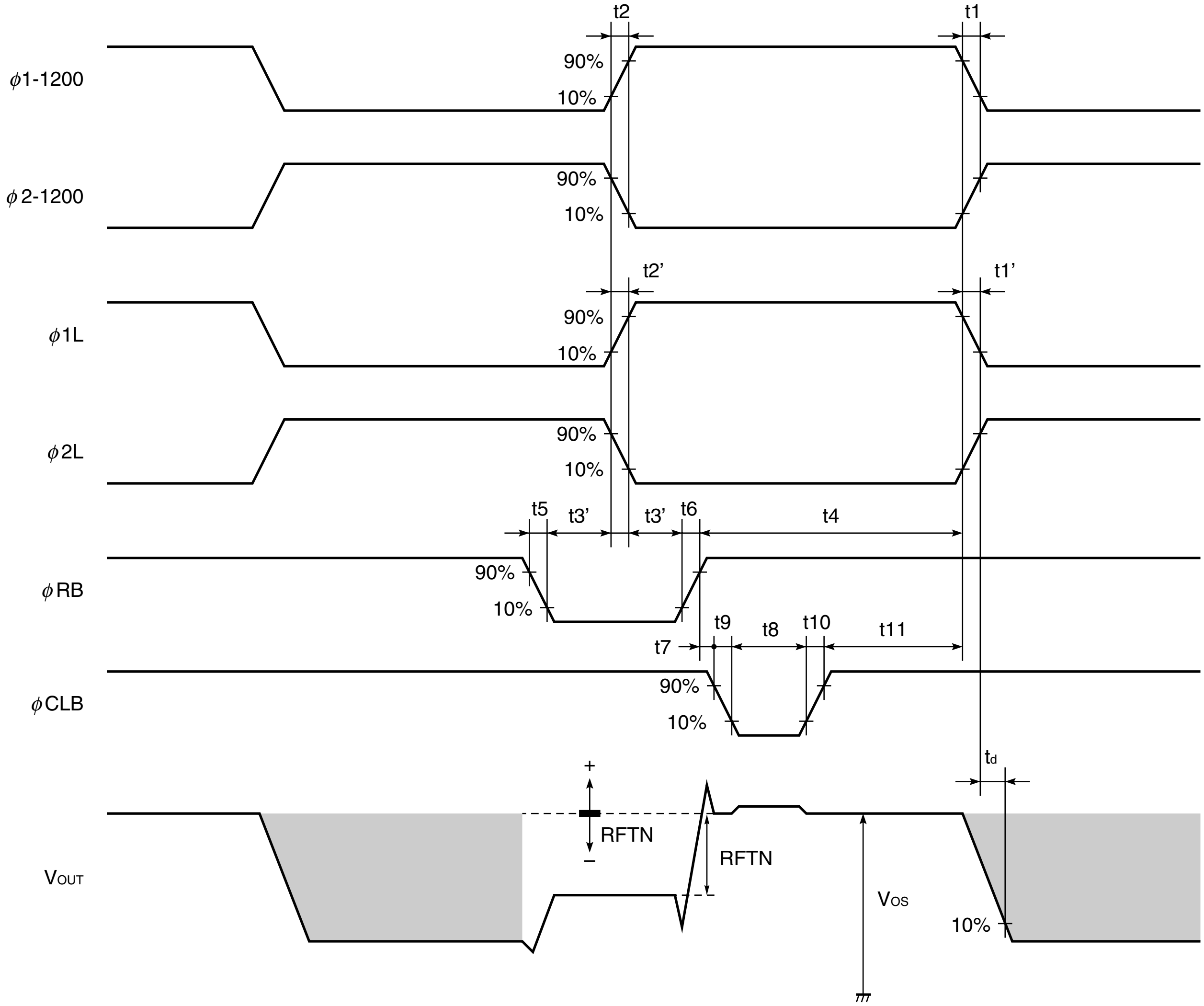


TIMING CHART 2–4 (600 dpi, even pixel, line clamp mode, for each color)



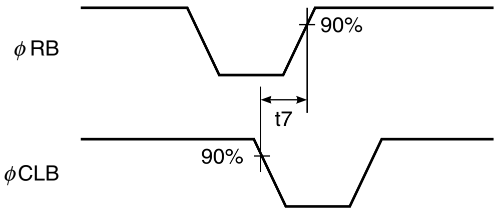
Symbol	Min.	Typ.	Max.	Unit
t1, t2	0	25	–	ns
t1’, t2’	0	5	–	ns
t3’	50	100	–	ns
t4	50	370	–	ns
t5, t6	0	5	–	ns

TIMING CHART 2–5 (600 dpi, odd pixel, bit clamp mode, for each color)

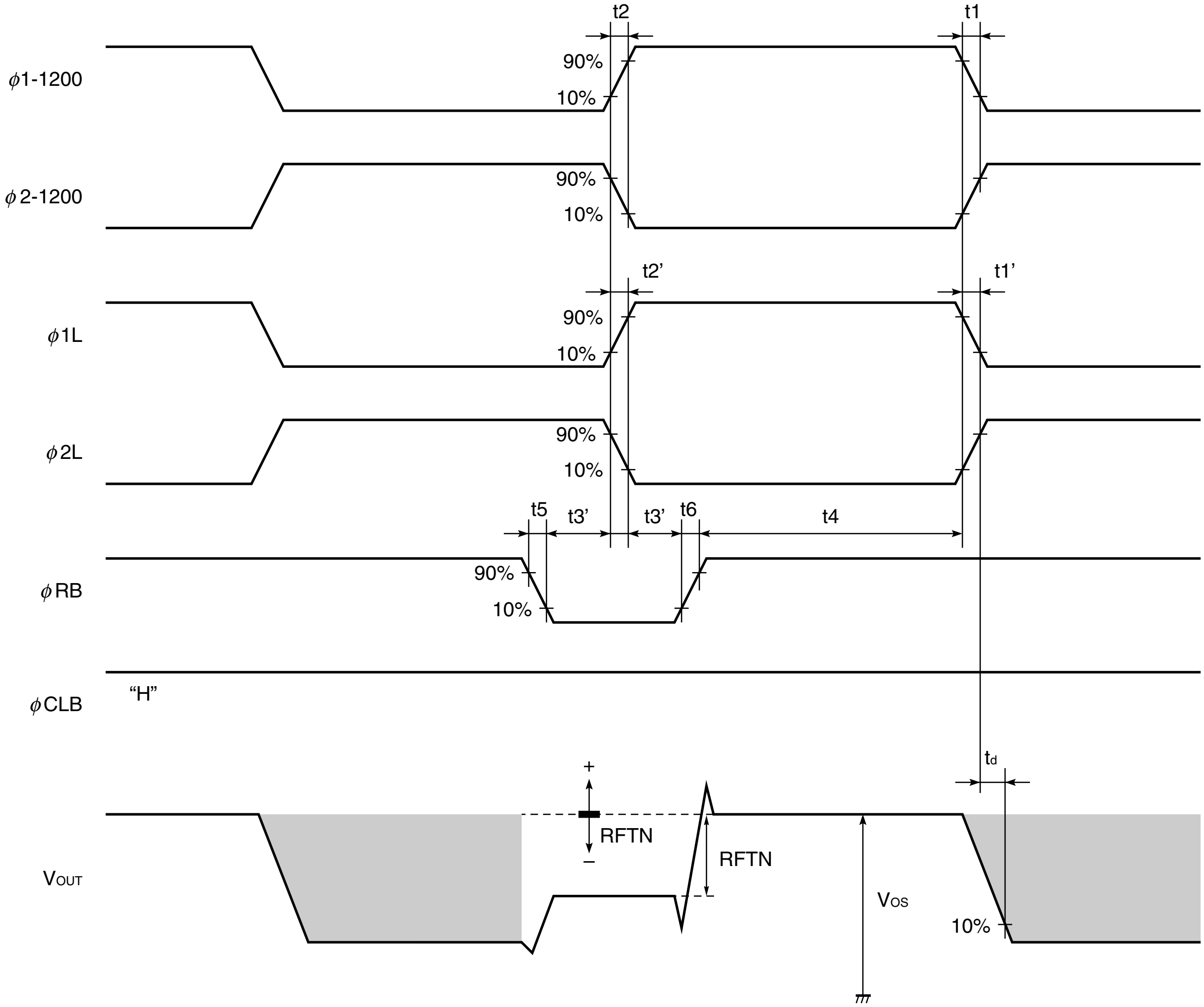


Symbol	Min.	Typ.	Max.	Unit
t1, t2	0	25	–	ns
t1', t2'	0	5	–	ns
t3'	50	100	–	ns
t4	50	370	–	ns
t5, t6	0	5	–	ns
t7	–5 **Note**	+25	–	ns
t8	100	200	–	ns
t9, t10	0	5	–	ns
t11	5	100	–	ns

Note Min. of t7 shows that the φRB and φCLB overlap each other.

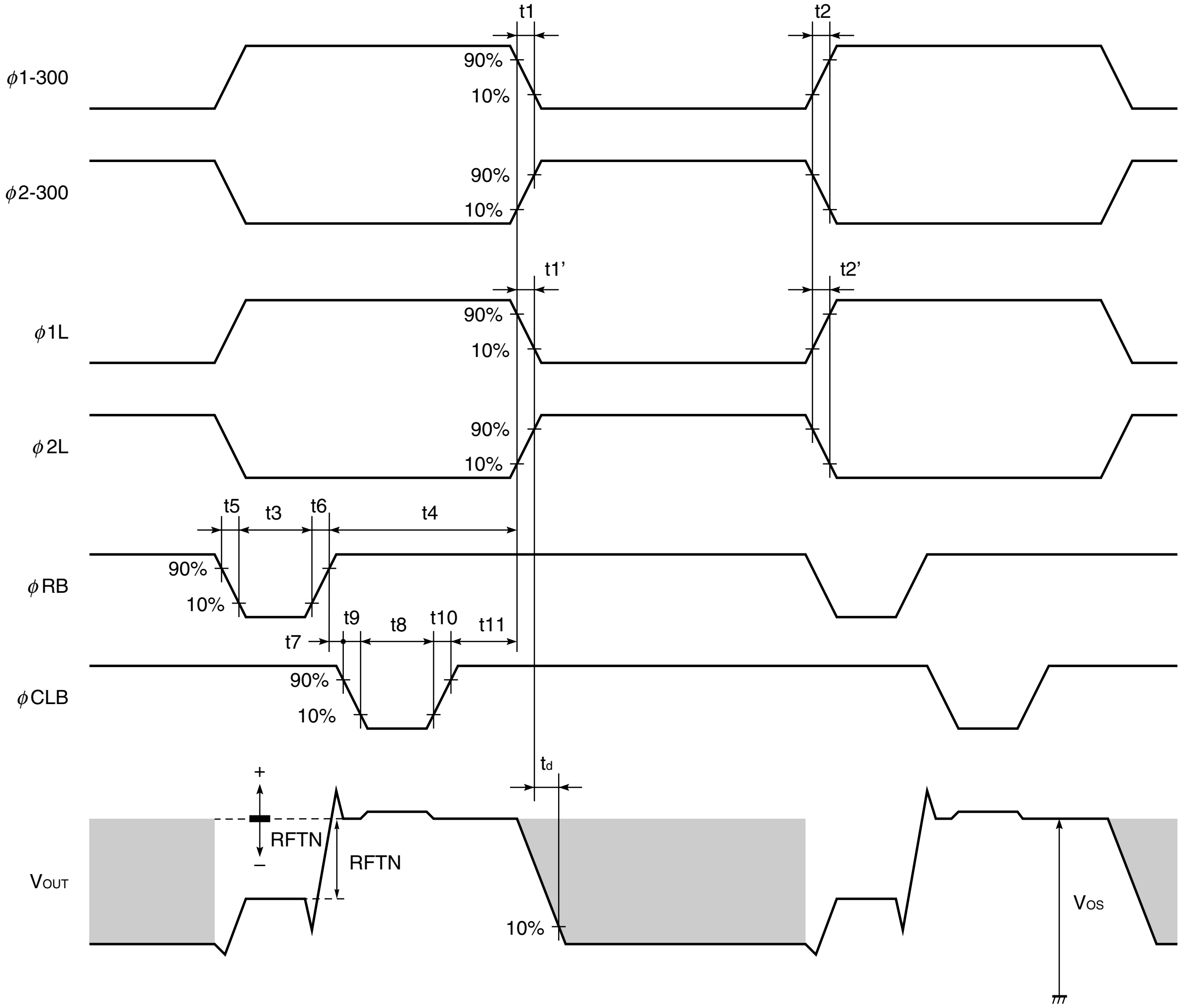


TIMING CHART 2–6 (600 dpi, odd pixel, line clamp mode, for each color)



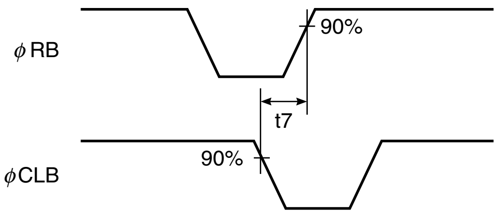
Symbol	Min.	Typ.	Max.	Unit
t1, t2	0	25	–	ns
t1', t2'	0	5	–	ns
t3'	50	100	–	ns
t4	50	370	–	ns
t5, t6	0	5	–	ns

TIMING CHART 2–7 (300 dpi, bit clamp mode, for each color)

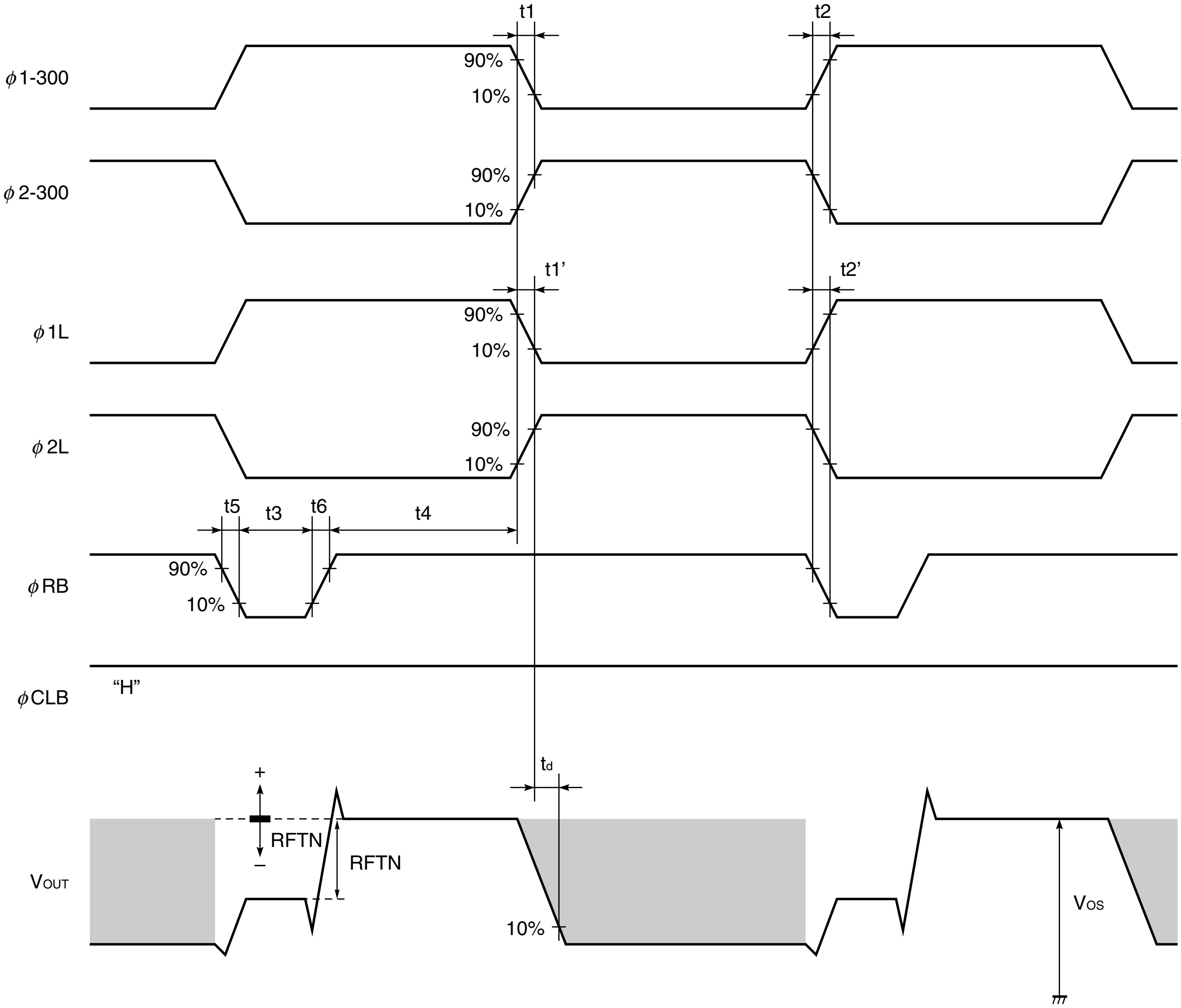


Symbol	Min.	Typ.	Max.	Unit
t1, t2	0	25	–	ns
t1', t2'	0	5	–	ns
t3	20	50	–	ns
t4	50	150	–	ns
t5, t6	0	5	–	ns
t7	–5 **Note**	+25	–	ns
t8	20	50	–	ns
t9, t10	0	5	–	ns
t11	5	25	–	ns

Note Min. of t7 shows that the φRB and φCLB overlap each other.

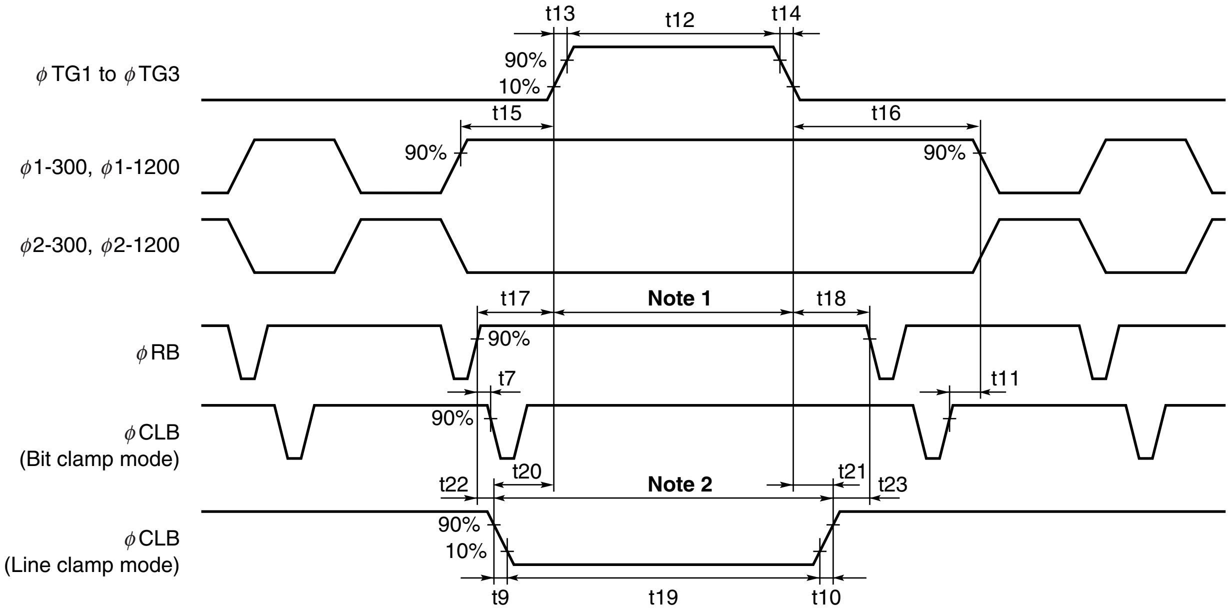


TIMING CHART 2–8 (300 dpi, line clamp mode, for each color)



Symbol	Min.	Typ.	Max.	Unit
t1, t2	0	25	–	ns
t1', t2'	0	5	–	ns
t3	20	50	–	ns
t4	50	150	–	ns
t5, t6	0	5	–	ns

φTG1 to φTG3, φ1, φ2 TIMING CHART

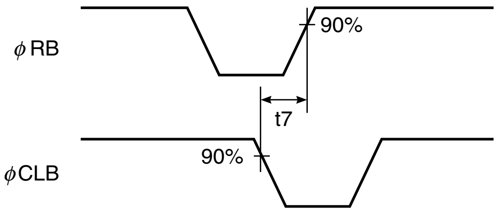


Symbol	Min.	Typ.	Max.	Unit
t7	–5 Note 3	+25	–	ns
t9, t10	0	5	–	ns
t11	5	25	–	ns
t12	5000	10000	50000	ns
t13, t14	0	50	–	ns
t15, t16	900	1000	–	ns
t17, t18	200	400	–	ns
t19	t12	t12	50000	ns
t20, t21	0	50	–	ns
t22, t23	0	350	–	ns

Notes 1. Set the φRB pulse and φCLB pulse (bit clamp mode) to high level during this period.

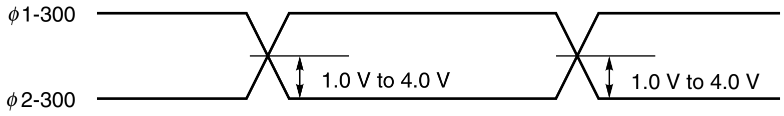
2. Set the φRB pulse to high level during this period.

3. Min. of t7 shows that the φRB and φCLB overlap each other.

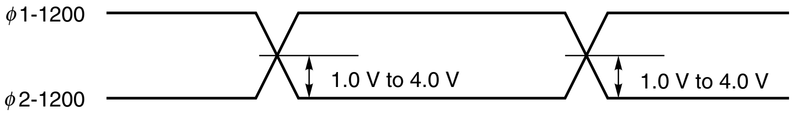


Remark Inverse pulse of the φTG1 to φTG3 can be used as φCLB.

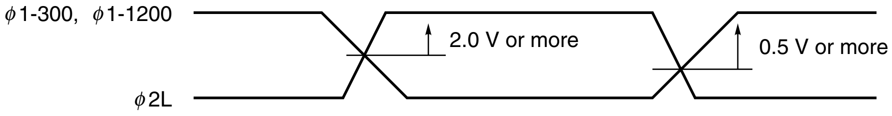
φ1-300, φ2-300 cross points



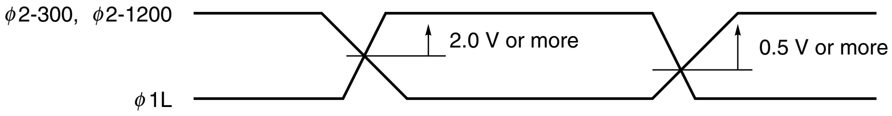
φ1-1200, φ2-1200 cross points



φ1-300, φ1-1200, φ2L cross points



φ2-300, φ1-1200, φ1L cross points



Remark Adjust cross points (φ1-300, φ2-300), (φ1-1200, φ2-1200), (φ1-300, φ1-1200, φ2L) and (φ2-300, φ1-1200, φ1L) with input resistance of each pin.

DEFINITIONS OF CHARACTERISTIC ITEMS

1. Saturation voltage : **V_{sat}**

   Output signal voltage at which the response linearity is lost.

2. Saturation exposure : **SE**

   Product of intensity of illumination (lx) and storage time (s) when saturation of output voltage occurs.

3. Photo response non-uniformity : **PRNU**

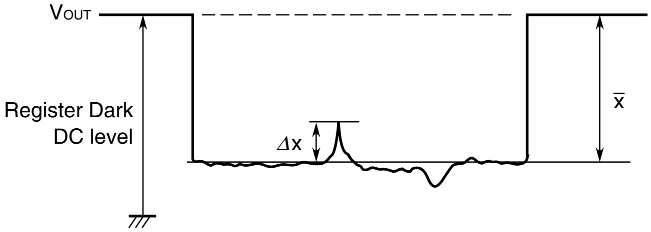
   The output signal non-uniformity of all the valid pixels when the photosensitive surface is applied with the light of uniform illumination. This is calculated by the following formula.

$$\text{PRNU (\%)} = \frac{\Delta x}{\overline{x}} \times 100$$

Δx : maximum of $|x_j - \overline{x}|$

$$\overline{x} = \frac{\sum_{j=1}^{\text{Valid pixels}} x_j}{\text{Valid pixels}}$$

x_j : Output voltage of valid pixel number j



4. Average dark signal : **ADS**

   Average output signal voltage of all the valid pixels at light shielding. This is calculated by the following formula.

$$\text{ADS (mV)} = \frac{\sum_{j=1}^{\text{Valid pixels}} d_j}{\text{Valid pixels}}$$

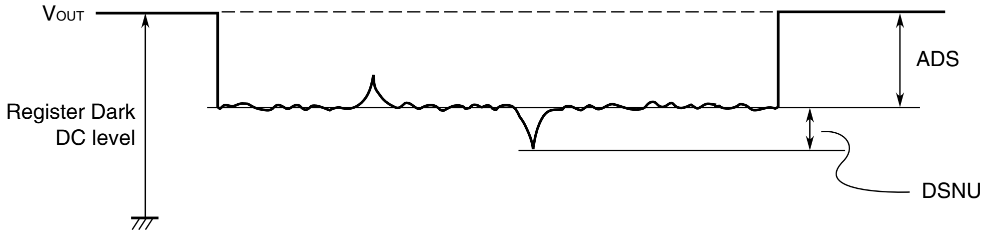
d_j : Dark signal of valid pixel number j

5. Dark signal non-uniformity : **DSNU**

   Absolute maximum of the difference between ADS and voltage of the highest or lowest output pixel of all the valid pixels at light shielding. This is calculated by the following formula.

$$\text{DSNU (mV) : maximum of } \left| d_j - \text{ADS} \right|_{j = 1 \text{ to valid pixels}}$$

d_j : Dark signal of valid pixel number j



6. Output impedance : **Zo**

   Impedance of the output pins viewed from outside.

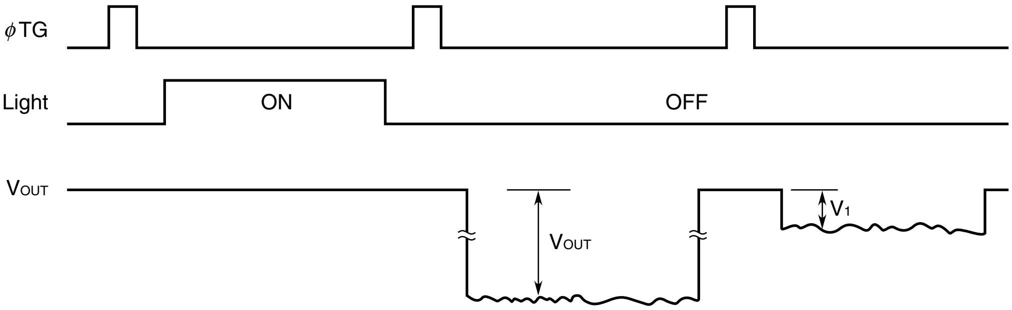
7. Response : **R**

   Output voltage divided by exposure (lx•s).

   Note that the response varies with a light source (spectral characteristic).

8. Image lag : **IL**

   The rate between the last output voltage and the next one after read out the data of a line.



$$\text{IL (\%)} = \frac{V_1}{V_{OUT}} \times 100$$

9. Register Imbalance : **RI** (1200 dpi)

The rate of the difference between the averages of the output voltage of Odd and Even bits, against the average output voltage of all the valid pixels.

$$\mathrm{RI}\ (\%) = \frac{\frac{2}{n}\left|\sum_{j=1}^{\frac{n}{2}} (V_{2j-1} - V_{2j})\right|}{\frac{1}{n}\sum_{j=1}^{n} V_j} \times 100$$

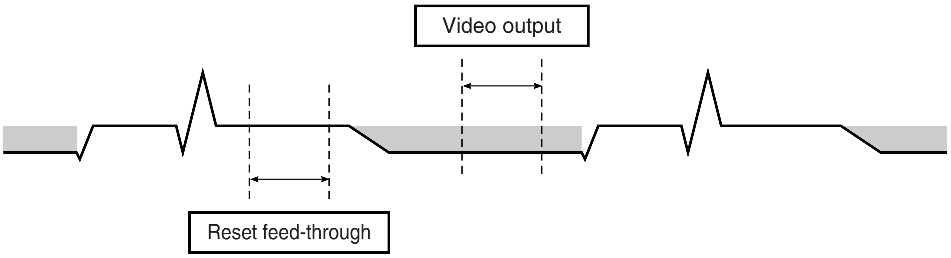
n : Number of valid pixels
V_j : Output voltage of each pixel

10. Random noise (CDS) : **σCDS**

Random noise σCDS is defined as the standard deviation of a valid pixel output signal with 100 times (=100 lines) data sampling at dark (light shielding). σCDS is calculated by the following procedure.

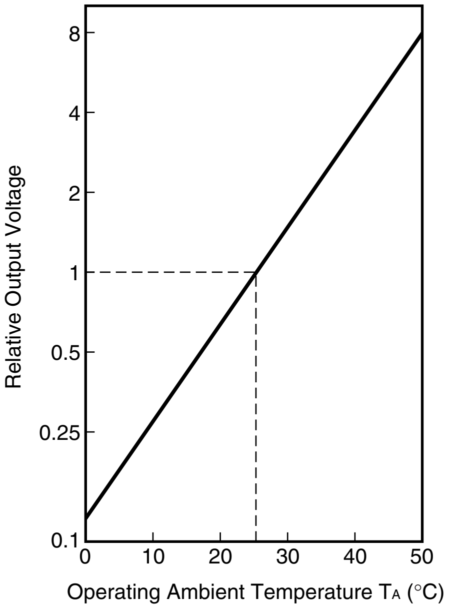
1. One valid photocell in one reading is fixed as measurement point.
2. The output level is measured during the reset feed-through period which is averaged over 100 ns to get "VD_i".
3. The output level is measured during the Video Output time averaged over 100 ns to get "VO_i".
4. The correlated double sampling output is defined by $VCDS_i = VD_i - VO_i$
5. Repeat the above procedure (1 to 4) for 100 times (= 100 lines).
6. Calculate the standard deviation σCDS using the following formula equation.

$$\sigma\mathrm{CDS\ (mV)} = \sqrt{\frac{\sum_{i=1}^{100} (VCDS_i - \overline{V})^2}{100}} \quad , \quad \overline{V} = \frac{1}{100}\sum_{i=1}^{100} VCDS_i$$

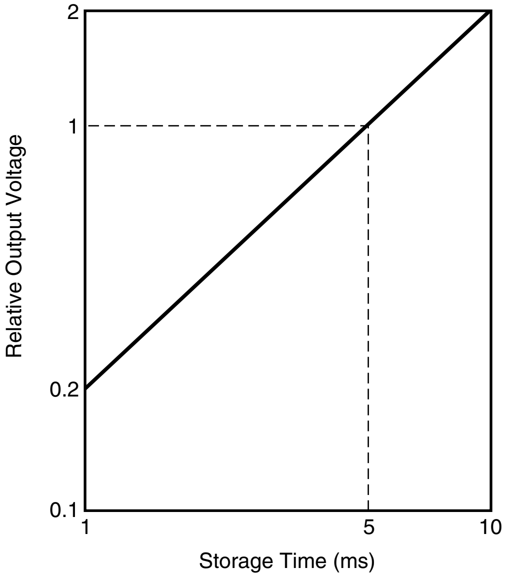


STANDARD CHARACTERISTIC CURVES (Reference Value)

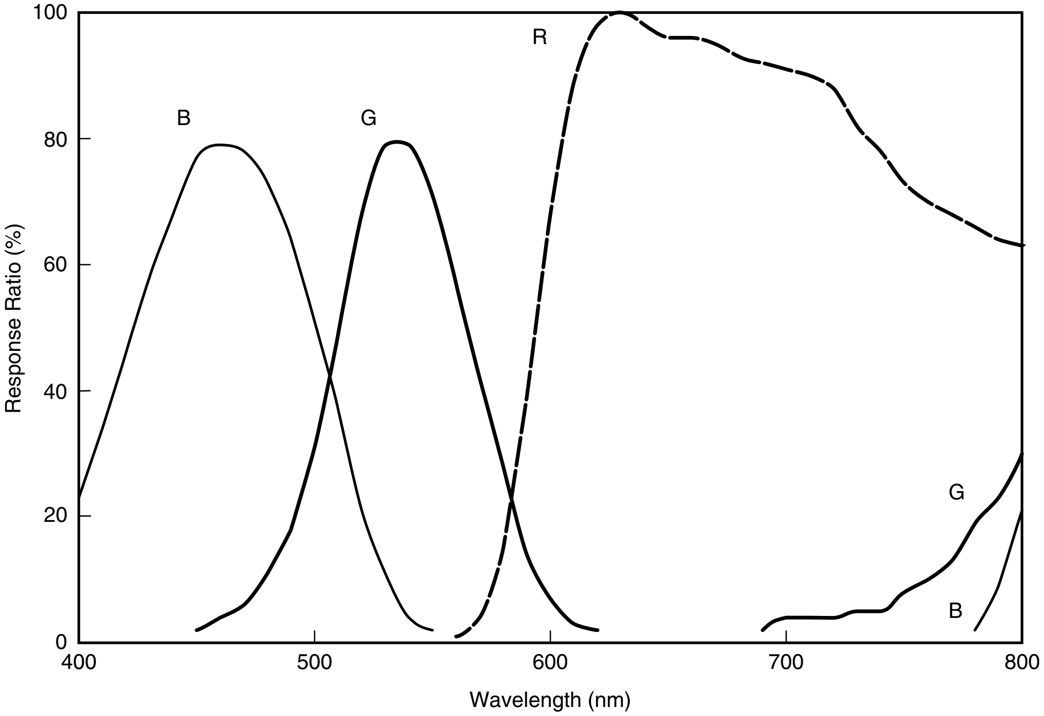
DARK OUTPUT TEMPERATURE CHARACTERISTIC



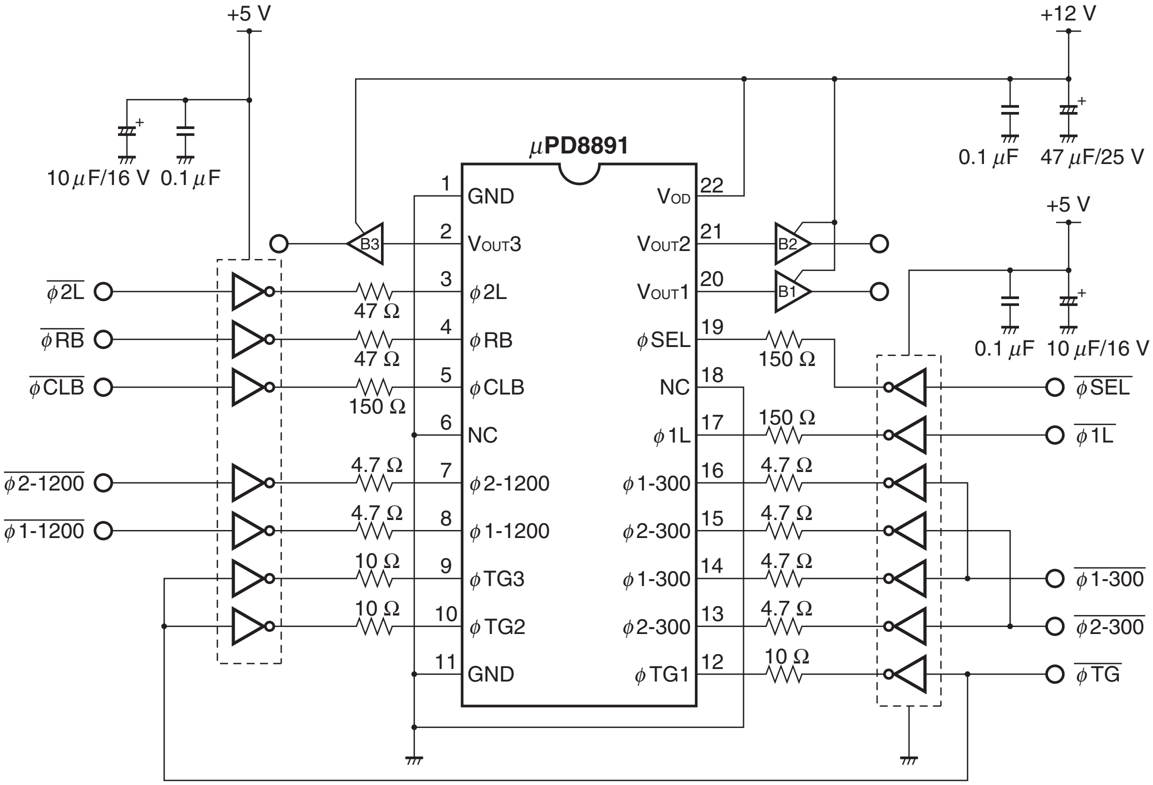
STORAGE TIME OUTPUT VOLTAGE CHARACTERISTIC (TA = +25°C)



TOTAL SPECTRAL RESPONSE CHARACTERISTICS (without infrared cut filter and heat absorbing filter) (TA = +25°C)



APPLICATION CIRCUIT EXAMPLE

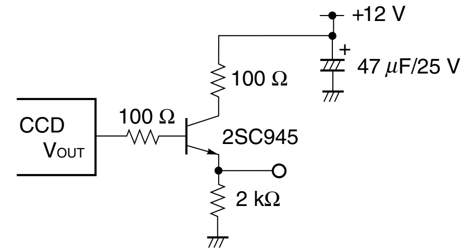


Caution Connect the No connection pins (NC) to GND.

Remarks 1. The inverters shown in the above application circuit example are the 74HC04 (data rate < 2 MHz) or the 74AC04 (2 ≤ data rate < 5 MHz).

2. B1 to B3 in the application circuit example are shown in the figure blow.

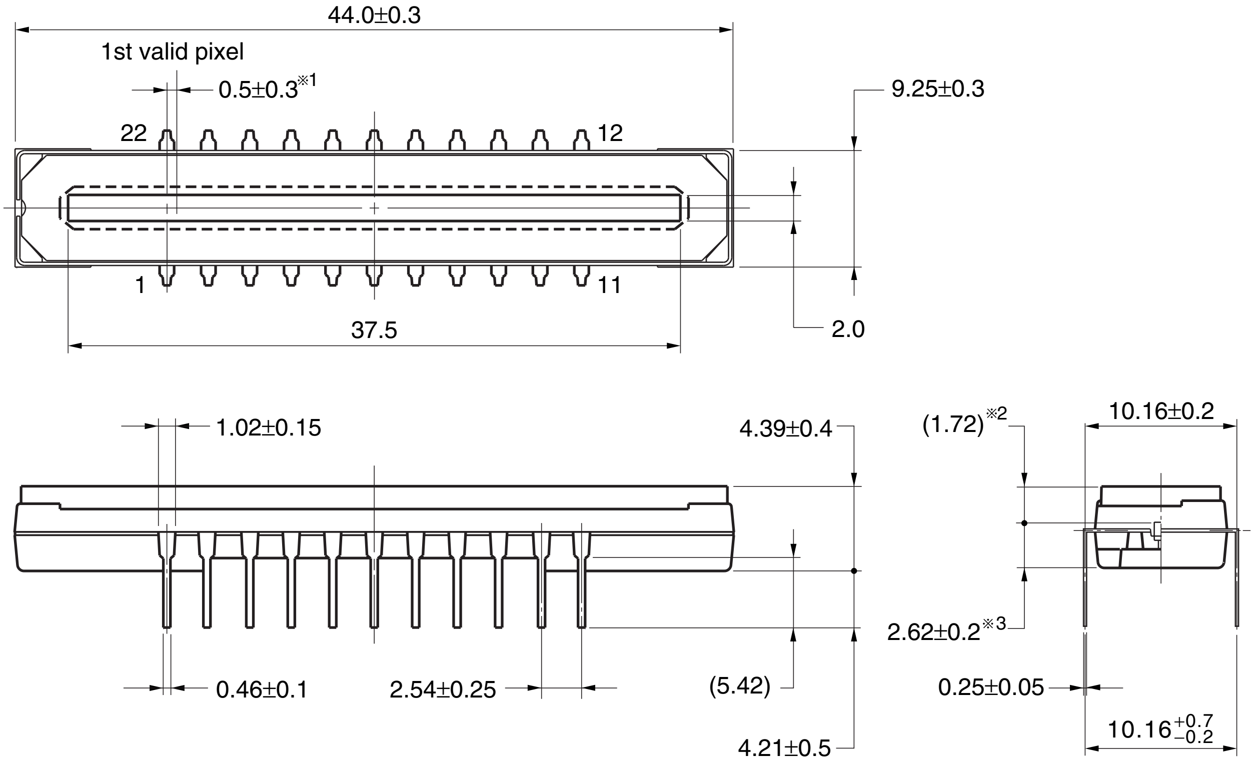
B1 to B3 EQUIVALENT CIRCUIT



PACKAGE DRAWING

μPD8891CY
CCD LINEAR IMAGE SENSOR 22-PIN PLASTIC DIP (10.16 mm (400))

(Unit : mm)



Name	Dimensions	Refractive index
Plastic cap	42.9×8.35×0.7	1.5

※1 1st valid pixel ←→ The center of the pin1
※2 The surface of the CCD chip ←→ The top of the cap
※3 The bottom of the package ←→ The surface of the CCD chip

22C-1CCD-PKG11-1

RECOMMENDED SOLDERING CONDITIONS

When soldering this product, it is highly recommended to observe the conditions as shown below.

If other soldering processes are used, or if the soldering is performed under different conditions, please make sure to consult with our sales offices.

Type of Through-hole Device

μPD8891CY-A : CCD linear image sensor 22-pin plastic DIP (10.16 mm (400))

Process	Conditions
Partial heating method	Pin temperature : 300°C or below, Heat time : 3 seconds or less (per pin)

Cautions 1. During assembly care should be taken to prevent solder or flux from contacting the plastic cap. The optical characteristics could be degraded by such contact.

2. Soldering by the solder flow method may have deleterious effects on prevention of plastic cap soiling and heat resistance. So the method cannot be guaranteed.

NOTES ON HANDLING THE PACKAGES

① DUST AND DIRT PROTECTING

The optical characteristics of the CCD will be degraded if the cap is scratched during cleaning. Don’t either touch plastic cap surface by hand or have any object come in contact with plastic cap surface. Should dirt stick to a plastic cap surface, blow it off with an air blower. For dirt stuck through electricity ionized air is recommended. And if the plastic cap surface is grease stained, clean with our recommended solvents.

○ CLEANING THE PLASTIC CAP

Care should be taken when cleaning the surface to prevent scratches.

We recommend cleaning the cap with a soft cloth moistened with one of the recommended solvents below. Excessive pressure should not be applied to the cap during cleaning. If the cap requires multiple cleanings it is recommended that a clean surface or cloth be used.

○ RECOMMENDED SOLVENTS

The following are the recommended solvents for cleaning the CCD plastic cap.

Use of solvents other than these could result in optical or physical degradation in the plastic cap. Please consult your sales office when considering an alternative solvent.

Solvents	Symbol
Ethyl Alcohol	EtOH
Methyl Alcohol	MeOH
Isopropyl Alcohol	IPA
N-methyl Pyrrolidone	NMP

② MOUNTING OF THE PACKAGE

The application of an excessive load to the package may cause the package to warp or break, or cause chips to come off internally. Particular care should be taken when mounting the package on the circuit board. Don't have any object come in contact with plastic cap. You should not reform the lead frame. We recommended to use a IC-inserter when you assemble to PCB.

Also, be care that the any of the following can cause the package to crack or dust to be generated.

1. Applying heat to the external leads for an extended period of time with soldering iron.
2. Applying repetitive bending stress to the external leads.
3. Rapid cooling or heating

③ OPERATE AND STORAGE ENVIRONMENTS

Operate in clean environments. CCD image sensors are precise optical equipment that should not be subject to mechanical shocks. Exposure to high temperatures or humidity will affect the characteristics. So avoid storage or usage in such conditions.

Keep in a case to protect from dust and dirt. Dew condensation may occur on CCD image sensors when the devices are transported from a low-temperature environment to a high-temperature environment. Avoid such rapid temperature changes.

For more details, refer to our document "Review of Quality and Reliability Handbook" (C12769E)

④ ELECTROSTATIC BREAKDOWN

CCD image sensor is protected against static electricity, but destruction due to static electricity is sometimes detected. Before handling be sure to take the following protective measures.

1. Ground the tools such as soldering iron, radio cutting pliers of or pincer.
2. Install a conductive mat or on the floor or working table to prevent the generation of static electricity.
3. Either handle bare handed or use non-chargeable gloves, clothes or material.
4. Ionized air is recommended for discharge when handling CCD image sensor.
5. For the shipment of mounted substrates, use box treated for prevention of static charges.
6. Anyone who is handling CCD image sensors, mounting them on PCBs or testing or inspecting PCBs on which CCD image sensors have been mounted must wear anti-static bands such as wrist straps and ankle straps which are grounded via a series resistance connection of about 1 MΩ.

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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