

### Description

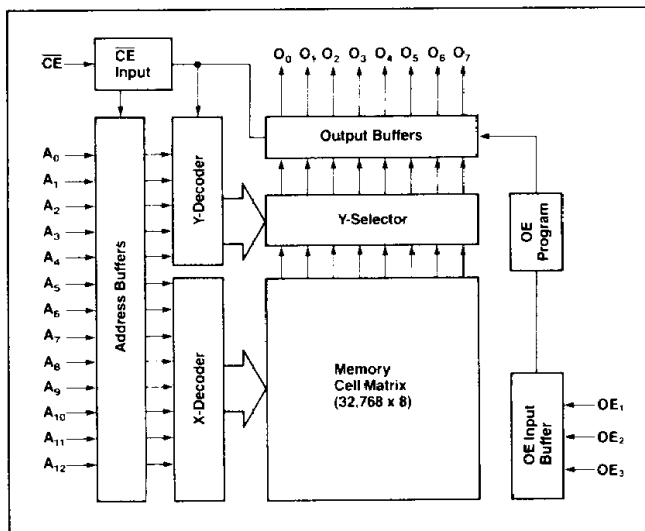
The μPD2364E is a 65,536-bit Read-only Memory utilizing NMOS silicon gate technology. The device is static in operation, organized as 8,192 words by 8 bits and operates from a single +5V power supply. The device has three-state outputs and all inputs and outputs are fully TTL-compatible. The chip select pins are mask-programmable and can be specified by selecting 1, 0, and Don't-care data. Pinout is compatible with 2764 EPROMs.

### Features

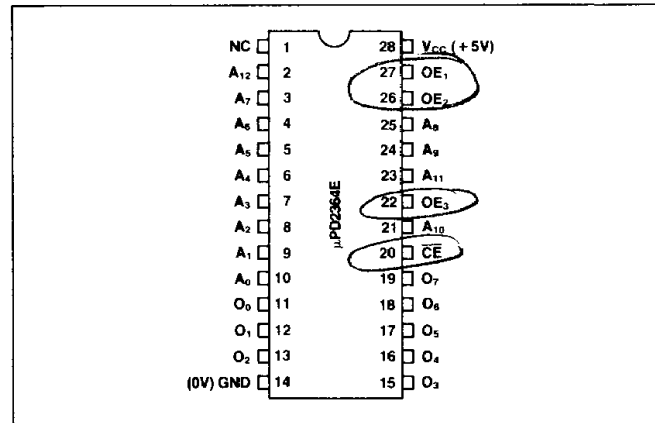
- All inputs and outputs are fully TTL-compatible
- Three-state outputs for direct bus compatibility
- Single +5V ± 5% power supply
- Three mask-programmable chip selects
- 2 performance ranges:

Device	Access Time	Power Supply	
		Active	Standby
μPD2364E	250ns	80mA	20mA
μPD2364E-1	200ns	80mA	20mA

### Block Diagram



### Pin Configuration



### Pin Identification

Pin		
No.	Symbol	Function
1	NC	No Connection.
2-10, 21, 23-25	A <sub>0</sub> -A <sub>12</sub>	Address Inputs.
11-13, 15-19	O <sub>0</sub> -O <sub>7</sub>	Three-state Data Outputs.
14	GND	Ground.
20	CE	Chip Enable.
22, 26-27	OE <sub>1</sub> -OE <sub>3</sub>	Mask-programmable Chip Selects.
28	V <sub>CC</sub>	Single +5V Power Supply.

**Absolute Maximum Ratings\***

Supply Voltage, V <sub>CC</sub>	-0.5V to +7V
Input Voltage, V <sub>I</sub>	-0.5V to +7V
Output Voltage, V <sub>O</sub>	-0.5V to +7V
Operating Temperature, T <sub>OPR</sub>	-10°C to +70°C
Storage Temperature, T <sub>STG</sub>	-65°C to +150°C

\*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Capacitance**

T<sub>A</sub> = -10°C to +70°C

Parameter	Symbol	Limits						Unit	Test Conditions
		μPD2364E			μPD2364E-1				
		Min	Typ	Max	Min	Typ	Max		
Input Capacitance	C <sub>i</sub>		10		10		pF	f = 1MHz	
Output Capacitance	C <sub>o</sub>		15		15		pF	f = 1MHz	

**DC Characteristics**

T<sub>A</sub> = -10°C to +70°C; V<sub>CC</sub> = +5V ± 5%

Parameter	Symbol	Limits			Unit	Test Conditions
		Min	Typ	Max		
Input High Voltage	V <sub>IH</sub>	+2.1	V <sub>CC</sub> + 1.0		V	
Input Low Voltage	V <sub>IL</sub>	-0.5	+0.7		V	
Output High Voltage	V <sub>OH</sub>	+2.4			V	I <sub>OH</sub> = -400μA
Output Low Voltage	V <sub>OL</sub>		+0.4		V	I <sub>OL</sub> = +2.1mA
Input Leakage Current High	I <sub>LH</sub>		+10		μA	V <sub>I</sub> = V <sub>CC</sub>
Input Leakage Current Low	I <sub>LL</sub>		-10		μA	V <sub>I</sub> = 0V
Output Leakage Current High	I <sub>LOH</sub>		+10		μA	V <sub>O</sub> = V <sub>CC</sub> , chip deselected
Output Leakage Current Low	I <sub>LOL</sub>		-10		μA	V <sub>O</sub> = 0V, chip deselected
Supply Voltage Current	I <sub>CC1</sub>		45	80	mA	CE = V <sub>IL</sub>
Supply Voltage Current	I <sub>CC2</sub>		12	20	mA	CE = V <sub>IH</sub> , standby mode

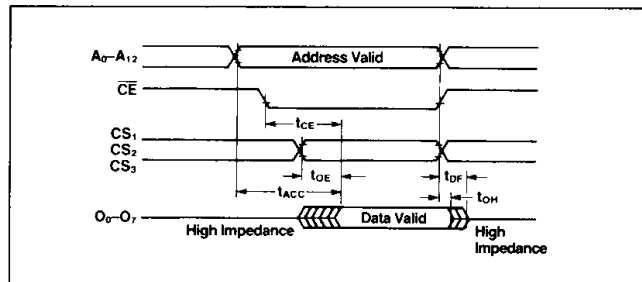
**AC Characteristics**

T<sub>A</sub> = -10°C to +70°C; V<sub>CC</sub> = +5 ± 5%

Parameter	Symbol	Limits						Unit	Test Conditions <sup>①</sup>
		μPD2364E			μPD2364E-1				
		Min	Typ	Max	Min	Typ	Max		
Access Time	t <sub>ACC</sub>		250		200		ns		
Chip Enable Access Time	t <sub>CE</sub>		250		200		ns		
OE <sub>1</sub> to OE <sub>3</sub> Output On Time	t <sub>OE</sub>	10	110	10	100		ns		
Output Hold Time	t <sub>OH</sub>	0		0			ns		
Output Disable Time	t <sub>DF</sub>	0	100	0	90		ns		

Notes: ① Input rise and fall times (t<sub>r</sub>, t<sub>f</sub>): 20ns  
Timing reference levels: Input and Output voltages = 0.8V and 2.0V  
Load = 1 TTL + 100 pF

**Timing Waveform**



**Definitions**

**Access Time, t<sub>ACC</sub>**

Access time is the maximum time between the application of a valid address and the corresponding valid data out.

**Output Hold Delay, t<sub>OH</sub>**

Output hold delay is the minimum time after an address change that the previous data remains valid.

**Chip Enable Access Time, t<sub>CE</sub>**

The maximum time between application of a valid chip enable input and the corresponding valid outputs.

**Output Enable Time, t<sub>OE</sub>**

Output enable time is the maximum delay between chip selects becoming true and output data becoming valid.

**Output Disable Time, t<sub>DF</sub>**

Output disable time is the delay between chip selects or chip enable becoming false and output stages going to the high impedance state. t<sub>DF</sub> is specified as CE or OE, whichever comes first.

**Custom Programming Instructions**

**Bit pattern submittal options**

The customer's unique bit pattern can be submitted in several convenient methods that are easy for the ROM customer, and readily verifiable for accuracy. The bit pattern can be delivered to NEC contained within:

1. One programmed 2764 EPROM
2. Two programmed 2732 EPROMs

**Bit pattern verification**

For customer verification of the submitted bit pattern, several alternatives are also available. The following are those found to be most expeditious.

**Customer Pattern Submitted Via**

**Verification Routine**

1. One programmed 2764 EPROM	Customer sends NEC one additional erased 2764. NEC programs the spare 2764 with the data from the programmed 2764, and returns it to the customer for verification.
2. Two programmed 2732 EPROMs	Customer sends NEC two additional erased 2732s. NEC programs the spare 2732s with the data from the programmed EPROMs and returns them to the customer for verification.