

7300 PIXELS \times 3 COLOR CCD LINEAR IMAGE SENSOR**DESCRIPTION**

The μ PD3728DZ is a high-speed and high sensitive color CCD (Charge Coupled Device) linear image sensor which changes optical images to electrical signal and has the function of color separation.

The μ PD3728DZ has 3 rows of 7300 pixels, and it is a 2-output/color type CCD sensor with 2 rows/color of charge transfer register, which transfers the photo signal electrons of 7300 pixels separately in odd and even pixels. Therefore, it is suitable for 600 dpi/A3 high-speed color digital copiers and so on.

FEATURES

- Valid photocell : 7300 pixels \times 3
- Photocell pitch : 10 μ m
- Line spacing : 40 μ m (4 lines) Red line - Green line, Green line - Blue line
- Color filter : Primary colors (red, green and blue), pigment filter (with light resistance 10^7 lx \cdot hour)
- Resolution : 24 dot/mm A3 (297 \times 420 mm) size (shorter side)
- Drive clock level : CMOS output under 5 V operation
- Data rate : 40 MHz MAX. (20 MHz/1 output)
- Output type : 2 outputs in phase/color
- Power supply : +12 V
- On-chip circuits : Reset feed-through level clamp circuits
Voltage amplifiers

ORDERING INFORMATION

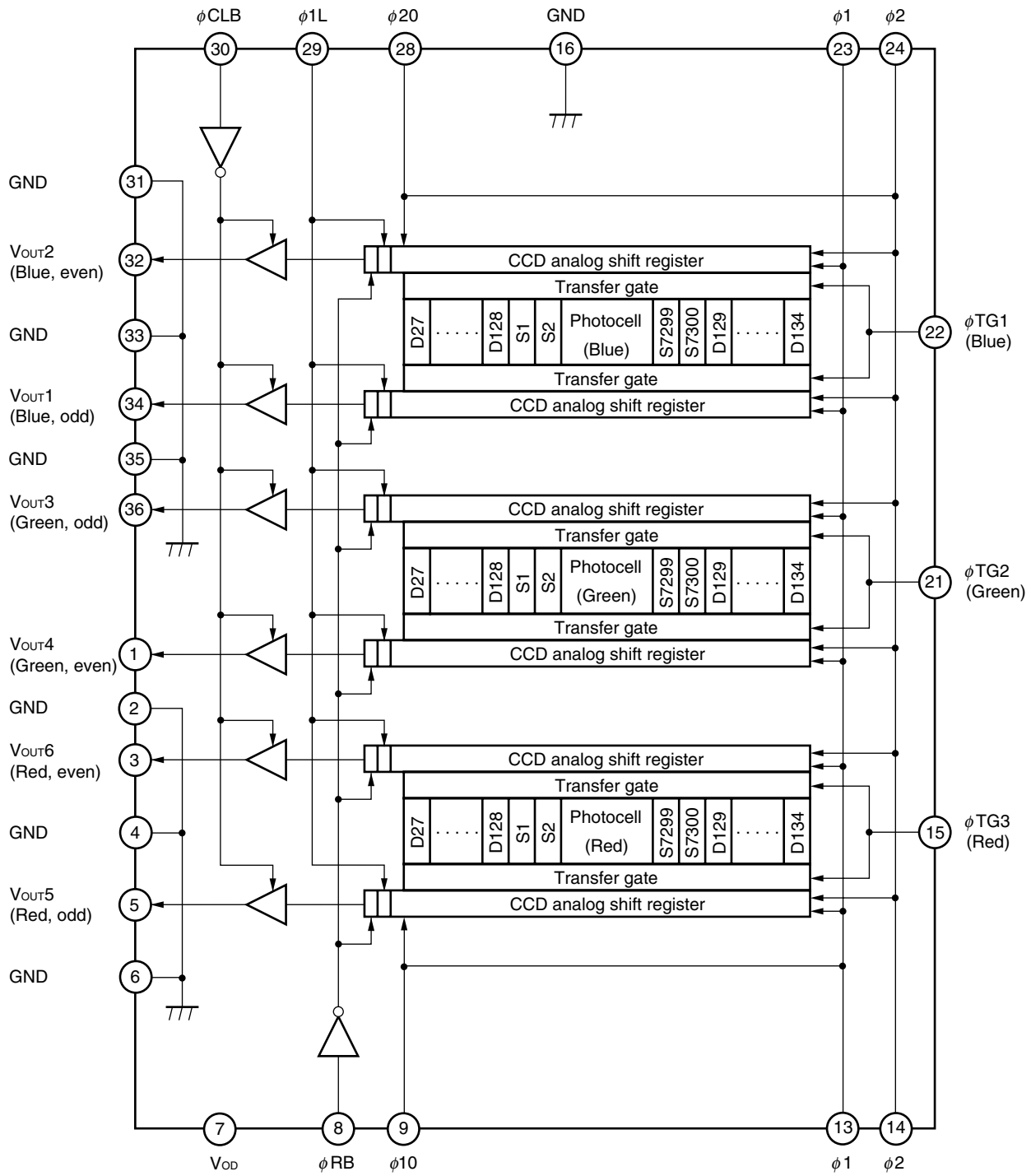
Part Number	Package
μ PD3728DZ-AZ	CCD linear image sensor 36-pin ceramic DIP (CERDIP) (15.24 mm (600))

<R> **Remark** The μ PD3728DZ-AZ is a lead-free product.

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Not all products and/or types are available in every country. Please check with an NEC Electronics sales representative for availability and additional information.

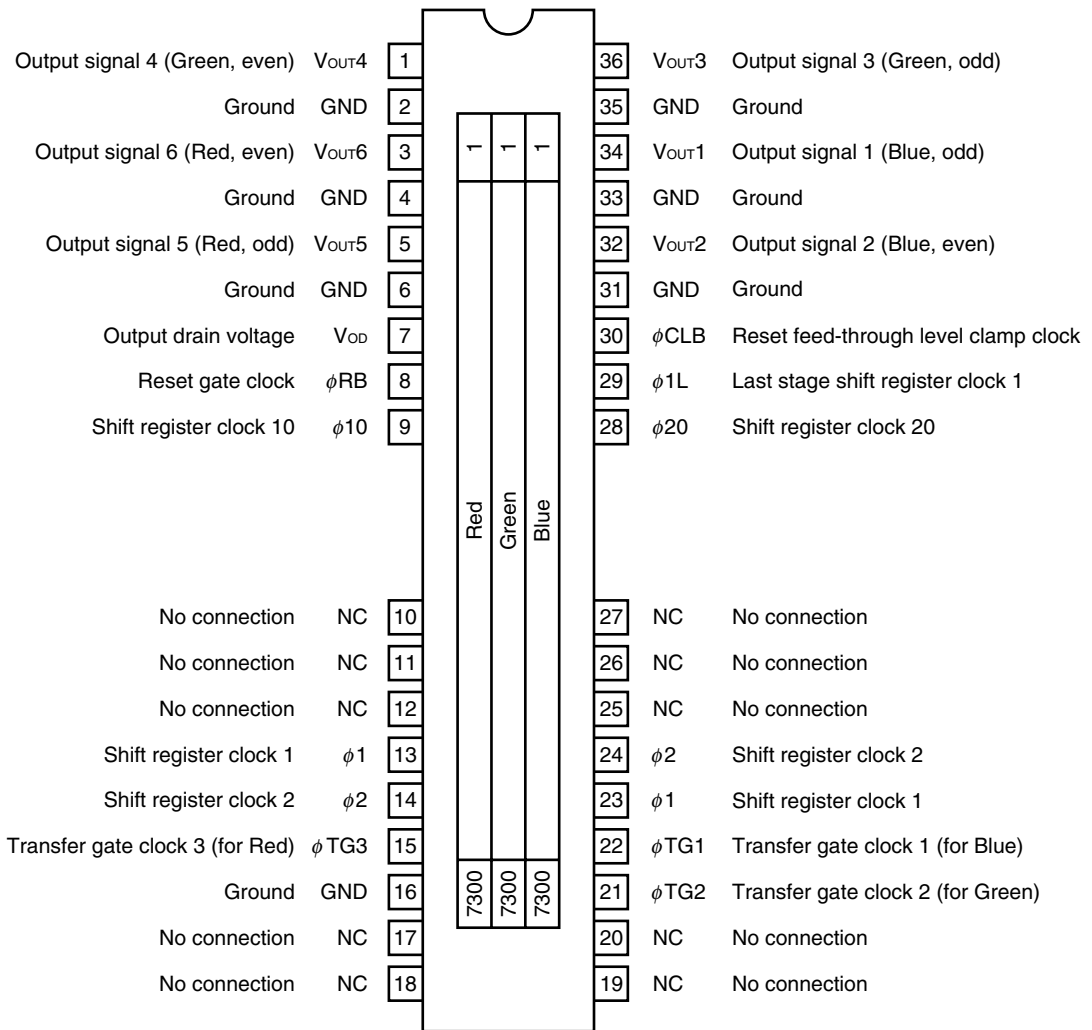
BLOCK DIAGRAM



PIN CONFIGURATION (Top View)

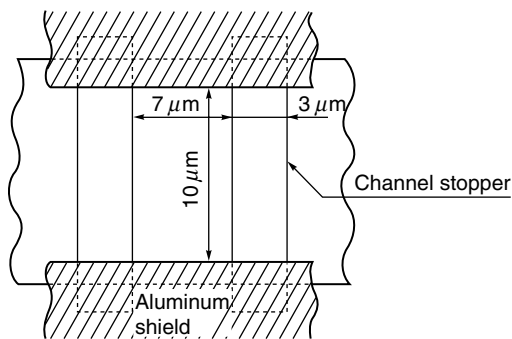
CCD linear image sensor 36-pin ceramic DIP (CERDIP) (15.24 mm (600))

• μPD3728DZ-AZ

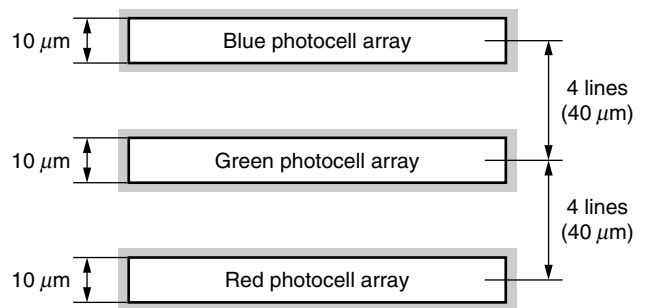


Caution Connect the No connection pins (NC) to GND.

PHOTOCELL STRUCTURE DIAGRAM



PHOTOCELL ARRAY STRUCTURE DIAGRAM (Line spacing)



ABSOLUTE MAXIMUM RATINGS (T_A = +25°C)

Parameter	Symbol	Ratings	Unit
Output drain voltage	V _{OD}	-0.3 to +15	V
Shift register clock voltage	V _{φ1} , V _{φ1L} , V _{φ10} , V _{φ2} , V _{φ20}	-0.3 to +8	V
Reset gate clock voltage	V _{φRB}	-0.3 to +8	V
Reset feed-through level clamp clock voltage	V _{φCLB}	-0.3 to +8	V
Transfer gate clock voltage	V _{φTG1} to V _{φTG3}	-0.3 to +8	V
Operating ambient temperature ^{Note}	T _A	-25 to +60	°C
Storage temperature	T _{stg}	-40 to +100	°C

Note Use at the condition without dew condensation.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

RECOMMENDED OPERATING CONDITIONS (T_A = +25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Output drain voltage	V _{OD}	11.4	12.0	12.6	V
Shift register clock high level	V _{φ1H} , V _{φ1LH} , V _{φ10H} , V _{φ2H} , V _{φ20H}	4.5	5.0	5.5	V
Shift register clock low level	V _{φ1L} , V _{φ1LL} , V _{φ10L} , V _{φ2L} , V _{φ20L}	-0.3	0	+0.5	V
Reset gate clock high level	V _{φRBH}	4.5	5.0	5.5	V
Reset gate clock low level	V _{φRBL}	-0.3	0	+0.5	V
Reset feed-through level clamp clock high level	V _{φCLBH}	4.5	5.0	5.5	V
Reset feed-through level clamp clock low level	V _{φCLBL}	-0.3	0	+0.5	V
Transfer gate clock high level	V _{φTG1H} to V _{φTG3H}	4.5	V _{φ1H} ^{Note} (V _{φ10H})	V _{φ1H} ^{Note} (V _{φ10H})	V
Transfer gate clock low level	V _{φTG1L} to V _{φTG3L}	-0.3	0	+0.5	V
Data rate	2f _{φRB}	-	2	40	MHz

Note When Transfer gate clock high level (V_{φTG1H} to V_{φTG3H}) is higher than Shift register clock high level (V_{φ1H} (V_{φ10H})), Image lag can increase.

Remark Pin 9 (φ10) and pin 28 (φ20) should be open to decrease the influence of input clock noise to output signal waveform, in case of operating at low or middle speed range; data rate under 24 MHz or so.

ELECTRICAL CHARACTERISTICS

$T_A = +25^{\circ}\text{C}$, $V_{OD} = 12\text{ V}$, $f_{\phi\text{RB}} = 1\text{ MHz}$, data rate = 2 MHz, storage time = 10 ms, input signal clock = 5 V_{p-p},
light source: 3200 K halogen lamp +C-500S (infrared cut filter, t = 1 mm)+HA-50 (heat absorbing filter, t = 3 mm)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Saturation voltage	V _{sat}		1.5	2.0	–	V
Saturation exposure	Red	SER	–	0.35	–	lx*s
	Green	SEG	–	0.39	–	lx*s
	Blue	SEB	–	0.31	–	lx*s
Photo response non-uniformity	PRNU	V _{OUT} = 1.0 V	–	6.0	18.0	%
Average dark signal ^{Note1}	ADS1	Light shielding	–	1.0	5.0	mV
	ADS2		–	0.5	5.0	mV
Dark signal non-uniformity ^{Note1}	DSNU1	Light shielding	–	2.0	5.0	mV
	DSNU2		–	1.0	5.0	mV
Power consumption	P _w		–	600	800	mW
Output impedance	Z _o		–	0.3	0.5	kΩ
Response	Red	R _R	3.9	5.6	7.3	V/lx*s
	Green	R _G	3.6	5.1	6.6	V/lx*s
	Blue	R _B	4.5	6.4	8.3	V/lx*s
Image lag ^{Note1}	IL1	V _{OUT} = 1.0 V	–	2.0	5.0	%
	IL2		–	1.0	5.0	%
Offset level ^{Note2}	V _{OS}		4.0	5.0	6.0	V
Output fall delay time ^{Note3}	t _d	V _{OUT} = 1.0 V	–	20	–	ns
Register imbalance	RI	V _{OUT} = 1.0 V	0	–	4.0	%
Total transfer efficiency	TTE	V _{OUT} = 1.0 V, data rate = 40 MHz	95	98	–	%
Response peak	Red		–	630	–	nm
	Green		–	540	–	nm
	Blue		–	460	–	nm
Dynamic range ^{Note1}	DR11	V _{sat} /DSNU1	–	1000	–	times
	DR12	V _{sat} /DSNU2	–	2000	–	times
	DR21	V _{sat} /σ _{bit1}	–	2000	–	times
	DR22	V _{sat} /σ _{bit2}	–	4000	–	times
Reset feed-through noise ^{Note2}	RFTN	Light shielding	–500	+200	+500	mV
Random noise ^{Note1}	σ _{bit1}	Light shielding, bit clamp mode (t _{cp} = 150 ns)	–	1.0	–	mV
	σ _{bit2}		–	0.5	–	mV
	σ _{line1}	Light shielding, line clamp mode (t ₁₉ = 3 μs)	–	4.0	–	mV
	σ _{line2}		–	2.0	–	mV

Notes 1. ADS1, DSNU1, IL1, DR11, DR21, σ_{bit1} and σ_{line1} show the specification of V_{OUT1} and V_{OUT2}.

ADS2, DSNU2, IL2, DR12, DR22, σ_{bit2} and σ_{line2} show the specification of V_{OUT3} to V_{OUT6}.

2. Refer to **TIMING CHART 2, 5**.

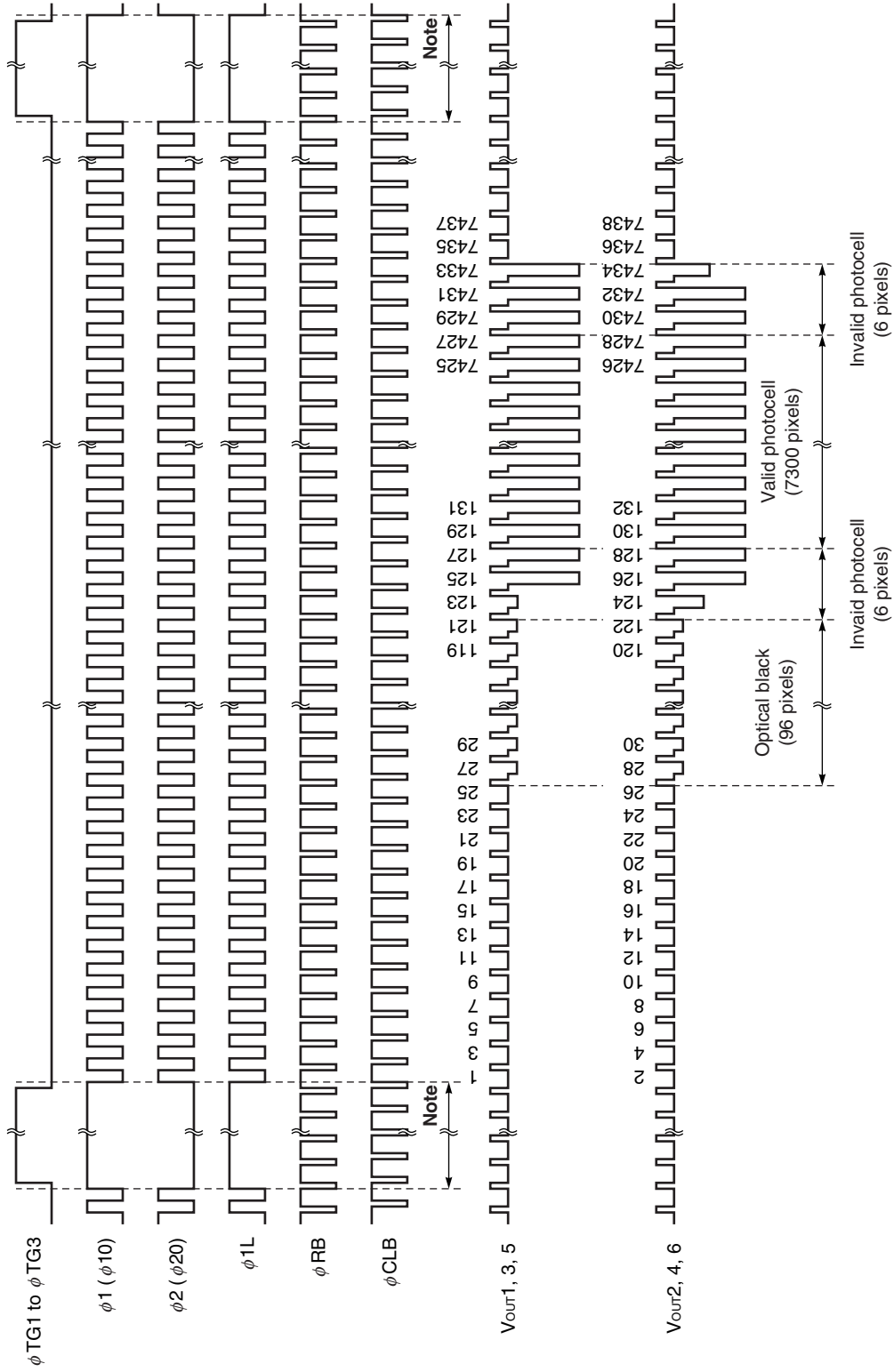
3. When the fall time of φ1L (t_{2'}) is the TYP. value (refer to **TIMING CHART 2, 5**).

INPUT PIN CAPACITANCE (T_A = +25°C, V_{OD} = 12 V)

Parameter	Symbol	Pin name	Pin No.	Min.	Typ.	Max.	Unit
Shift register clock pin capacitance 1	C _{φ1}	φ 1	13	–	350	500	pF
			23	–	350	500	pF
		φ 10	9	–	350	500	pF
Shift register clock pin capacitance 2	C _{φ2}	φ 2	14	–	350	500	pF
			24	–	350	500	pF
		φ 20	28	–	350	500	pF
Last stage shift register clock pin capacitance	C _{φL}	φ 1L	29	–	10	–	pF
Reset gate clock pin capacitance	C _{φRB}	φ RB	8	–	10	–	pF
Reset feed-through level clamp clock pin capacitance	C _{φCLB}	φ CLB	30	–	10	–	pF
Transfer gate clock pin capacitance	C _{φTG}	φ TG1	22	–	100	–	pF
		φ TG2	21	–	100	–	pF
		φ TG3	15	–	100	–	pF

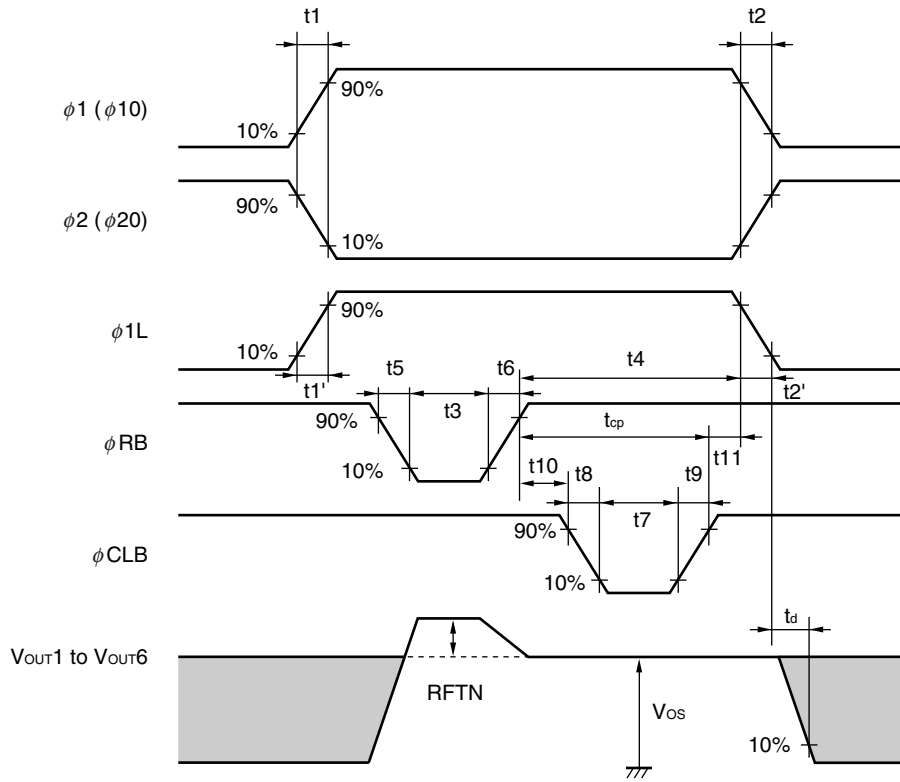
Remark Pins 13, 23 (φ 1) and pin 9 (φ 10) are connected each other inside of the device.
Pins 14, 24 (φ 2) and pin 28 (φ 20) are connected each other inside of the device.

TIMING CHART 1 (Bit clamp mode, for each color)



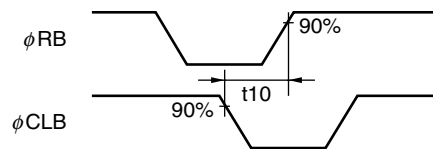
Note Input the ϕ RB and ϕ CLB pulses continuously during this period, too.

TIMING CHART 2 (Bit clamp mode, for each color)

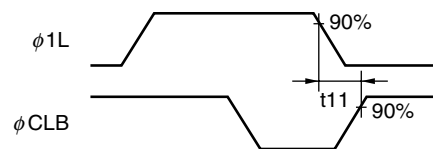


Symbol	Min.	Typ.	Max.	Unit
t_1, t_2	0	50	–	ns
t_1', t_2'	0	5	–	ns
t_3	17	50	–	ns
t_4	5	200	–	ns
t_5, t_6	0	20	–	ns
t_7	17	150	–	ns
t_8, t_9	0	20	–	ns
t_{10}	-10 ^{Note 1}	+50	–	ns
t_{11}	-5 ^{Note 2}	+50	–	ns
t_{cp}	5	150	–	ns

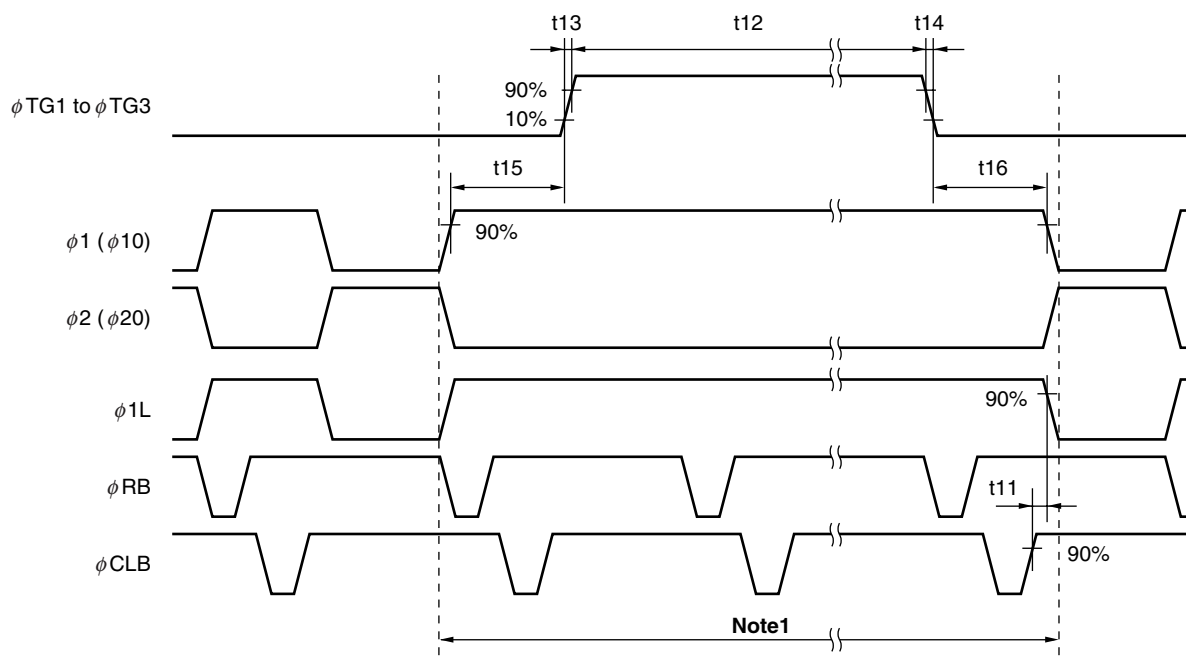
Notes 1. Min. of t_{10} shows that the ϕRB and ϕCLB overlap each other.



2. Min. of t_{11} shows that the $\phi 1L$ and ϕCLB overlap each other.

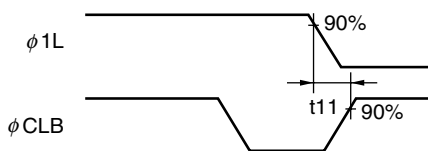


TIMING CHART 3 (Bit clamp, for each color)

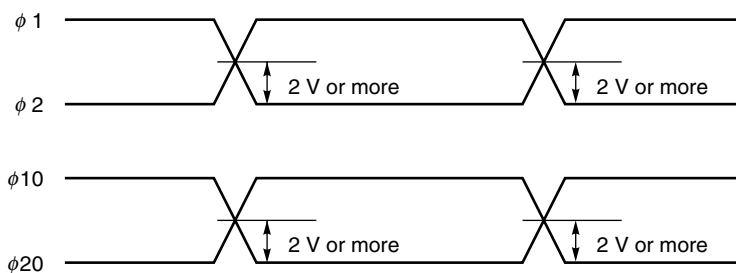


Symbol	Min.	Typ.	Max.	Unit
t11	-5 ^{Note 2}	+50	-	ns
t12	3000	10000	-	ns
t13, t14	0	50	-	ns
t15, t16	900	1000	-	ns

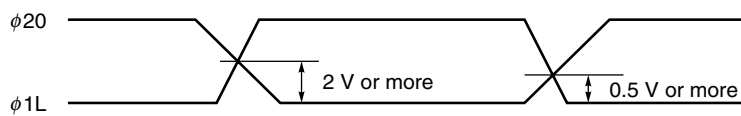
- Notes 1.** Input the ϕ RB and ϕ CLB pulses continuously during this period, too.
2. Min. of t11 shows that the ϕ 1L and ϕ CLB overlap each other.



$\phi 1, \phi 2$ and $\phi 10, \phi 20$ cross points

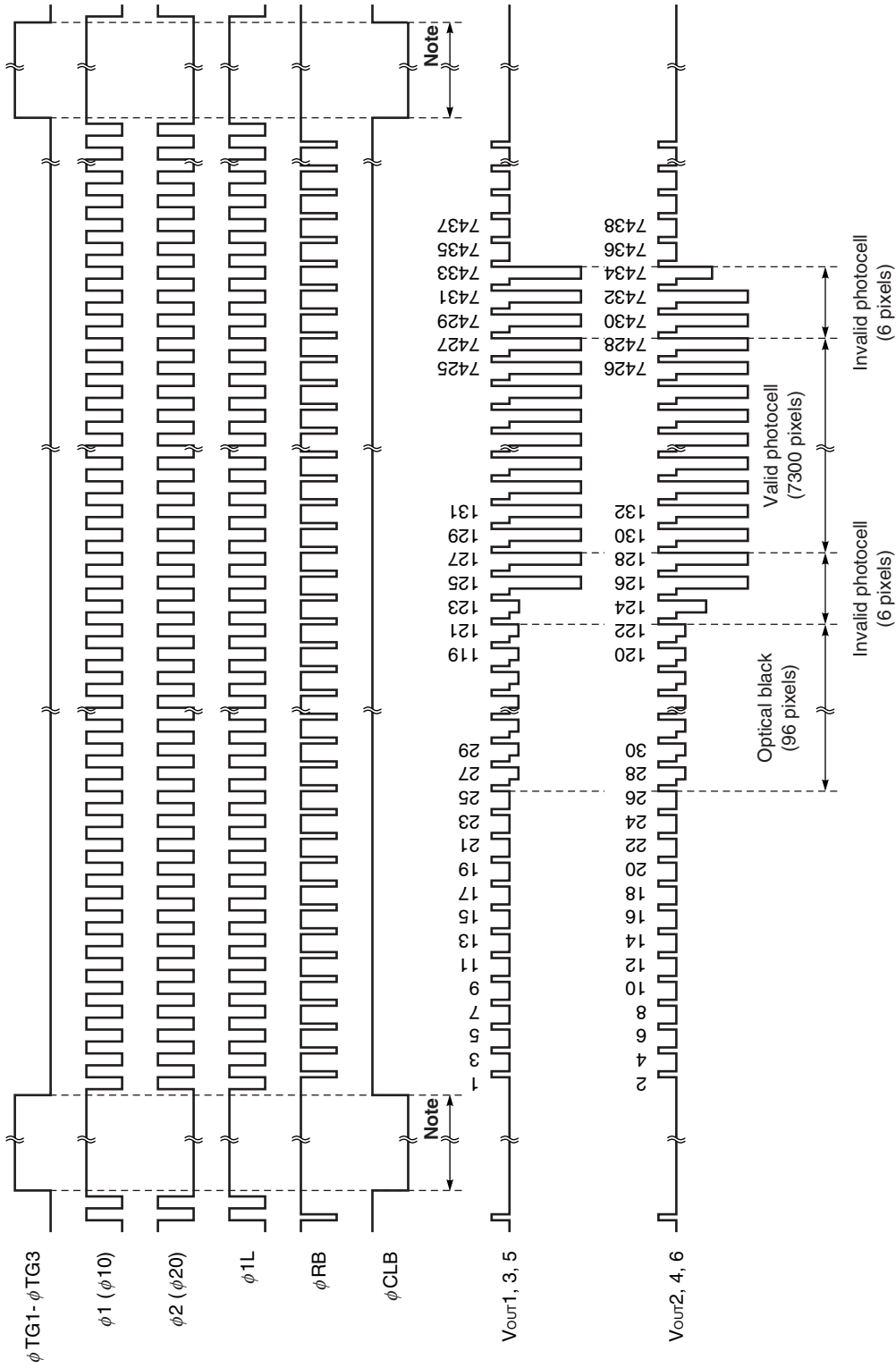


$\phi 1L, \phi 20$ cross points



Remark Adjust cross points ($\phi 1, \phi 2$), ($\phi 10, \phi 20$) and ($\phi 1L, \phi 20$) with input resistance of each pin.

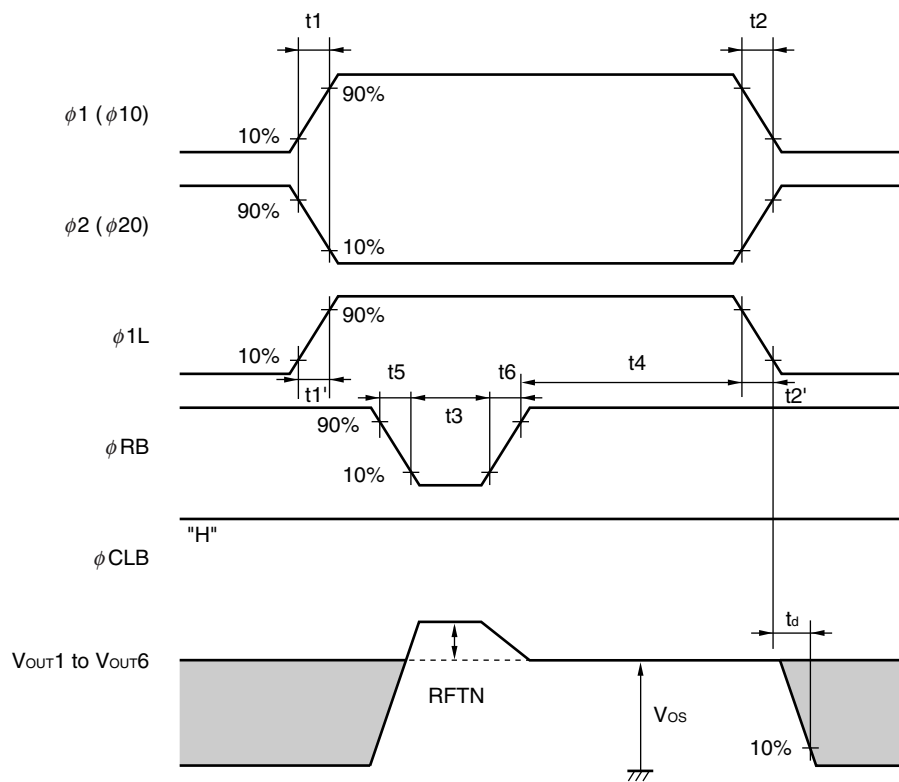
TIMING CHART 4 (Line clamp mode, for each color)



Note Set the ϕ RB pulse to high level during this period.

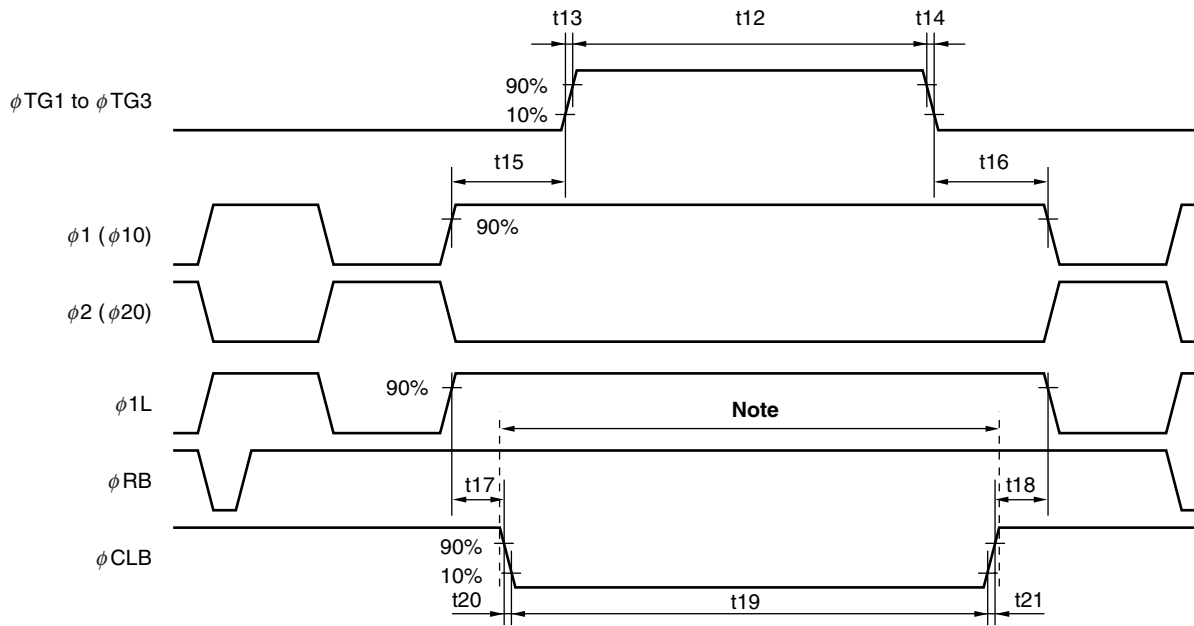
Remark Inverse pulse of ϕ TG1 to ϕ TG3 can be used as ϕ CLB.

TIMING CHART 5 (Line clamp mode, for each color)



Symbol	Min.	Typ.	Max.	Unit
t_1, t_2	0	50	–	ns
t_1', t_2'	0	5	–	ns
t_3	17	50	–	ns
t_4	5	200	–	ns
t_5, t_6	5	20	–	ns

TIMING CHART 6 (Line clamp mode, for each color)

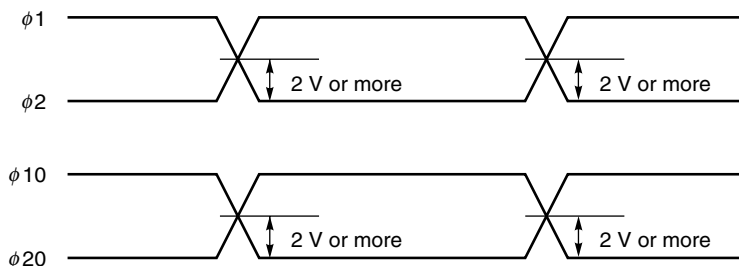


Symbol	Min.	Typ.	Max.	Unit
t_{12}	3000	10000	–	ns
t_{13}, t_{14}	0	50	–	ns
t_{15}, t_{16}	900	1000	–	ns
t_{17}, t_{18}	100	1000	–	ns
t_{19}	200	t_{12}	–	ns
t_{20}, t_{21}	0	20	–	ns

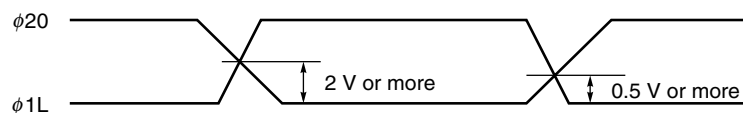
Note Set the ϕRB pulse to high level during this period.

Remark Inverse pulse of the $\phi TG1$ and $\phi TG3$ can be used as ϕCLB .

$\phi 1, \phi 2,$ and $\phi 10, \phi 20$ cross points



$\phi 1L, \phi 20$ cross points



Remark Adjust cross points ($\phi 1, \phi 2$), ($\phi 10, \phi 20$) and ($\phi 1L, \phi 20$) with input resistance of each pin.

DEFINITIONS OF CHARACTERISTIC ITEMS

1. Saturation voltage : **V_{sat}**
Output signal voltage at which the response linearity is lost.

2. Saturation exposure : **SE**
Product of intensity of illumination (lx) and storage time (s) when saturation of output voltage occurs.

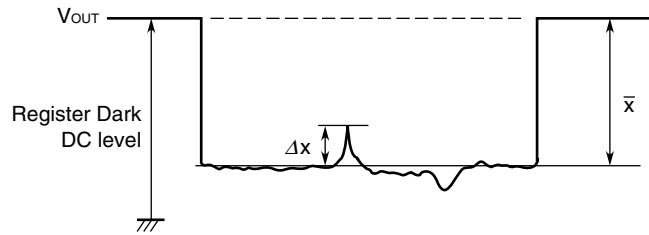
3. Photo response non-uniformity : **PRNU**
The output signal non-uniformity of all the valid pixels when the photosensitive surface is applied with the light of uniform illumination. This is calculated by the following formula.

$$PRNU (\%) = \frac{\Delta x}{\bar{x}} \times 100$$

Δx : maximum of $|x_j - \bar{x}|$

$$\bar{x} = \frac{\sum_{j=1}^{7300} x_j}{7300}$$

x_j : Output voltage of valid pixel number j



4. Average dark signal : **ADS**
Average output signal voltage of all the valid pixels at light shielding. This is calculated by the following formula.

$$ADS (mV) = \frac{\sum_{j=1}^{7300} d_j}{7300}$$

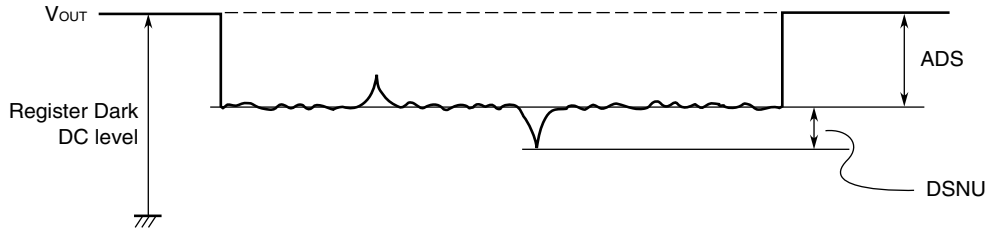
d_j : Dark signal of valid pixel number j

5. Dark signal non-uniformity : **DSNU**

Absolute maximum of the difference between ADS and voltage of the highest or lowest output pixel of all the valid pixels at light shielding. This is calculated by the following formula.

$$\text{DSNU (mV)} : \text{maximum of } |d_j - \text{ADS}|_{j=1 \text{ to } 7300}$$

d_j : Dark signal of valid pixel number j



6. Output impedance : **Zo**

Impedance of the output pins viewed from outside.

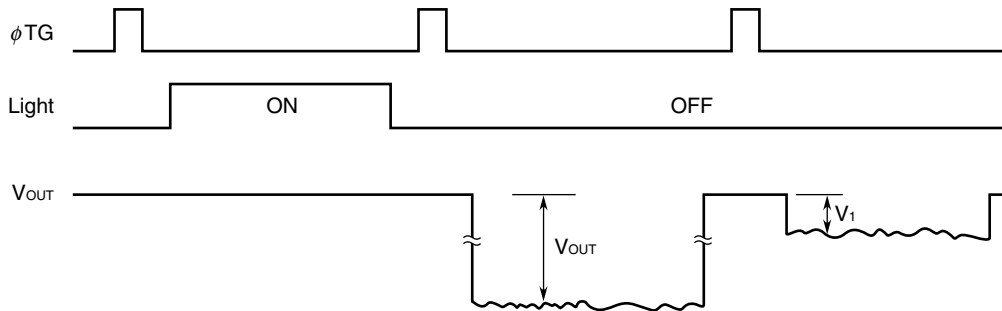
7. Response : **R**

Output voltage divided by exposure ($I \times s$).

Note that the response varies with a light source (spectral characteristic).

8. Image lag : **IL**

The rate between the last output voltage and the next one after read out the data of a line.



$$\text{IL (\%)} = \frac{V_1}{V_{\text{OUT}}} \times 100$$

9. Register imbalance : **RI**

The rate of the difference between the averages of the output voltage of Odd and Even pixels, against the average output voltage of all the valid pixels. This is calculated by the following formula.

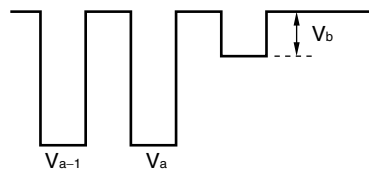
$$RI (\%) = \frac{\frac{2}{n} \left| \sum_{j=1}^{\frac{n}{2}} (V_{2j-1} - V_{2j}) \right|}{\frac{1}{n} \sum_{j=1}^n V_j} \times 100$$

n : Number of valid pixels
 V_j : Output voltage of each pixel

10. Total transfer efficiency : **TTE**

The total transfer rate of CCD analog shift register. This is calculated by the following formula, it is defined by each output.

$$TTE (\%) = (1 - V_b / \text{average output of all the valid pixels}) \times 100$$



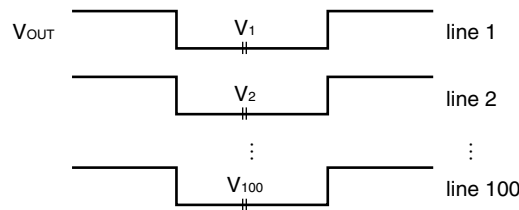
V_{a-1} : The last pixel output - 1 (Odd pixel: 7431st pixel)
 V_a : The last pixel output (Odd pixel: 7433rd pixel)
 V_b : The split pixel output (Odd pixel: 7435th pixel)

11. Random noise : **σ**

Random noise is defined as the standard deviation of a valid pixel output signal with 100 times (=100 lines) data sampling at dark (light shielding). This is calculated by the following formula.

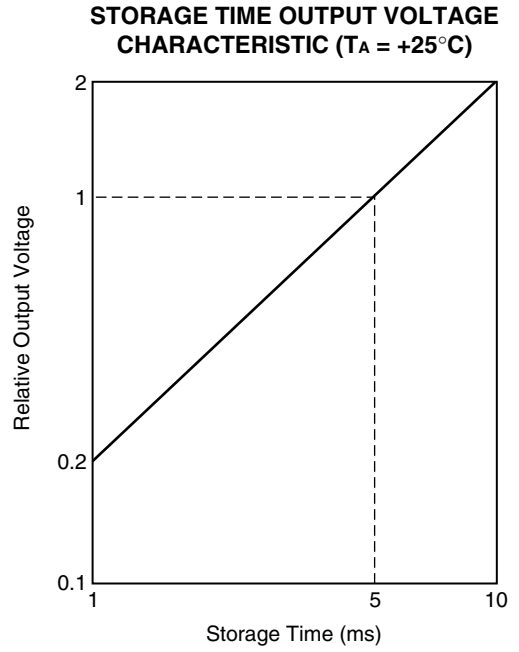
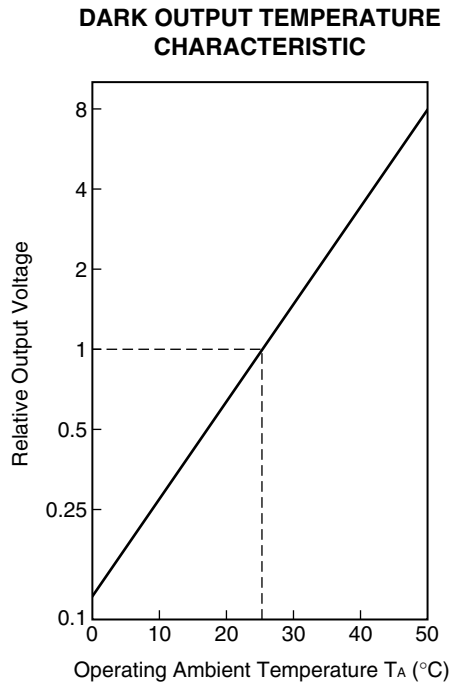
$$\sigma (mV) = \sqrt{\frac{\sum_{i=1}^{100} (V_i - \bar{V})^2}{100}}, \quad \bar{V} = \frac{1}{100} \sum_{i=1}^{100} V_i$$

V_i : A valid pixel output signal among all of the valid pixels for each color

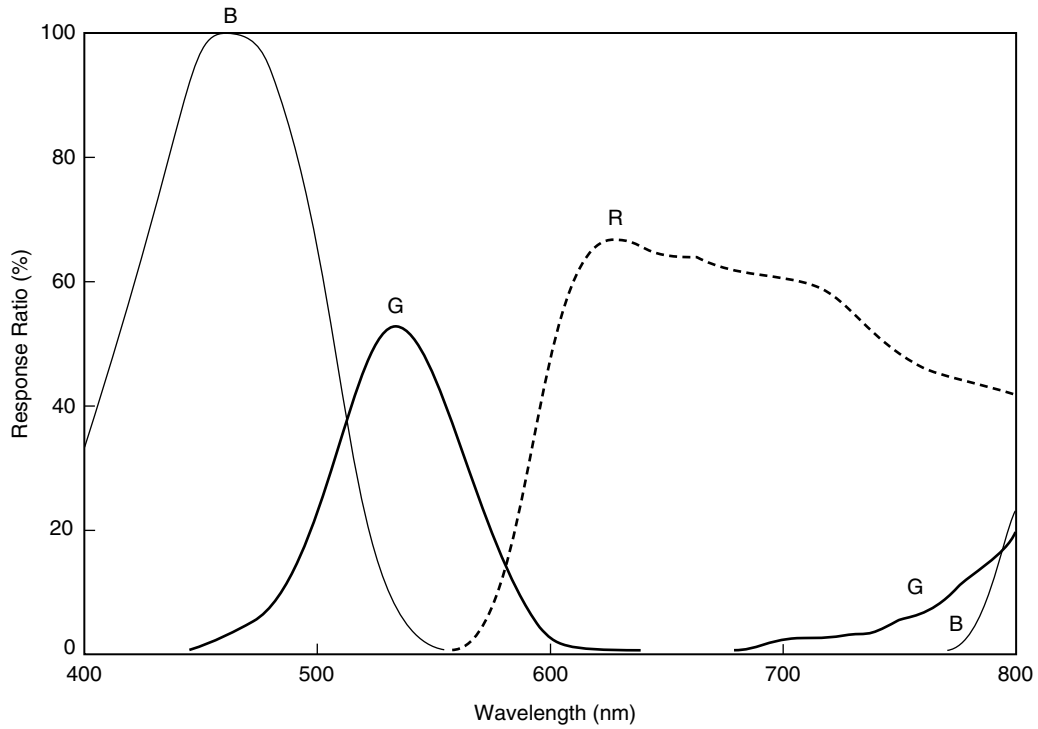


This is measured by the DC level sampling of only the signal level, not by CDS (Correlated Double Sampling).

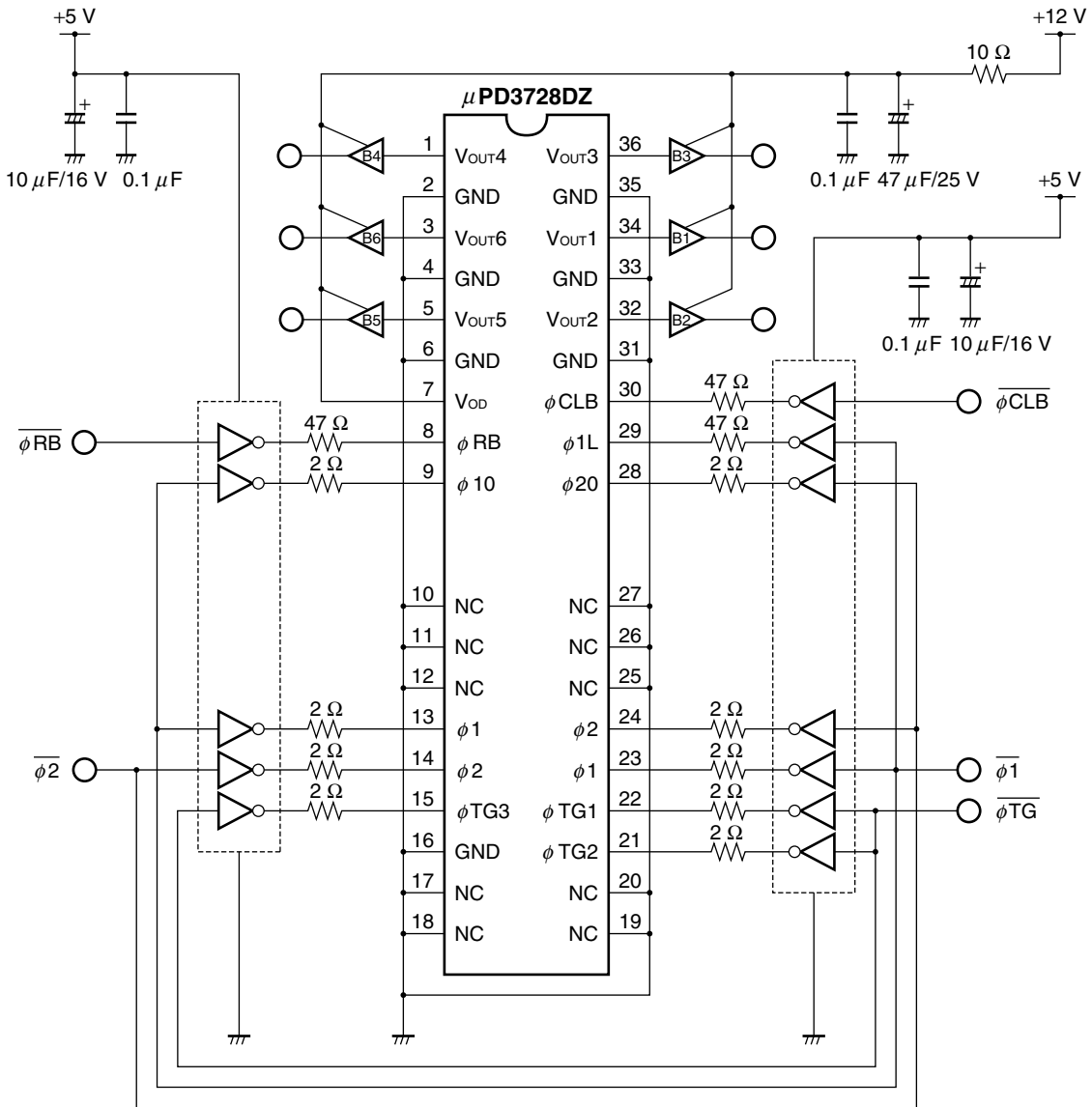
STANDARD CHARACTERISTIC CURVES (Reference Value)



TOTAL SPECTRAL RESPONSE CHARACTERISTICS (without infrared cut filter and heat absorbing filter) ($T_A = +25^\circ\text{C}$)

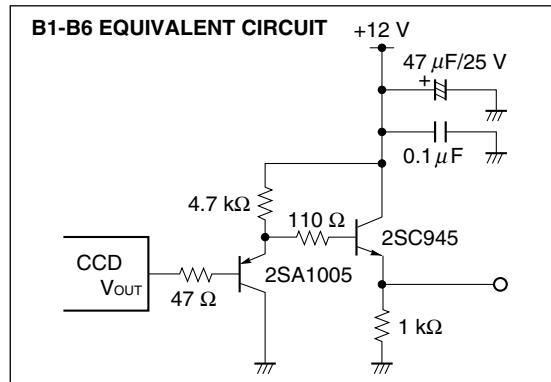


APPLICATION CIRCUIT EXAMPLE



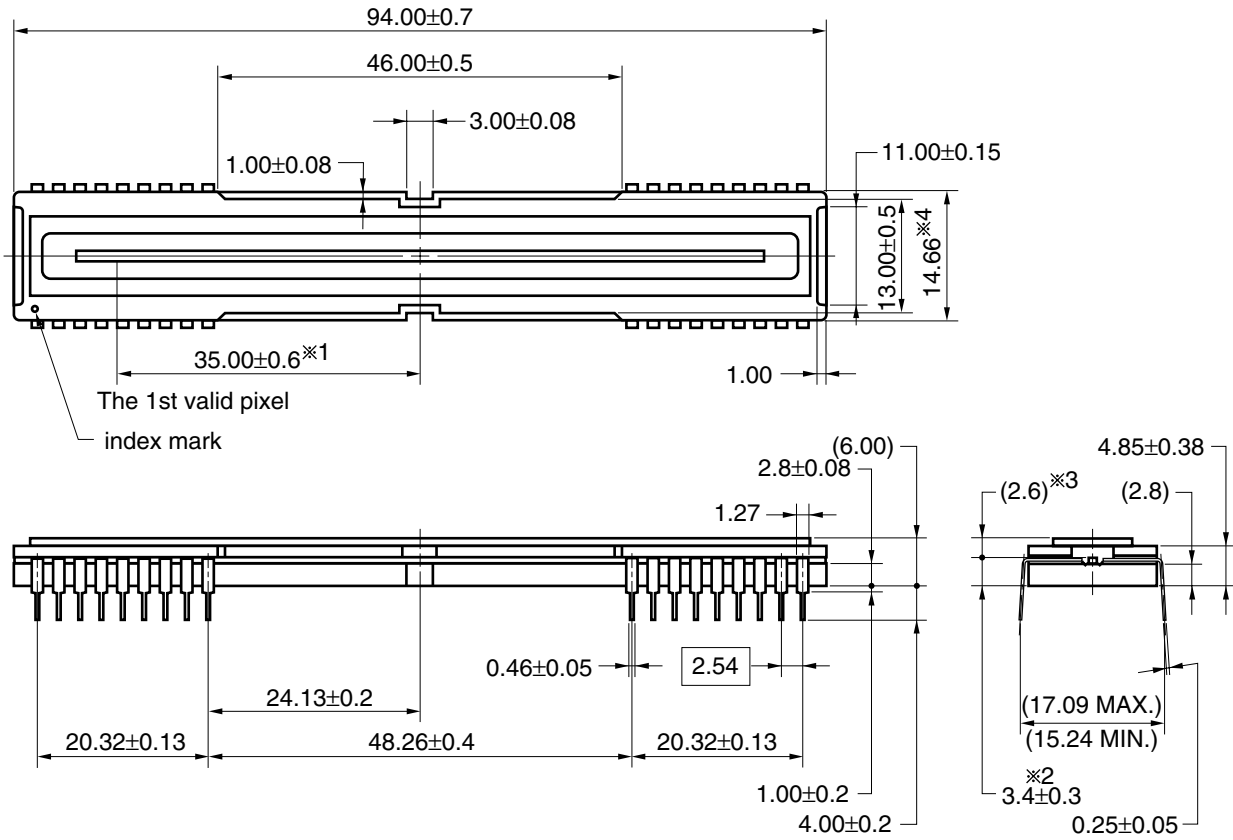
Caution Connect the No connection pins (NC) to GND.

- Remarks 1. Pin 9 (ϕ 10) and pin 28 (ϕ 20) should be open to decrease the influence of input clock noise to output signal waveform, in case of operating at low or middle speed range; data rate under 24 MHz or so.
- 2. Inverters shown in the above application circuit example are the 74AC04.
- 3. B1 to B6 in the application circuit example are shown in the figure below.



PACKAGE DRAWING

CCD LINEAR IMAGE SENSOR 36-PIN CERAMIC DIP (15.24 mm (600))



Name	Dimensions	Refractive index
Glass cap	93.0 × 9.0 × 1.1	1.5

- ※ 1 1st valid pixel ↔ Center of package
- ※ 2 The bottom of package ↔ The surface of the chip
- ※ 3 The surface of the chip ↔ The surface of the glass cap
- ※ 4 The tolerance of package dimension
 - ±0.25 : less than 10mm from W/F edge
 - ±0.50 : equal or more than 10mm from W/F edge

36D-1CCD-PKG2-4

RECOMMENDED SOLDERING CONDITIONS

When soldering this product, it is highly recommended to observe the conditions as shown below.

If other soldering processes are used, or if the soldering is performed under different conditions, please make sure to consult with our sales offices.

Type of Through-hole Device

μPD3728DZ-AZ : CCD linear image sensor 36-pin ceramic DIP (CERDIP) (15.24 mm (600))

Process	Conditions
Partial heating method	Pin temperature : 300 °C or below, Heat time : 3 seconds or less (per pin)

- Cautions**
1. **During assembly care should be taken to prevent solder or flux from contacting the glass cap. The optical characteristics could be degraded by such contact.**
 2. **Soldering by the solder flow method may have deleterious effects on prevention of glass cap soiling and heat resistance. So the method cannot be guaranteed.**

NOTES ON HANDLING THE PACKAGES

① MOUNTING OF THE PACKAGE

The application of an excessive load to the package may cause the package to warp or break, or cause chips to come off internally. Particular care should be taken when mounting the package on the circuit board. Don't have any object come in contact with glass cap. You should not reform the lead frame. We recommended to use a IC-inserter when you assemble to PCB.

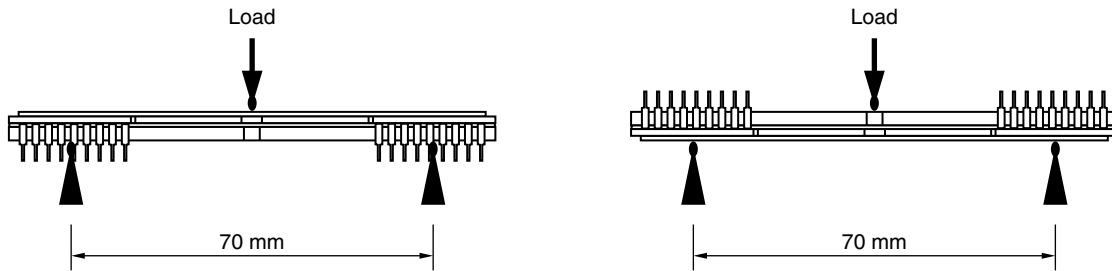
Also, be care that the any of the following can cause the package to crack or dust to be generated.

1. Applying heat to the external leads for an extended period of time with soldering iron.
2. Applying repetitive bending stress to the external leads.
3. Rapid cooling or heating

For this product, the reference value for the three-point bending strength ^{Note} is 180 [N] (at distance between supports: 70 mm). Avoid imposing a load, however, on the inside portion as viewed from the face on which the window (glass) is bonded to the package body (ceramic).

Note Three-point bending strength test

Distance between supports: 70 mm, Support R: R 2 mm, Loading rate: 0.5 mm/min.



② GLASS CAP

Don't either touch glass cap surface by hand or have any object come in contact with glass cap surface. Care should be taken to avoid mechanical or thermal shock because the glass cap is easily to damage. For dirt stuck through electricity ionized air is recommended.

NOTES ON HANDLING THE PACKAGES

③ OPERATE AND STORAGE ENVIRONMENTS

Operate in clean environments. CCD image sensors are precise optical equipment that should not be subject to mechanical shocks. Exposure to high temperatures or humidity will affect the characteristics. So avoid storage or usage in such conditions.

Keep in a case to protect from dust and dirt. Dew condensation may occur on CCD image sensors when the devices are transported from a low-temperature environment to a high-temperature environment. Avoid such rapid temperature changes.

For more details, refer to our document "Review of Quality and Reliability Handbook" (C12769E)

④ ELECTROSTATIC BREAKDOWN

CCD image sensor is protected against static electricity, but destruction due to static electricity is sometimes detected. Before handling be sure to take the following protective measures.

1. Ground the tools such as soldering iron, radio cutting pliers or pincer.
2. Install a conductive mat or on the floor or working table to prevent the generation of static electricity.
3. Either handle bare handed or use non-chargeable gloves, clothes or material.
4. Ionized air is recommended for discharge when handling CCD image sensor.
5. For the shipment of mounted substrates, use box treated for prevention of static charges.
6. Anyone who is handling CCD image sensors, mounting them on PCBs or testing or inspecting PCBs on which CCD image sensors have been mounted must wear anti-static bands such as wrist straps and ankle straps which are grounded via a series resistance connection of about 1 M Ω .

[MEMO]

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NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

• **The information in this document is current as of February, 2006. The information is subject to change without notice. For actual design-in, refer to the latest publications of NEC Electronics data sheets or data books, etc., for the most up-to-date specifications of NEC Electronics products. Not all products and/or types are available in every country. Please check with an NEC Electronics sales representative for availability and additional information.**

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