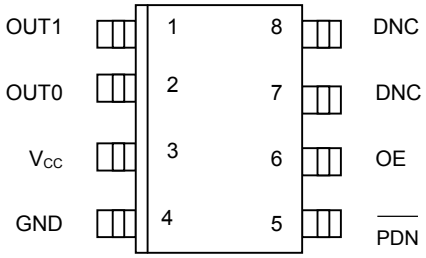
DS1073 Special EconOscillator/Divider

www.maxim-ic.com

FEATURES

- Dual Fixed frequency outputs (29.2 kHz to 100 MHz)
- No external components
- 0.5% Initial tolerance
- 1% variation over temperature and voltage
- Single 2.7Vto 3.6V supply
- Power-down mode
- Synchronous output gating



DS1073Z 150-MIL SOIC
DS1073M 300-MIL DIP

DESCRIPTION

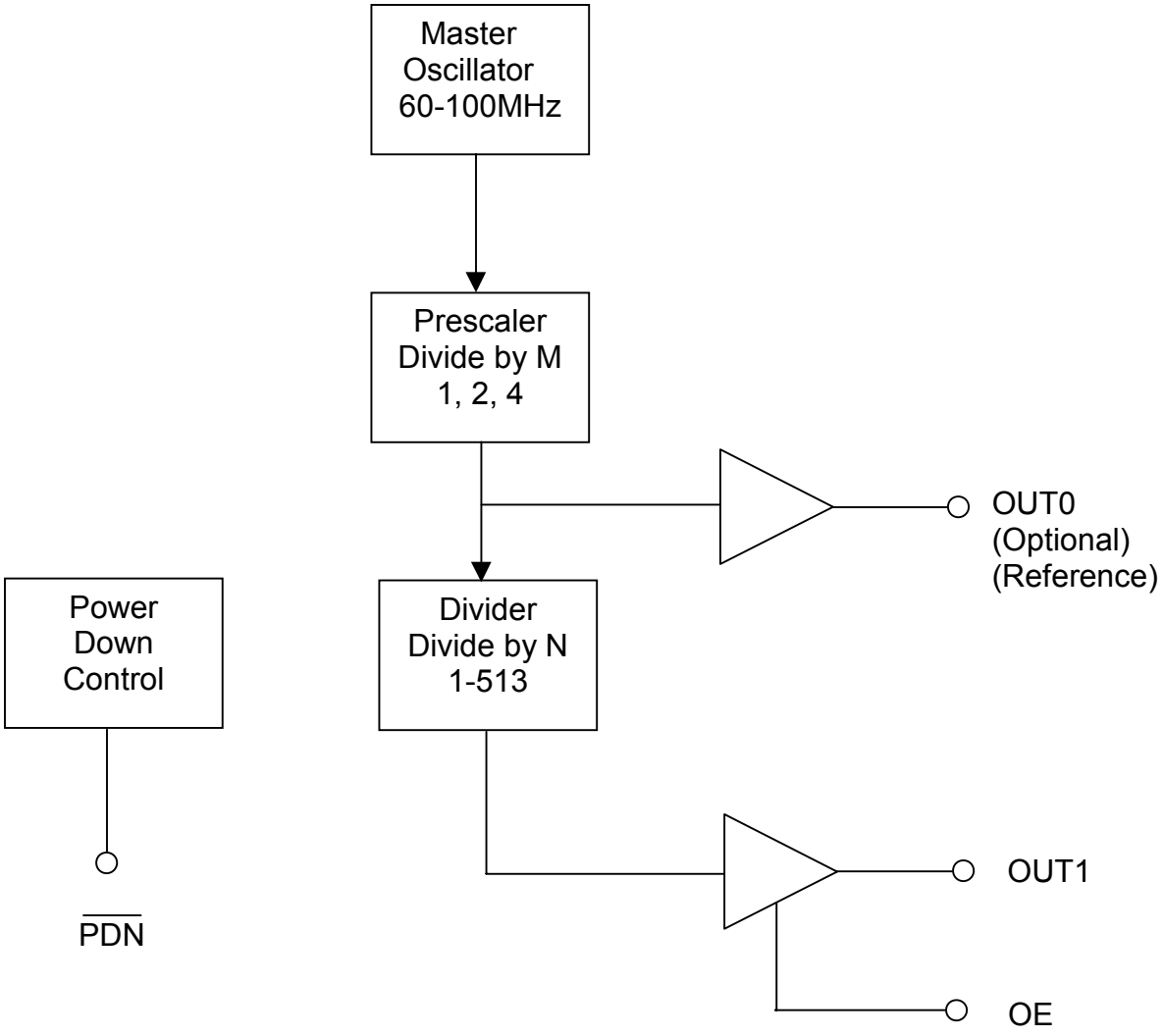
The DS1073 Special is a fixed frequency oscillator requiring no external components for operation. Numerous set operating frequencies are possible in the range 29.2 kHz to 100 MHz.

The DS1073 Special is shipped from the factory pre-programmed to a specific output frequency and mode of operation. The part is branded according to the device's master frequency (see DS1073 data sheet). The customer fills out a "1073 Special Order Form" with the required information and submits it to the factory for approval.

Contact the factory for availability of specific frequencies. In general, any frequency possible on a standard DS1073 can be made available.

The DS1073 special is available in 8-pin DIP or SOIC packages, allowing the generation of a clock signal easily, economically and using minimal board area.

BLOCK DIAGRAM Figure 1



1073 SPECIAL Order Form

Use this form for **DS1073 Special programmed EconOscillators .** All sections must be completed. Refer to the datasheet or contact the factory at (972) 371-6822 for assistance.

Parent Part Number: **DS1073**

Customer Name: _____

Customer Contact: _____

Customer Address: _____

_____

Customer Phone: (Area) _____ _____ _____

Salesman: _____

Sales Representative: _____

Distributor (if any): _____

Package: 300mil 8-pin DIP 150mil 8-pin SOIC (circle one)

Parent Device: **DS** _____ (part will be branded with this speed)

Master Frequency: _____ **MHz** **Standard or Special** (circle one)
(60,66,80 or 100MHz)

Reference Output: ☐ Disabled ☐ Enabled - Frequency _____
(Equals master frequency/M)

Output Frequency: _____ (Equals master frequency/MN)

Prescaler (M) : _____ **Divider (N):** _____

Special Instructions (Tape & Reel, etc.):

_____

_____

_____

_____

_____

Customer Signature: _____
(acknowledges acceptance of special settings)

Fax the completed form to Louis Grantham at (972) 371-4799 (FAX).

PIN DESCRIPTIONS

Output Pin (OUT1 pin): This pin is the main oscillator output.

Output Enable Function (OE pin): The DS1073 Special features a "synchronous" output enable. When OE is at a high logic level the oscillator free runs. When this pin is taken low OUT1 is held low, immediately if OUT1 is already low, or at the next high-to-low transition if OUT1 is high. This prevents any possible truncation of the output pulse width when the enable is used. While the output is disabled the master oscillator continues to run (producing an output at OUT0, if the $\overline{EN0}$ bit = 0) but the internal counters (/N) are reset. This results in a constant phase relationship between OE's return to a high level and the resulting OUT1 signal. When the enable is released OUT1 will make its first transition within one to two clock periods of the master clock.

Power-Down ($\overline{PDN}$ pin): A low logic level on this pin can be used to make the device stop oscillating (active low) and go into a reduced power consumption state. Internal "Enabling Sequencer" circuitry will first disable OUT in the same way as when OE is used. Next OUT0 will be disabled in a similar fashion. Finally the oscillator circuitry will be disabled. In this mode both outputs will go into a high impedance state. The power consumption in the power-down state is much less than if OE is used because the internal oscillator is completely powered down. Consequently the device will take considerably longer to recover (i.e., achieve stable oscillation) from a power-down condition than if the OE is used.

Reference Output (OUT0 pin): A reference output, OUT0, is also available from the output of the prescaler. OUT0 is unaffected by the OE pin, but is disabled in a glitchless fashion if the device is powered down. If this output is not required it can be permanently disabled and there will be a corresponding reduction in overall power consumption. The availability of this output and its frequency are specified on the special order form.

DNC: Do not connect.

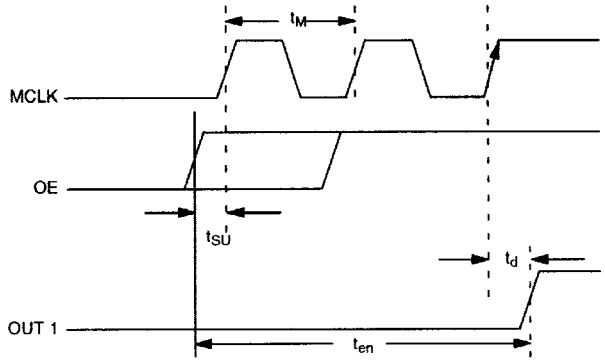
OPERATION OF OUTPUT ENABLE

Since the output enable and internal master oscillator are asynchronous there is the possibility of timing difficulties in the application. To minimize these difficulties the DS1073 features an "enabling sequencer" to produce predictable results when the device is enabled and disabled. In particular the output gating is configured so that truncated output pulses can never be produced.

ENABLE TIMING

The output enable function is produced by sampling the OE input with the output from the pre-scaler mux (MCLK) and gating this with the output from the programmable divider. The exact behavior of the device is therefore dependent on the setup time (t_{SU}) from a transition on the OE input to the rising edge of MCLK. If the actual setup time is less than T_{SUEM} then one more complete cycle of MCLK will be required to complete the enable or disable operation (see diagrams). This is unlikely to be of any consequence in most applications, and then only if the value for N is small. In general, the output will make its first positive transition between approximately one and two clock periods of MCLK after the rising edge of OE. (Figure 2)

Figure 2



t_M = PERIOD OF MCLK
t_d = PROP DELAY FROM MCLK ↑ TO OUT ↑

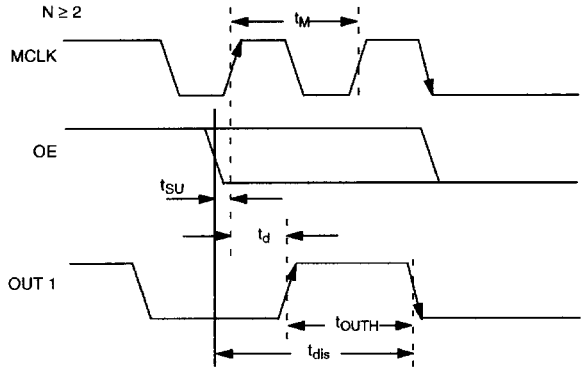
MAX VALUE OF $t_{en} = t_{SUEM} + 2\,t_M + t_d$
MIN VALUE OF $t_{en} = t_{SUEM} + t_M + t_d$

Disable Timing

If OE goes low while OUT1 is high, the output will be disabled on the completion of the output pulse. If OUT1 is low, the disabling behavior will be dependent on the setup time between the falling edge of OE and the rising edge of MCLK. If $t_{SU} < T_{SUEM}$ the result will be one additional pulse appearing on the output before disabling occurs.

If the device is in divide-by-one mode, the disabling occurs slightly differently. In this case if $t_{SU} > T_{SUEM}$ one additional output pulse will appear, if $t_{SU} < T_{SUEM}$ then two additional output pulses will appear. The following diagrams illustrate the timing in each of these cases. (Figure 3 and 4)

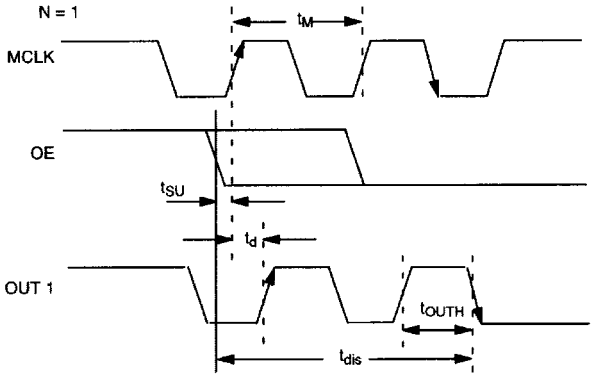
Figure 3



t_M = PERIOD OF MCLK
t_d = PROP DELAY FROM MCLK ↑ TO OUT ↑
t_{OUTH} = WIDTH OF OUTPUT PULSE

MAX VALUE OF $t_{dis} = t_{SUEM} + t_d + t_{OUTH}$
MIN VALUE OF $t_{dis} = 0$

Figure 4



t_M = PERIOD OF MCLK
t_d = PROP DELAY FROM MCLK ↑ TO OUT ↑
t_{OUTH} = WIDTH OF OUTPUT PULSE

MAX VALUE OF $t_{dis} = t_{SUEM} + t_d + t_{OUTH} + t_M$
MIN VALUE OF $t_{dis} = t_{SUEM} + t_d + t_{OUTH}$

POWER-DOWN CONTROL

POWER-DOWN

If $\overline{\text{PDN}}$ is taken low a power-down sequence is initiated. The "Enabling Sequencer" is used to execute events in the following sequence:

1. Disable OUT1 (same sequence as when OE is used) and reset N counters.
2. When OUT1 is low, switch OUT1 to high-impedance state.
3. Disable MCLK, switch OUT0 to high impedance state.
4. Disable master oscillator.

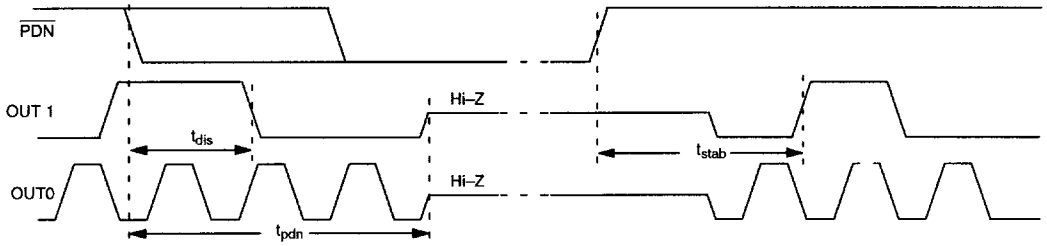
POWER-UP

When $\overline{\text{PDN}}$ is taken to a high level the following power-up sequence occurs:

1. Enable internal oscillator.
2. Set M and N to maximum values.
3. Wait approximately 256 cycles of MCLK for it to stabilize.
4. Reset M and N to programmed values.
5. Enable OUT0 (if enabled)
6. Enable OUT1.

Steps 2 through 4 exist to allow the oscillator to stabilize before enabling the outputs.

Figure 5

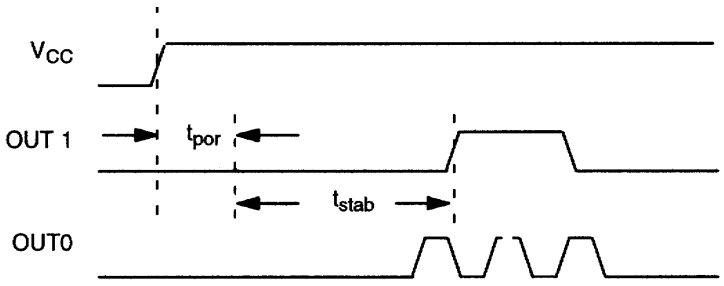


POWER-ON RESET

When power is initially applied to the device supply pin, a power-on reset sequence is executed, similar to that which occurs when the device is restored from a power-down condition. This sequence comprises two stages, first a conventional POR to initialize all on-chip circuitry, followed by a stabilization period to allow the oscillator to reach a stable frequency before enabling the outputs:

1. Initialize internal circuitry.
2. Enable internal oscillator.
3. Set M and N to maximum values.
4. Wait approximately 256 cycles of MCLK for the oscillator to stabilize.
5. Load M and N programmed values from EEPROM.
6. Enable OUT0 (if enabled).
7. Enable OUT1.

Figure 6



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	-1.0V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to +125°C
Soldering Temperature	See J-STD-020A Specification

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC ELECTRICAL CHARACTERISTICS

(T_A = 0°C to +70°C) (V_{CC} =2.7V to 3.6V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTE
Supply Voltage	V_{CC}		2.7		3.6	V	
High-level Output Voltage (OUT1, OUT0)	V_{OH}	I_{OH} = -2 mA, V_{CC} = MIN	2.4			V	
Low-level Output Voltage (OUT1, OUT0)	V_{OL}	I_{OL} = 2 mA			0.4	V	
High-level Input Voltage	V_{IH}		2			V	
Low-level Input Voltage	V_{IL}				0.8	V	
High-level Input Current ($\overline{PDN}$, OE)	I_{IH}	V_{IH} =2.4V,V_{CC} = 3.6V			1	uA	
Low-level Input Current ($\overline{PDN}$, OE)	I_{IL}	V_{IL}=0,V_{CC}=3.6V	-1			uA	
Supply Current (Active) DS1073-100 DS1073-80 DS1073-66 DS1073-60	I_{CC}	C_L = 15 pF (both outputs)		25	40	uA	
Standby Current (power-down)	I_{CCQ}	Power-Down Mode		0.8		uA	

AC ELECTRICAL CHARACTERISTICS

(T_A = 0°C to +70°C) (V_{CC} =2.7V to 3.6V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Output Frequency Accuracy	f_O	V_{CC} = 3.15V, T_A =25°C	-0.5	0	+0.5	%	
Combined Freq. Variation	Δf_O	Over temp and voltage	-1		+1	%	
Long Term Stability	Δf_O		-0.5		+0.5	%	
Minimum Output Frequency	f_{OUT}		29.3			kHz	1
Power-Up Time	$t_{POR}+t_{STAB}$			0.1	1	ms	2,3
Enable OUT1 from $\overline{PDN}$ ↑	t_{STAB}			0.1	1	ms	3
Enable OUT0 from $\overline{PDN}$ ↑	t_{STAB}			0.1	1	ms	3,4
OUT1 Hi-Z from $\overline{PDN}$ ↓	t_{PDN}				1	ms	
OUT0 Hi-Z from $\overline{PDN}$ ↓	t_{PDNd}				1	ms	
Load Capacitance (OUT1, OUT0)	C_L			15		pF	5
Output Duty Cycle OUT1 OUT0			 40 40		 60 60	 % %	
T Setup Enable MCLK	T_{SUEM}	MCLK=100 MHz			20	ns	
Jitter	J				100	pS	6

NOTES:

1. The values of M and N must be chosen so that this specification is met.

2. This is the time from when V_{CC} is applied until the output starts oscillating.

3. When the device is initially powered up, or restored from the power-down mode, OE should be asserted (high). Otherwise the start of the t_{stab} interval will be delayed until OE goes high. OE can subsequently be returned to a low level during the t_{stab} interval to force out low after the t_{stab}, interval. If the external mode is selected t_{stab} will be a function of the OSCIN period, i.e., external clock frequency. See "Calculated Parameters" to determine the value of t_{stab} in this case.

4. Although OE does not normally affect OUT0 operation, if OE is held low during power-up the start of the t_{stab} period will be delayed until OE is asserted. If OE remains low, OUT0 will not start.

5. Operation with higher capacitive loads is possible but may impair output voltage swing and maximum operation frequency.

6. Parameter given is a typical at 3 sigma.

AC ELECTRICAL CHARACTERISTICS – CALCULATED PARAMETERS

The following characteristics are derived from various device operating parameters (frequency, mode etc.). They are not specifically tested or guaranteed and may differ from the min and max limits shown by a small amount due to internal device setup times and propagation delays. However, the equations in the max column can be used to estimate a more accurate idea of typical device performance than the guaranteed values.

PARAMETER	SYMBOL	CONDITION	MIN	MAX
OUT1 ↑ from OE ↑	t_{EN}		t_M	$2t_M$
OUT1 ↓ from OE ↓ N = 1 N ≥ 2	t_{DIS} t_{DIS}		t_{OUTH} 0	$t_{OUTH} + t_M$ t_{OUTH}
$\overline{PDN}$ ↓ to OUT1 Hi-Z N = 1 N ≥ 2	t_{PDN} t_{PDN}		t_{OUTH} 0	$t_{OUTH} + t_M$ t_{OUTH}
$\overline{PDN}$ ↓ to OUT0 Hi-Z N = 1 N ≥ 2	t_{PDN} t_{PDN}		t_{OUTH} 0	$t_{OUTH} + t_M$ t_{OUTH}
$\overline{PDN}$ ↑ to OUT1 ↑	t_{STAB}			$256t_M$
$\overline{PDN}$ ↑ to OUT0 ↑	t_{STAB}			$256t_M$
OUT1 ↑ after Power-up				$256t_M$
OUT0 ↑ after Power-up				$256t_M$

DC ELECTRICAL CHARACTERISTICS

(TA = -40°C to +85°C) (Vcc =2.7V to 3.6V)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTE
Supply Voltage	V_{CC}		2.7		3.6	V	
High-level Output Voltage (OUT1, OUT0)	V_{OH}	I_{OH} = -2 mA, V_{CC} = MIN	2.4			V	
Low-level Output Voltage (OUT1, OUT0)	V_{OL}	I_{OL} = 2 mA			0.4	V	
High-level Input Voltage	V_{IH}		2			V	
Low-level Input Voltage	V_{IL}				0.8	V	
High-level Input Current ($\overline{PDN}$, OE)	I_{IH}	V_{IH} =2.4V,V_{CC} = 3.6V			1	uA	
Low-level Input Current($\overline{PDN}$,OE)	I_{IL}	V_{IL}=0,V_{CC}=3.6V	-1			uA	
Supply Current (Active) DS1073-100 DS1073-80 DS1073-66 DS1073-60	I_{CC}	C_L = 15 pF (both outputs)		25	50	mA	
Standby Current (power-down)	I_{CCQ}	Power-Down Mode		0.8		uA	

AC ELECTRICAL CHARACTERISTICS

(T_A = -40°C to +85°C) (V_{CC} =3.15V ± 10%)

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Output Frequency Accuracy	f_O	V_{CC} = 3.15V, T_A =25°C	-0.5	0	+0.5	%	
Combined Freq. Variation	Δf_O	Over temp and voltage	-2.5%		2.5%	%	
Long Term Stability	Δf_O		-0.5		+0.5	%	
Minimum Output Frequency	f_{OUT}		29.3			kHz	1
Power-Up Time	$t_{POR}+t_{STAB}$			0.1	1	ms	2.3
Enable OUT from $\overline{PDN}$ ↑	t_{STAB}			0.1	1	ms	3
Enable OUT0 from $\overline{PDN}$ ↑	t_{STAB}			0.1	1	ms	3,4
OUT Hi-Z from $\overline{PDN}$ ↓	t_{PDN}				1	ms	
OUT0 Hi-Z from $\overline{PDN}$ ↓	t_{PDN}				1	ms	
Load Capacitance (IN/OUT, OUT0)	C_L			15		pF	5
Output Duty Cycle IN/OUT OUT0			 40 40		 60 60	 % %	
T Setup Enable Master	T_{SUEM}	MCLK=100 MHz			20	ns	
Jitter	J				100	pS	6

NOTES:

1. The values of M and N must be chosen so that this specification is met.

2. This is the time from when V_{CC} is applied until the output starts oscillating.

3. When the device is initially powered up or restored from the power-down mode, OE should be asserted (high). Otherwise the start of the t_{STAB} interval will be delayed until OE goes high. OE can subsequently be returned to a low level during the t_{STAB} interval to force out low after the t_{STAB} interval. If the external mode is selected, t_{STAB} will be a function of the OSCIN period, i.e. external clock frequency. See "Calculated Parameters" to determine the value of t_{STAB} in this case.

4. Although OE does not normally affect OUT0 operation, if OE is held low during power-up, the start of the t_{STAB} period will be delayed until OE is asserted. If OE remains low, OUT0 will not start.

5. Operation with higher capacitive loads is possible but may impair output voltage swing and maximum operation frequency.

6. Parameter given is typical at 3 sigma.