DS21610
3.3V/5V Clock Rate Adapter

www.maxim-ic.com

GENERAL DESCRIPTION

The DS21610 is a multirate, low-jitter clock adapter that converts E-carrier and T-carrier clocks to multiple PDH carrier clock rates. Two clock outputs are available that are frequency-locked to the input clock. The clock outputs along with an 8kHz frame-sync output can be phase-aligned to a frame-sync input. The device is backward compatible with the LXP610 and operates from either a 3.3V or 5V supply. All modes of operation include a standard 8kHz output.

PIN CONFIGURATION

TOP VIEW

SO

FEATURES

- **Direct Replacement for LXP610SE**
- **Converts E-Carrier Clock Rates to T-Carrier Clock Rates**
- **Converts T-Carrier Clock Rates to E-Carrier Clock Rates**
- **3.3V or 5V Supply**
- **Low Jitter Output**
- **Multiple Output Clocks Synchronized to Input Clock**
- **8kHz Frequency-Locked Output for all Operation Modes**
- **No External Components Required**
- **16-Pin SO and 28-Pin PLCC**
- **Industrial Temperature Range: -40°C to +85°C**

ORDERING INFORMATION

PART	TEMP RANGE	PIN-PACKAGE
DS21610SN	-40°C to +85°C	16 SO
DS21610SN+	-40°C to +85°C	16 SO
DS21610QN	-40°C to +85°C	28 PLCC
DS21610QN+	-40°C to +85°C	28 PLCC

+ Denotes a lead-free/RoHS-compliant device.

Note: *Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click here: www.maxim-ic.com/errata.*

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1. PIN DESCRIPTION

Table 1-A. Pin Description

PIN		NAME	TYPE	FUNCTION
PLCC	SO			
1	1	P3	Input	Program Pin 3. Used to select the various combinations of clock and sync outputs.
2	2	SYNCOUT	Output	Synchronization Pulse Output. An 8kHz output that can be synchronized to the clock outputs and SYNCIN (if present).
3–5, 7–9, 11, 12, 17–19, 21, 23, 25, 26	3, 6, 11	N.C.	—	No Connection
6	4	CLKOUT2	Output	Clock Output 2. T1 or E1 carrier clock output referenced to CLKIN.
10	5	CLKIN	Input	Clock Input. Reference Clock Input. CLKOUT1 and CLKOUT2 will be referenced to this clock.
13	7	CLKOUT1	Output	Clock Output 1. T1 or E1 carrier clock output referenced to CLKIN.
14	8	P1	Input	Program Pin 3. Used to select the various combinations of clock and sync outputs.
15	9	V_{SS}	Supply	Ground
16	10	P2	Input	Program Pin 2. Used to select the various combinations of clock and sync outputs.
20	12	SEL	Input	Clock Mode Select. T-carrier/E-carrier mode select.
22	13	FSP	Input	Frame Synchronization Pulse Polarity. Used to change the polarity of the SYNCOUT output.
24	14	SYNCIN	Input	Synchronization Pulse Input. Used to synchronize the clock outputs and SYNCOUT to CLKIN and SYNCIN. SYNCIN should be tied high or low when not in use.
27	15	P4	Input	Program Pin 4. Used to select the various combinations of clock and sync outputs.
28	16	V_{DD}	Supply	Positive Supply, 3.3V or 5V ±5%

1.1 Compatibility with LXP610

The DS21610 is pin compatible with the LXP610.

Table 1-B. Pin Name Cross-Reference to LXP610

DS21610	LXP610	FUNCTION
P3	P3	Program Pin 3
SYNCOUT	FSO	Synchronization Pulse Output
CLKOUT2	HFO	Clock 2 Output
CLKIN	CLKI	Clock Input
CLKOUT1	CLKO	Clock 1 Output
P1	P1	Program pin 1
V_{SS}	GND	Ground
P2	P2	Program Pin 2
N.C.	N.C.	No Connection

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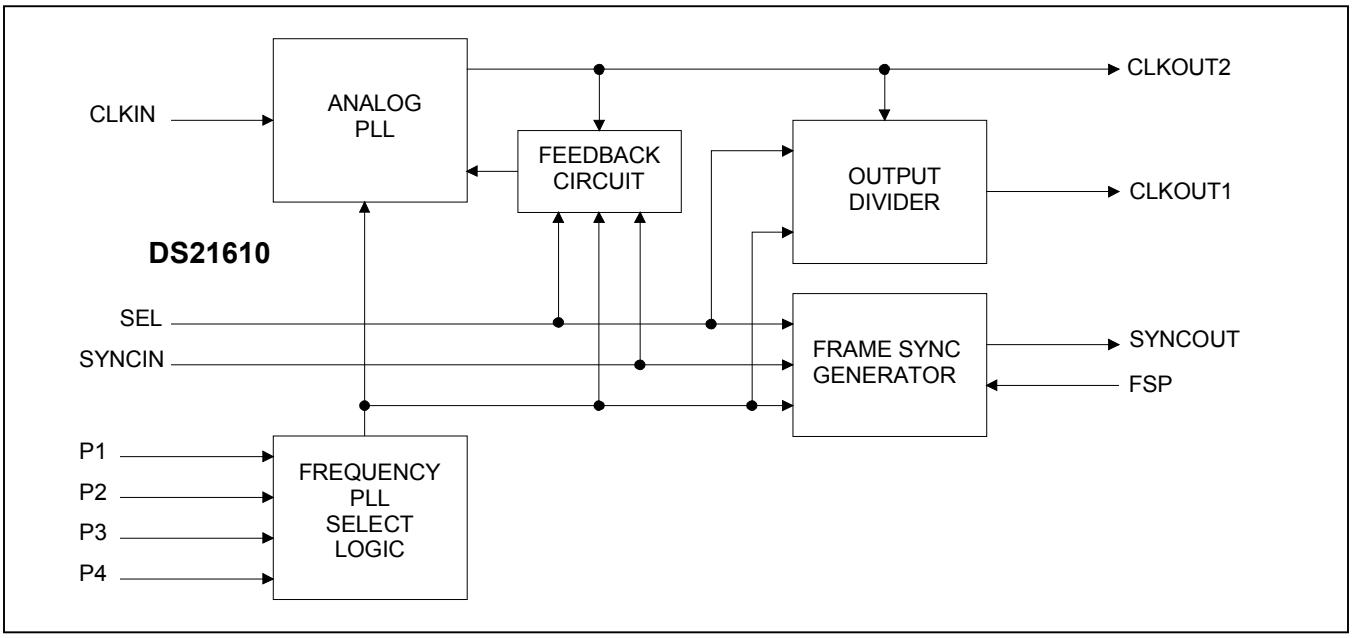
Figure 1-1. Block Diagram



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2. FUNCTIONAL DESCRIPTION

A clock input at CLKIN is converted to various clocks available on CLKOUT1 and CLKOUT2. Additionally, an 8kHz clock locked to CLKIN and SYNCIN (if present) is always available at the SYNCOUT pin. The pulse width of the SYNCOUT is selectable. It can be one or one-half the clock period of CLKIN, centered on the rising edge of CLKIN. Pins P1 to P4 are used to select the various clock rates and operational modes. Table 2-A and Table 2-B list the various operational modes of the DS21610.

CLKIN, CLKOUT1, and CLCKOUT2 are always frequency-locked. They can all be phase-locked to a system frame-sync pulse. A frame-sync pulse applied to SYNCIN will cause CLKIN and CLKOUT1 and CLKOUT2 to be phased-locked to that sync pulse. This causes the clocks to have a fixed alignment at the frame-sync boundaries. The signal applied to SYNCIN can be 8kHz or some integer subrate such as 1kHz, 2kHz, or 4kHz. Phase synchronization occurs within a maximum of 50ms when SYNCIN is 8kHz.

Table 2-A. Program Pin Functions (SEL = 0)

P4	P3	P2	P1	CLKIN	CLKOUT1	CLKOUT2	SYNCOUT
0	0	0	0	1.544	2.048	6.144	Long
0	0	0	1	3.088	2.048	8.192	Short
0	0	1	0	1.544	2.048	6.144	Long
0	0	1	1	1.544	2.048	8.192	Short
0	1	0	0	1.544	2.560	7.680	Long
0	1	0	1	6.176	4.096	8.192	Long
0	1	1	0	1.544	2.560	7.680	Long
0	1	1	1	6.176	2.048	8.192	Short
1	0	0	0	3.088	2.048	6.144	Long
1	0	0	1	3.088	4.096	8.192	Long
1	0	1	0	3.088	2.048	6.144	Long
1	0	1	1	1.544	4.096	8.192	Long
1	1	0	0	6.176	2.560	7.680	Long
1	1	0	1	6.176	4.096	8.192	Long
1	1	1	0	6.176	2.560	7.680	Long
1	1	1	1	6.176	4.096	8.192	Long

Table 2-B. Program Pin Functions (SEL = 1)

P4	P3	P2	P1	CLKIN	CLKOUT1	CLKOUT2	SYNCOUT
0	0	0	0	2.048	3.088	6.176	Long
0	0	0	1	2.048	3.088	6.176	Long
0	0	1	0	2.048	1.544	6.176	Long
0	0	1	1	2.048	1.544	6.176	Long
0	1	0	0	2.560	1.544	7.720	Long
0	1	0	1	8.192	3.088	6.176	Long
0	1	1	0	2.560	1.544	7.720	Long
0	1	1	1	8.192	1.544	6.176	Long
1	0	0	0	2.048	3.088	6.176	Long
1	0	0	1	4.096	3.088	6.176	Long
1	0	1	0	2.048	3.088	6.176	Long
1	0	1	1	4.096	1.544	6.176	Long
1	1	0	0	2.560	1.544	7.720	Long
1	1	0	1	8.192	3.088	6.176	Long
1	1	1	0	2.560	1.544	7.720	Long
1	1	1	1	8.192	1.544	6.176	Long

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3. OUTPUT JITTER

Table 3-A shows the output jitter specifications for 2.048MHz (or 4.096MHz) to 1.544MHz conversions (SEL = 1) and 1.544MHz to 2.048MHz (or 4.096MHz) conversions (SEL = 0).

Table 3-A. Output Jitter Specifications, CLKOUT1 = 1.544MHz

FREQUENCY BAND	TR62411 SPECIFICATION	TYP	MAX	UNITS
No bandlimiting	TR62411	0.010	0.020	UI_{P-P}
10Hz–40kHz	TR62411	0.005	0.010	UI_{P-P}
8kHz–40kHz	TR62411	0.006	0.012	UI_{P-P}

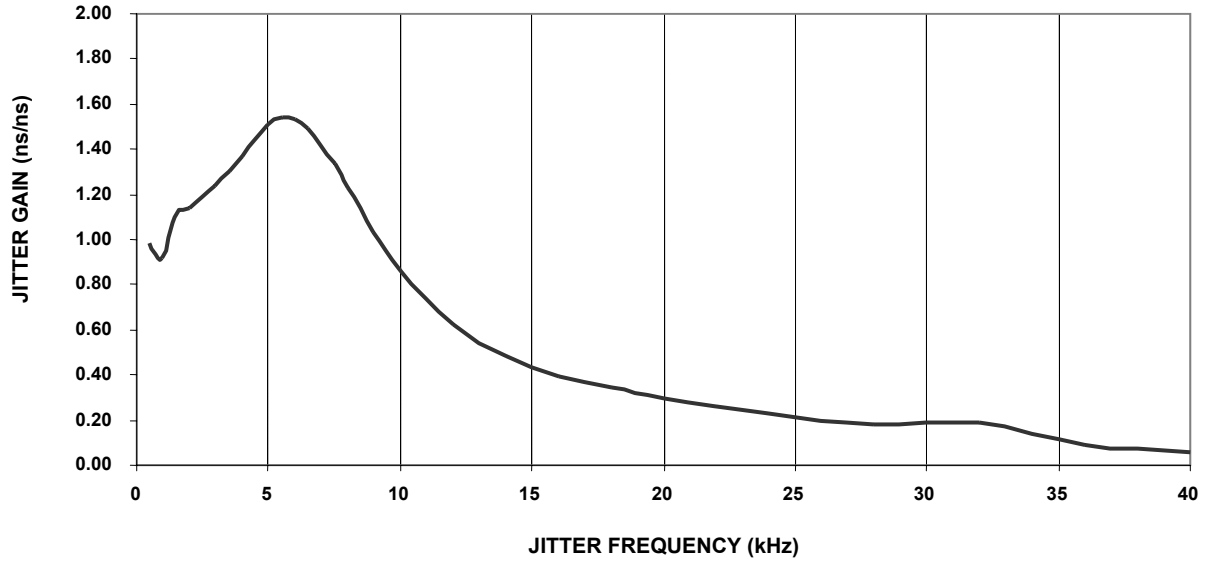
Table 3-B. Output Jitter Specifications, CLKOUT1 = 2.048MHz

FREQUENCY BAND	G.823 SPECIFICATION	TYP	MAX	UNITS
20Hz–100kHz	1.5	0.018	0.035	UI_{P-P}
18kHz–100kHz	0.2	0.012	0.025	UI_{P-P}

3.1 Jitter Transfer

Figure 3-1 and Figure 3-2 show jitter transfer for 2.048MHz-to-1.544MHz conversions and vice versa.

Figure 3-1. Nominal Jitter Transfer (1.544MHz CLKIN to 2.048MHz CLKOUT1)



NOTE: THE TYPICAL PEAK JITTER GAIN OF THE DS21610 IS ABOUT 1.6 FOR CONVERSION FROM T1 TO E1. THE TYPICAL PEAK-JITTER GAIN OF THE LEVEL ONE DEVICE IS ABOUT 1.1. HOWEVER, THE JITTER GAIN FOR THE DS21610 PEAKS IN THE 4kHz TO 8kHz RANGE, WHEREAS THE PEAK JITTER GAIN FOR THE LXP610 SPANS A GREATER FREQUENCY RANGE (20kHz TO 40kHz).

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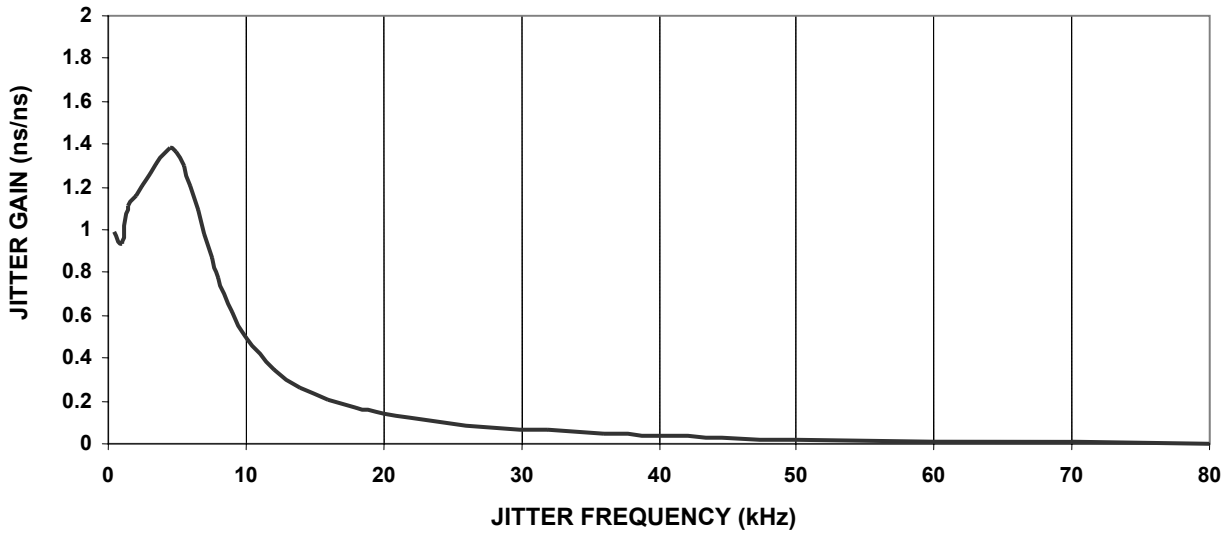
Figure 3-2. Nominal Jitter Transfer (2.048MHz CLKIN to 1.544MHz CLKOUT1)



NOTE: THE TYPICAL PEAK JITTER GAIN OF THE DS2161 IS ABOUT 1.4 FOR CONVERSION FROM T1 TO E1. THE TYPICAL PEAK-JITTER GAIN OF THE LEVEL ONE DEVICE IS ABOUT 1.1. HOWEVER, THE JITTER GAIN FOR THE DS21610 PEAKS IN THE 4kHz TO 8kHz RANGE, WHEREAS THE PEAK JITTER GAIN FOR THE LXP610 SPANS A GREATER FREQUENCY RANGE (20kHz TO 40kHz).

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4. OPERATING PARAMETERS

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground……..-1.0V to +6.0V
Operating Temperature Range for DS21610SN……...-40°C to +85°C
Storage Temperature……..-55°C to +125°C
Soldering Temperature……See IPC/JEDEC J-STD-020 Specification

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A = -40°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logic 1	V_{IH}	(Note 1)	2.0		5.5	V
Logic 0	V_{IL}	(Note 1)	-0.3		+0.8	V
Supply Voltage	V_{DD}	3.3V	3.135	3.3	3.465	V
		5V	4.75	5.0	5.25	

DC CHARACTERISTICS

(V_{DD} = 3.3V/5V ± 5%, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{DD}	(Note 2)			14	mA
Input Leakage	I_{IL}	(Note 3)	-10.0		+10.0	µA
Output Leakage	I_{LO}					µA
Output Current (2.4V)	I_{OH}		-1.0			mA
Output Current (0.4V)	I_{OL}		+4.0			mA

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AC TIMING

(Figure 4-1, Figure 4-2, Figure 4-3, Figure 4-4, and Figure 4-5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Capture Range on CLKIN		(Note 1)	±10,000			ppm
Lock Range on CLKIN		(Note 1)	±10,000			ppm
CLKIN Duty Cycle		(Note 1)	35		65	%
SYNCIN Setup to CLKIN Rising	t_{SU}	(Note 1)	46			ns
SYNCIN Hold After CLKIN Rising	t_{HI}	(Note 1)	30			ns
SYNCIN Pulse Width	t_{PW}	(Note 1)	76		CLKIN period	ns
CLKOUT1 Delay from CLKIN Rising	t_D	3.3V (Note 1)	-15	0	+41	ns
		5V (Note 1)	-15	0	+22	
CLKOUT1 Duty Cycle	C_D	(Note 1)		50		%
SYNCOUT Delay from CLKOUT2	t_{DF}	3.3V (Note 1)	-5		+30	ns
SYNCOUT Pulse Width	t_{SPW}	(Note 1)		CLKOUT1 period		ns
CLKOUT1 Delay from CLKOUT2 Rising	t_{DH}	3.3V (Note 1)	-15	0	+15	ns
Rise/Fall Time on CLKIN, SYNCIN	t_{RF}	3.3V (Note 1)			60	ns
		5V (Note 1)			40	
Rise/Fall Time on CLKOUT1, SYNCOUT, CLKOUT2 (Note 4)	t_{RF}	3.3V (Note 1)			75	ns
		5V (Note 1)			40	

Note 1: Guaranteed by design.
Note 2: 100pF load on all outputs.
Note 3: $0V < V_{IN} < V_{DD}$.
Note 4: 100pF load on CLKOUT1, SYNCOUT, CLKOUT2.

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Figure 4-1. SYNCIN/CLKIN to CLKOUT1/SYNCOUT and CLKOUT2

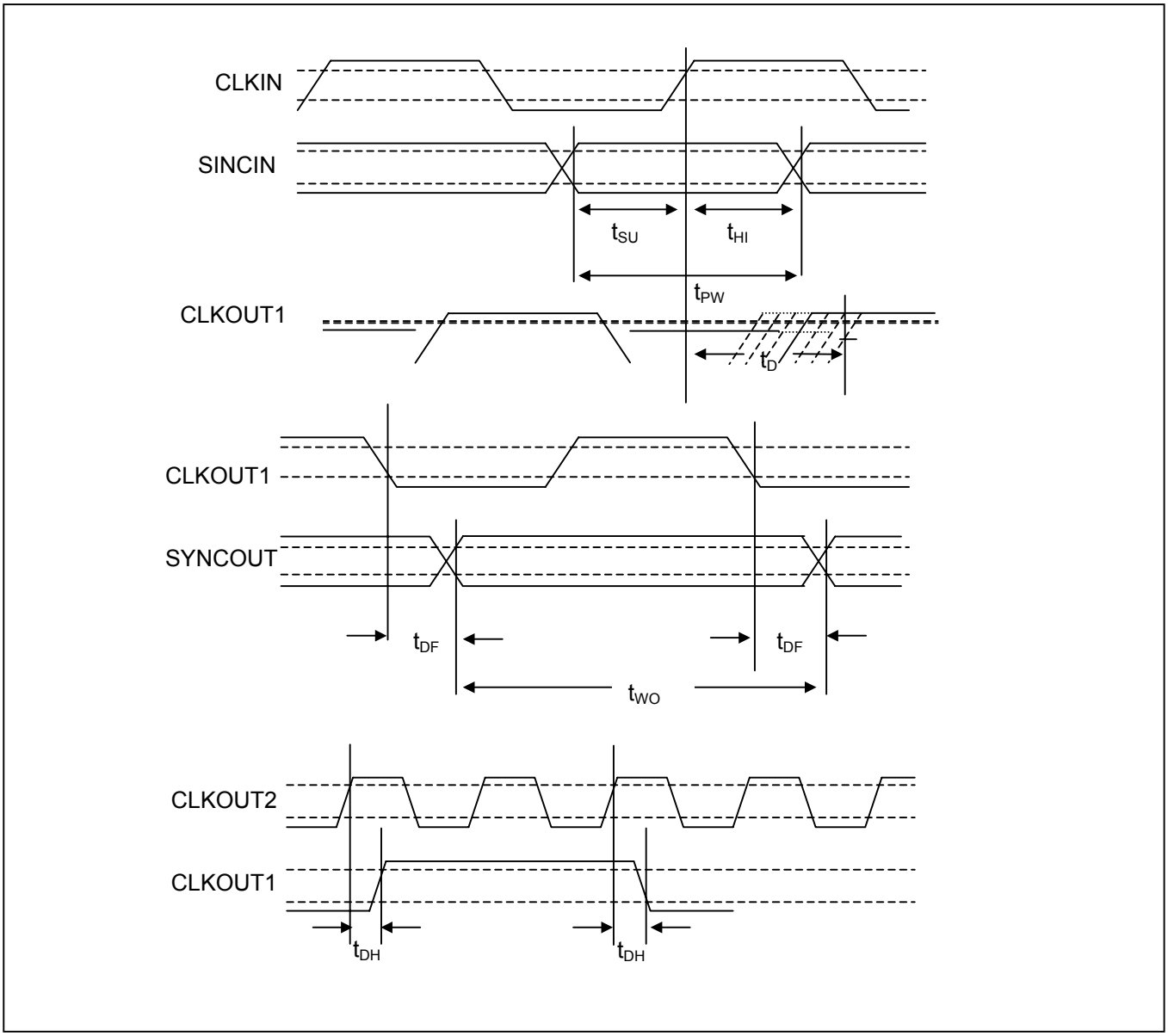

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Figure 4-2. Output Frame-Sync Alignment When CLKOIT2 = 2 x CLKOUT1

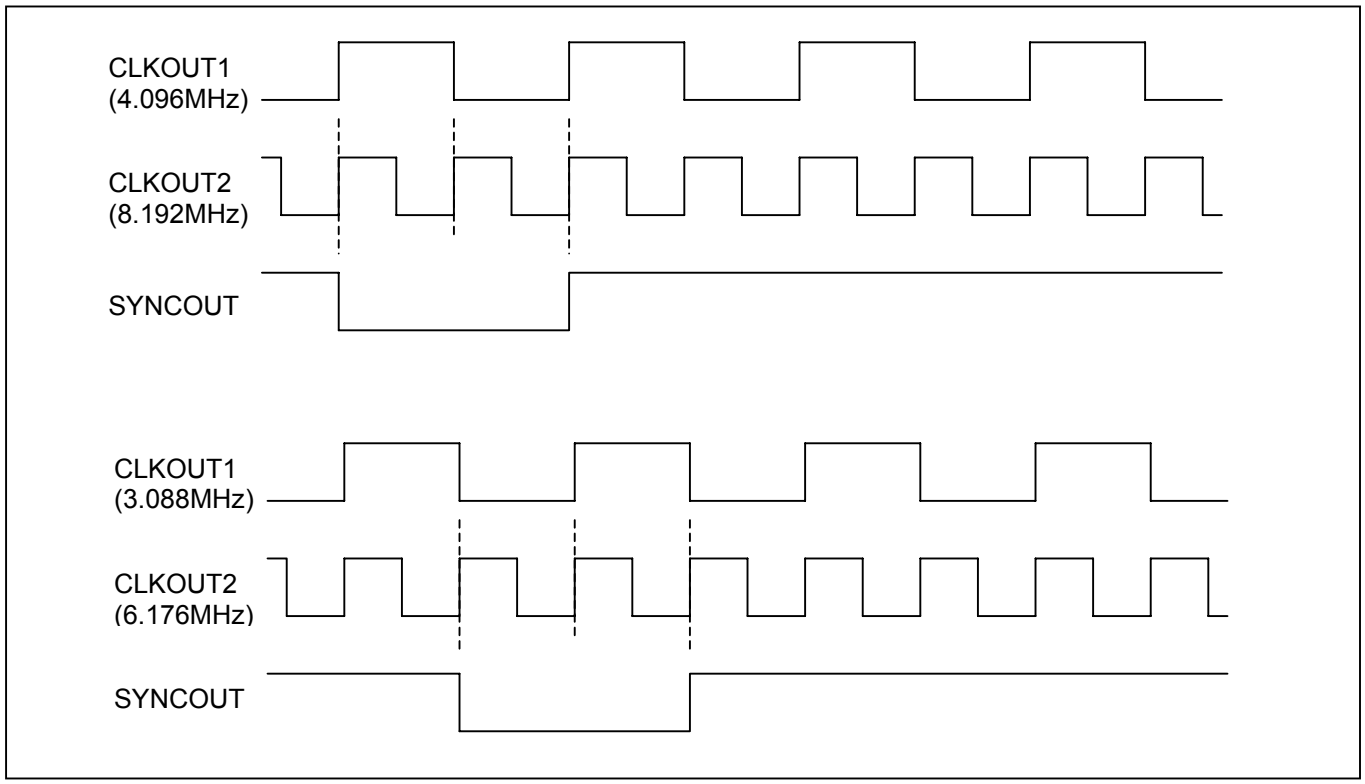

Figure 4-3. Output Frame-Sync Alignment When CLKOUT2 = 3 x CLKOUT1

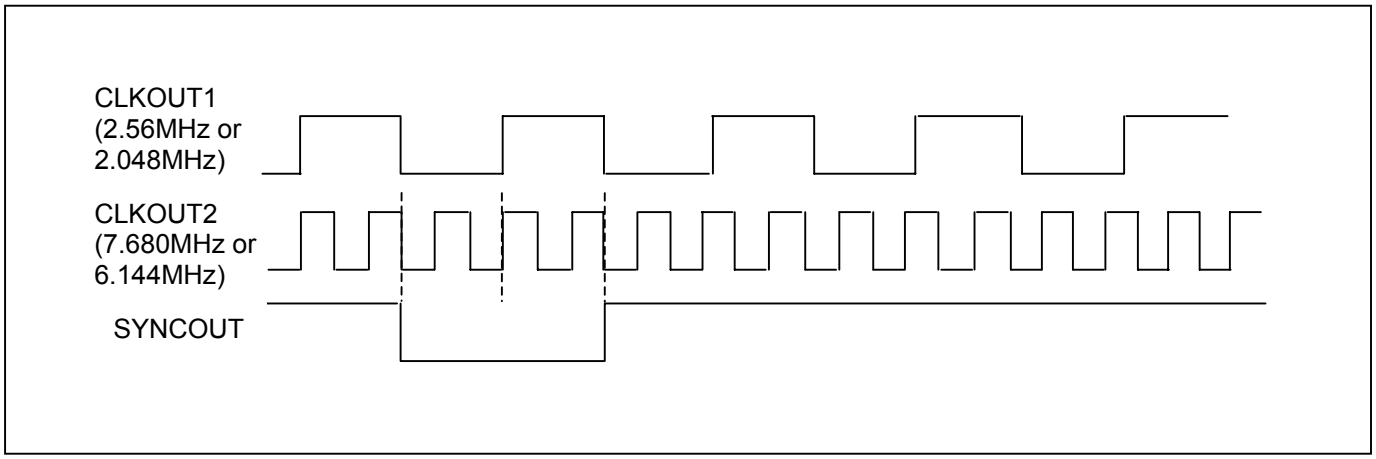

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Figure 4-4. Output Frame-Sync Alignment When CLKOIT2 = 4 x CLKOUT1

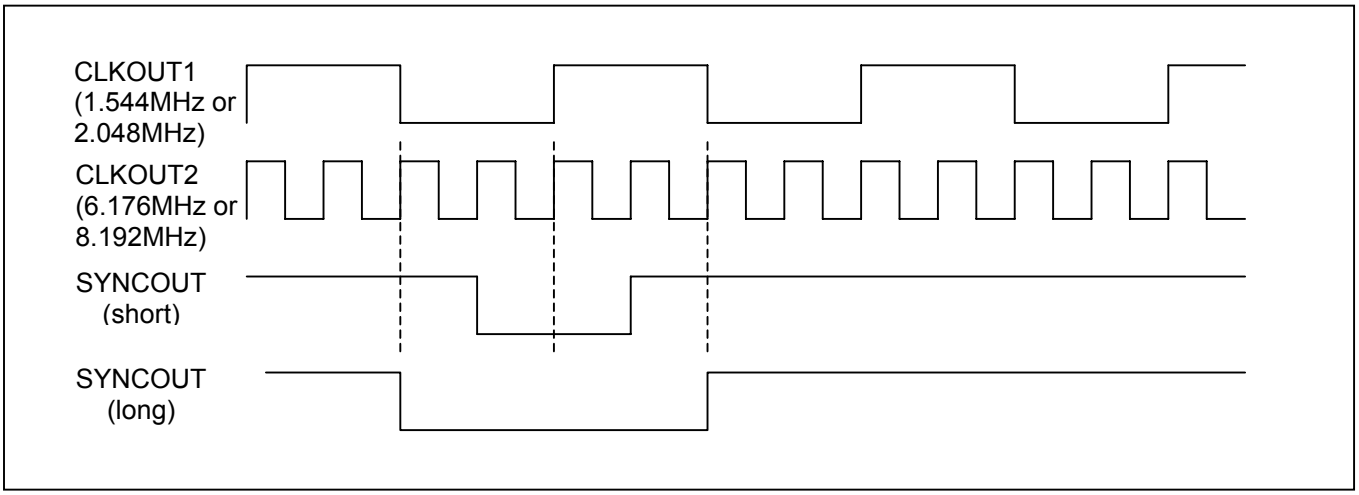
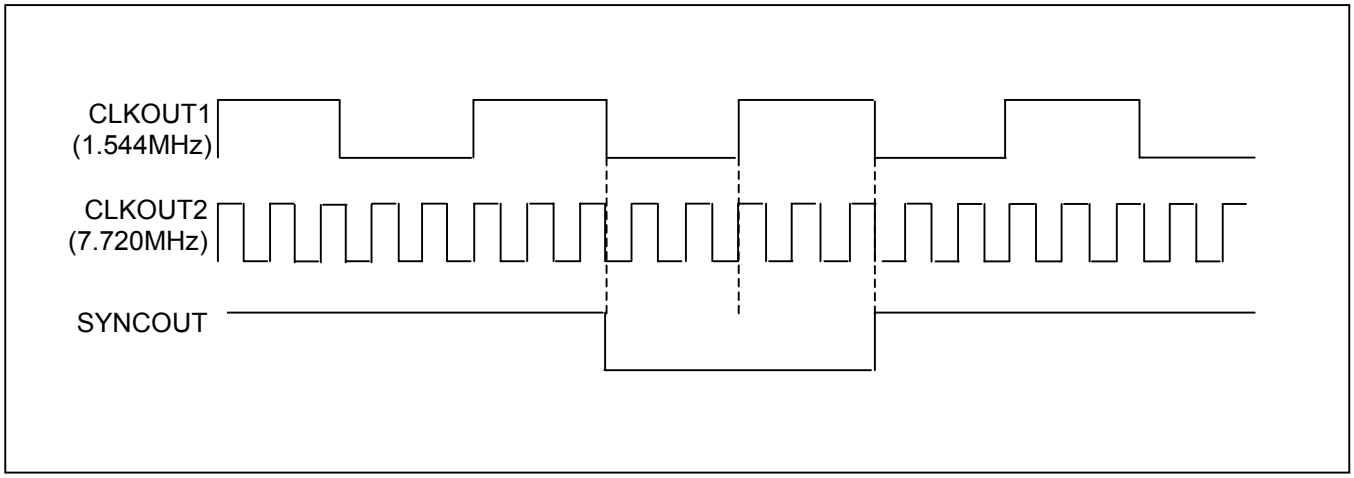


Figure 4-5. Output Frame-Sync Alignment When CLKOUT2 = 5 x CLKOUT1



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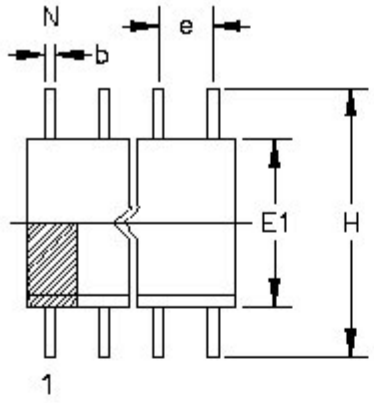
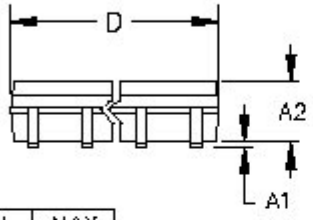
5. PACKAGE INFORMATION

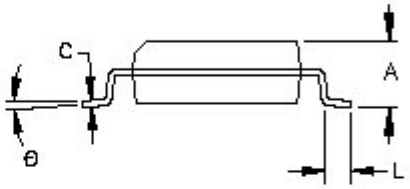
(The package drawing(s) in this data sheet may not reflect the most current specifications. The package number provided for each package is a link to the latest package outline information.)

5.1 16-Pin SO (300 mils) (56-G4009-001)

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	NEW DRAWING	5/18	J.W.
B	INC. ECN NO. 8680		







LTR		MIN	MAX
A	IN.	0.094	0.105
	MM	2.39	2.67
A1	IN.	0.004	0.012
	MM	0.102	0.30
A2	IN.	0.089	0.095
	MM	2.26	2.41
b	IN.	0.013	0.020
	MM	0.33	0.51
C	IN.	0.009	0.013
	MM	0.229	0.33
e	IN.	.050 BSC	
	MM	1.27 BSC	
E1	IN.	0.290	0.300
	MM	7.37	7.62
H	IN.	0.398	0.416
	MM	10.11	10.57
L	IN.	0.016	0.040
	MM	0.40	1.02
θ		0°	8°

	16 PIN		18 PIN		20 PIN		24 PIN		28 PIN	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
D IN.	0.398	0.412	0.448	0.462	0.498	0.511	0.598	0.612	0.698	0.712
MM	10.11	10.46	11.38	11.73	12.65	12.99	15.19	15.54	17.73	18.08

THE CHAMFER ON THE BODY IS OPTIONAL.
IF IT IS NOT PRESENT, A TERMINAL 1 IDENTIFIER
MUST BE POSITIONED SO THAT 1/2 OR MORE OF
IT'S AREA IS CONTAINED IN THE HATCHED ZONE.

SIGNATURE		DATE
DOC. CONTROL:	J.WILKINS	5/'94
ENGR. MGR:	B.W.MCARTY	5/94
MFG. ENGR:	C.M.SELLS	5/'94
CHECKED BY:	C.M.SELLS	5/'94
DRAWN BY:	M.W.C.	5/94

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE .300" SOIC 16,18,20,24&28 LD.

SIZE	FSCM NO	PART NO.	REV
A		56-G4009-001	B

DO NOT SCALE DWG. | SCALE N/A | SHEET 1 OF 1

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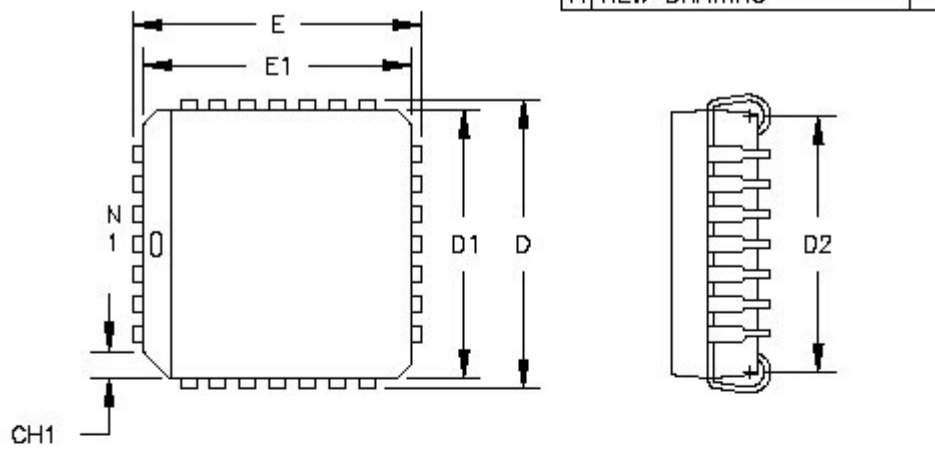
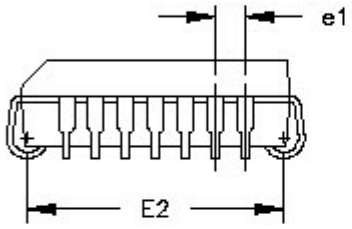
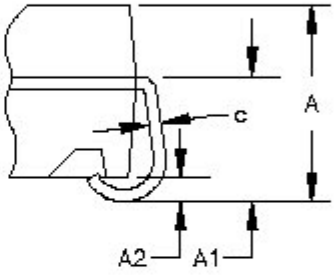
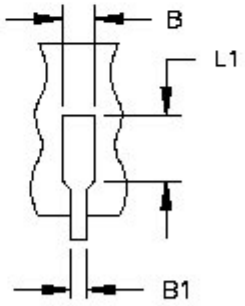
5.2 28-Pin PLCC (56-G4001-001)

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	NEW DRAWING		









LTR	MIN	MAX
A	.165	.180
A1	.090	.120
A2	.020	–
B	.026	.033
B1	.013	.021
c	.009	.012
D	.485	.495
D1	.450	.456
D2	.390	.430
E	.485	.495
E1	.450	.456
E2	.390	.430
L1	.060	–
N	28	–
e1	.050 BSC	
CH1	.042	.048

SIGNATURE		DATE
DOC. CONTROL:		
ENGR. MGR:		
MFG. ENGR:		
CHECKED BY:	B.W.M.	4/92
DRAWN BY:	M.W.C.	4/92
DO NOT SCALE DWG.		

DALLAS SEMICONDUCTOR MAXIM

TITLE: MARKETING OUTLINE, 28 PIN PLCC, SQUARE

SIZE	FSCM NO	PART NO.	REV
A		56-G4001-001	A

SCALE N/A SHEET 1 OF 1

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6. REVISION HISTORY

REVISION	DESCRIPTION
090100	Preliminary release.
112700	Remove references to 3V operation.
120600	Add FSP pin to block diagram.
021501	Add mechanical drawings for PLCC package.
060601	Added jitter specifications and pinout for all packages.
082001	Added timing diagrams.
032002	Updated jitter specifications.
032803	Added 3.3V operation specifications.
113004	Added soldering temperature to *Absolute Maximum Ratings* section.
112105	Changed timing specs in DC Characteristics and AC Timing tables to guaranteed by design.
011606	Added lead-free packages to Ordering Information on page 1.

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