Document Title

32Mbit / 16Mbit, Low Voltage, Serial Flash Memory With 100MHz Uniform 4KB Sectors

Revision History

Rev. No.	History	Issue Date	Remark
0.0	Initial issue	January 30, 2008	Preliminary

A25L032/A25L016 Series

32Mbit / 16Mbit Low Voltage, Serial Flash Memory

Preliminary — With 100MHz Uniform 4KB Sectors

FEATURES

- Family of Serial Flash Memories
  - A25L032: 32M-bit /4M-byte
  - A25L016: 16M-bit /2M-byte
- Flexible Sector Architecture with 4KB sectors
  - Sector Erase (4K-bytes) in 0.4s (typical)
  - Block Erase (64K-bytes) in 1s (typical)
- Page Program (up to 256 Bytes) in 3ms (typical)
- 2.7 to 3.6V Single Supply Voltage
- Dual input / output instructions resulting in an equivalent clock frequency of 200MHz:
  - Dual Output Fast Read Instruction
  - Dual Input and Output Fast Read Instruction
  - Dual Input Fast Program Instruction
- SPI Bus Compatible Serial Interface
- 100MHz Clock Rate (maximum)
- Deep Power-down Mode 1μA (typical)
- Additional 64-byte user-lockable, one-time programmable (OTP) area
- 32 Mbit / 16Mbit Flash memory
  - Uniform 4-Kbyte sectors
  - Uniform 64-Kbyte blocks
- Electronic Signatures
  - JEDEC Standard Two-Byte Signature
    A25L032: (3016h)
    A25L016: (3015h)
  - RES Instruction, One-Byte, Signature, for backward compatibility
    A25L032 (15h)
    A25L016 (14h)
- Package options
  - 8-pin SOP (209mil), 8-pin DIP (300mil) or 8-pin DFN8
  - All Pb-free (Lead-free) products are RoHS compliant

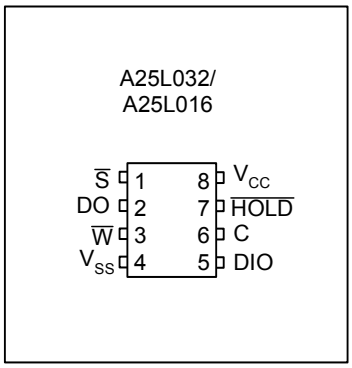
GENERAL DESCRIPTION

The A25L032/A25L016 are 32M/16M bit Serial Flash Memory, with advanced write protection mechanisms, accessed by a high speed SPI-compatible bus.

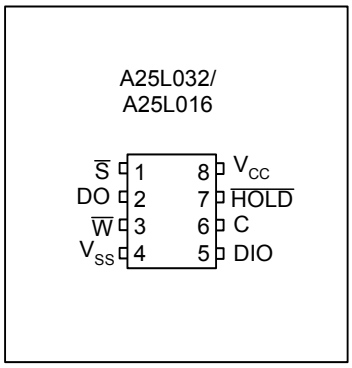
The memory can be programmed 1 to 256 bytes at a time, using the Page Program instruction.
The memory is organized as 64/32(A25L032/A25L016) blocks, each containing 16 sectors. Each sector is composed of 16 pages. Each page is 256 bytes wide. Thus, the whole memory can be viewed as consisting of 16,384/8,192 (A25L032/A25L016) pages, or 4,194,304/2,097,152 (A25L032/A25L016) bytes.
The whole memory can be erased using the Chip Erase instruction, a block at a time, using Block Erase instruction, or a sector at a time, using the Sector Erase instruction.

Pin Configurations

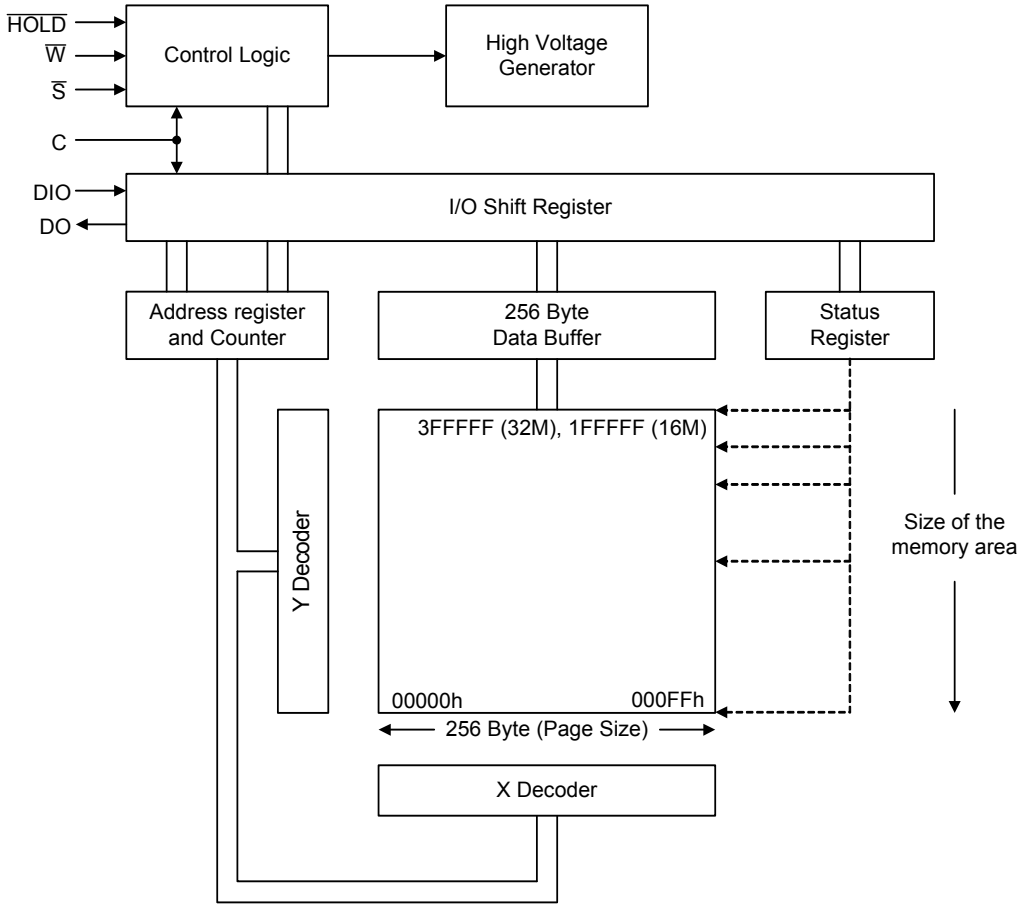
■ **SOP8 Connections**



■ **DIP8 Connections**



Block Diagram

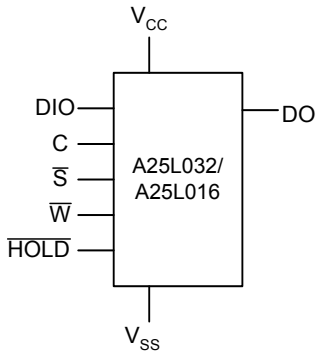


Pin Descriptions

Pin No.	Description
C	Serial Clock
DIO	Serial Data Input [1]
DO	Serial Data Output [2]
$\overline{S}$	Chip Select
$\overline{W}$	Write Protect
$\overline{HOLD}$	Hold
Vcc	Supply Voltage
Vss	Ground

Notes:
1. The DIO is also used as an output pin when the Fast Read Dual Output instruction and the Fast Read Dual Input-Output instruction are executed.
2. The DO is also used as an input pin when the Fast Read Dual Input-Output instruction and Dual Input Fast Program is executed.

Logic Symbol



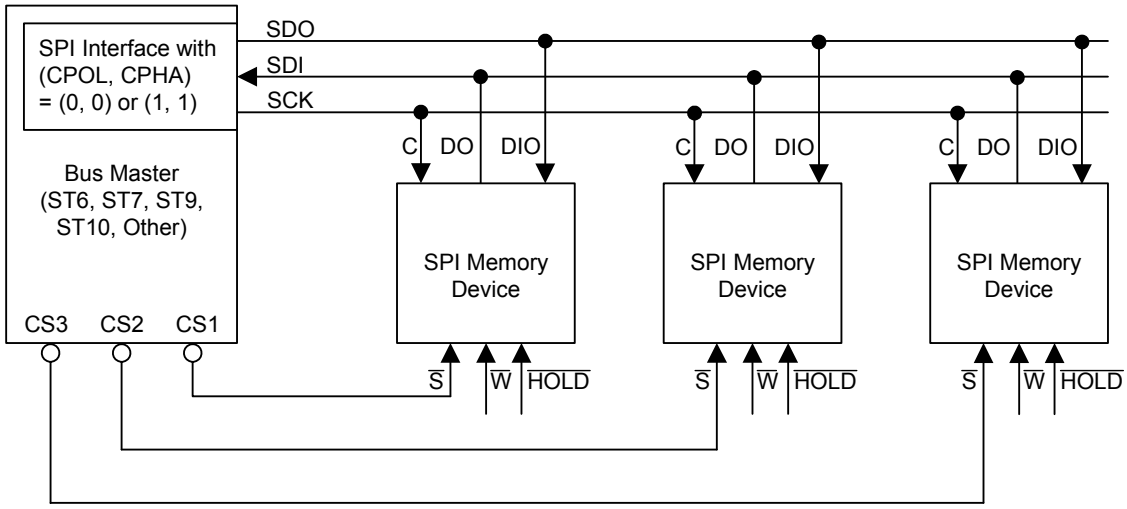
SIGNAL DESCRIPTION

Serial Data Output (DO). This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of Serial Clock (C).
The DO pin is also used as an input pin when the Fast Read Dual Input-Output instruction and Dual Input Fast Program is executed.
Serial Data Input (DIO). This input signal is used to transfer data serially into the device. It receives instructions, addresses, and the data to be programmed. Values are latched on the rising edge of Serial Clock (C).
The DIO pin is also used as an output pin when the Fast Read Dual Output instruction and the Fast Read Dual Input-Output instruction are executed.
Serial Clock (C). This input signal provides the timing of the serial interface. Instructions, addresses, or data present at Serial Data Input (DIO) are latched on the rising edge of Serial Clock (C). Data on Serial Data Output (DO) changes after the falling edge of Serial Clock (C).
Chip Select ($\overline{S}$). When this input signal is High, the device is deselected and Serial Data Output (DO) is at high impedance. Unless an internal Program, Erase or Write Status Register cycle is in progress, the device will be in the Standby mode (this is not the Deep Power-down mode). Driving Chip Select ($\overline{S}$) Low enables the device, placing it in the active power mode.
After Power-up, a falling edge on Chip Select ($\overline{S}$) is required prior to the start of any instruction.
Hold ($\overline{HOLD}$). The Hold ($\overline{HOLD}$) signal is used to pause any serial communications with the device without deselecting the device.
During the Hold condition, the Serial Data Output (DO) is high impedance, and Serial Data Input (DIO) and Serial Clock (C) are Don't Care. To start the Hold condition, the device must be selected, with Chip Select ($\overline{S}$) driven Low.
Write Protect ($\overline{W}$). The main purpose of this input signal is to freeze the size of the area of memory that is protected against program or erase instructions (as specified by the values in the BP2, BP1, and BP0 bits of the Status Register).

SPI MODES

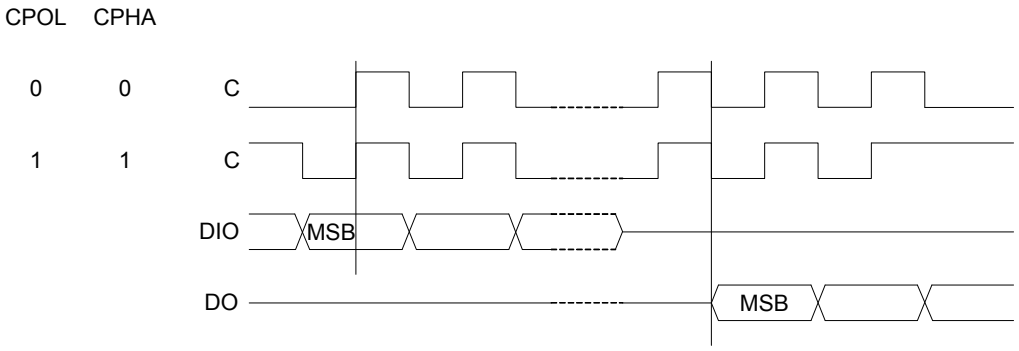
These devices can be driven by a microcontroller with its SPI peripheral running in either of the two following modes:
– CPOL=0, CPHA=0
– CPOL=1, CPHA=1
For these two modes, input data is latched in on the rising edge of Serial Clock (C), and output data is available from the falling edge of Serial Clock (C).
The difference between the two modes, as shown in Figure 2, is the clock polarity when the bus master is in Stand-by mode and not transferring data:
– C remains at 0 for (CPOL=0, CPHA=0)
– C remains at 1 for (CPOL=1, CPHA=1)

Figure 1. Bus Master and Memory Devices on the SPI Bus



Note: The Write Protect ($\overline{W}$) and Hold ($\overline{HOLD}$) signals should be driven, High or Low as appropriate.

Figure 2. SPI Modes Supported



OPERATING FEATURES

Page Programming

To program one data byte, two instructions are required: Write Enable (WREN), which is one byte, and a Page Program (PP) sequence, which consists of four bytes plus data. This is followed by the internal Program cycle (of duration t_{PP}).
To spread this overhead, the Page Program (PP) instruction allows up to 256 bytes to be programmed at a time (changing bits from 1 to 0), provided that they lie in consecutive addresses on the same page of memory.

Dual Input Fast Program

The Dual Input Fast Program (DIFP) instruction makes it possible to program up to 256 bytes using two input pins at the same time (by changing bits from 1 to 0).
For optimized timings, it is recommended to use the Dual Input Fast Program (DIFP) instruction to program all consecutive targeted bytes in a single sequence rather to using several Dual Input Fast Program (DIFP) sequences each containing only a few bytes.

Sector Erase, Block Erase, and Chip Erase

The Page Program (PP) instruction and Dual Input Fast Program (DIFP) instruction allow bits to be reset from 1 to 0. Before this can be applied, the bytes of memory need to have been erased to all 1s (FFh). This can be achieved, a sector at a time, using the Sector Erase (SE) instruction, a block at a time, using the Block Erase (BE) instruction, or throughout the entire memory, using the Chip Erase (CE) instruction. This starts an internal Erase cycle (of duration t_{SE}, t_{BE}, or t_{CE}).
The Erase instruction must be preceded by a Write Enable (WREN) instruction.

Polling During a Write, Program or Erase Cycle

A further improvement in the time to Write Status Register (WRSR), Program OTP (POTP), Program (PP), Dual Input Fast Program (DIFP) or Erase (SE, BE, or CE) can be achieved by not waiting for the worst case delay (t_W, t_{PP}, t_{SE}, t_{BE}, t_{CE}). The Write In Progress (WIP) bit is provided in the Status Register so that the application program can monitor its value, polling it to establish when the previous Write cycle, Program cycle or Erase cycle is complete.

Active Power, Stand-by Power and Deep Power-Down Modes

When Chip Select ($\overline{S}$) is Low, the device is enabled, and in the Active Power mode.

When Chip Select ($\overline{S}$) is High, the device is disabled, but could remain in the Active Power mode until all internal cycles have completed (Program, Erase, Write Status Register). The device then goes in to the Stand-by Power mode. The device consumption drops to I_{CC1}.
The Deep Power-down mode is entered when the specific instruction (the Deep Power-down Mode (DP) instruction) is executed. The device consumption drops further to I_{CC2}. The device remains in this mode until another specific instruction (the Release from Deep Power-down Mode and Read Electronic Signature (RES) instruction) is executed.
All other instructions are ignored while the device is in the Deep Power-down mode. This can be used as an extra software protection mechanism, when the device is not in active use, to protect the device from inadvertent Write, Program or Erase instructions.

Status Register

The Status Register contains a number of status and control bits that can be read or set (as appropriate) by specific instructions.
WIP bit. The Write In Progress (WIP) bit indicates whether the memory is busy with a Write Status Register, Program or Erase cycle.
WEL bit. The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch.
BP2, BP1, BP0 bits. The Block Protect (BP2, BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase instructions.
TB bit
The Top/Bottom (TB) bit is non-volatile. It is used in conjunction with Block Protect (BP0, BP1, BP2) bits to determine if the protected area defined by the Block Protect bits starts from the top or bottom of memory array.
SRWD bit. The Status Register Write Disable (SRWD) bit is operated in conjunction with the Write Protect ($\overline{W}$) signal. The Status Register Write Disable (SRWD) bit and Write Protect ($\overline{W}$) signal allow the device to be put in the Hardware Protected mode. In this mode, the non-volatile bits of the Status Register (SRWD, TB, BP2, BP1, BP0) become read-only bits.

Protection Modes

The environments where non-volatile memory devices are used can be very noisy. No SPI device can operate correctly in the presence of excessive noise. To help combat this, the A25L032/A25L016 boasts the following data protection mechanisms:

- Power-On Reset and an internal timer (t_{PUW}) can provide protection against inadvertant changes while the power supply is outside the operating specification.
- Program, Erase and Write Status Register instructions are checked that they consist of a number of clock pulses that is a multiple of eight, before they are accepted for execution.
- All instructions that modify data must be preceded by a Write Enable (WREN) instruction to set the Write Enable Latch (WEL) bit. This bit is returned to its reset state by the following events:
  - Power-up
  - Write Disable (WRDI) instruction completion
  - Write Status Register (WRSR) instruction completion
  - Program OTP (POTP) instruction completion
  - Page Program (PP) instruction completion
  - Dual Input Fast Program (DIFP) instruction completion
  - Sector Erase (SE) instruction completion
  - Block Erase (BE) instruction completion
  - Chip Erase (CE) instruction completion
- The Block Protect (BP2, BP1, BP0) bits allow part of the memory to be configured as read-only. This is the Software Protected Mode (SPM).
- The Write Protect ($\overline{W}$) signal allows the Block Protect (BP2, BP1, BP0) bits and Status Register Write Disable (SRWD) bit to be protected. This is the Hardware Protected Mode (HPM).
- In addition to the low power consumption feature, the Deep Power-down mode offers extra software protection

from inadvertant Write, Program and Erase instructions, as all instructions are ignored except one particular instruction (the Release from Deep Power-down instruction).

Table 1. Protected Area Sizes

A25L032

Status Register Content				(32M-Bit) Memory Protection			
TB	BP2	BP1	BP0	Block(s)	Addresses	Density	Portion
X	0	0	0	None	None	None	None
0	0	0	1	63	3F0000h – 3FFFFFh	64KB	Upper 1/64
0	0	1	0	62 – 63	3E0000h – 3FFFFFh	128KB	Upper 1/32
0	0	1	1	60 – 63	3C0000h – 3FFFFFh	256KB	Upper 1/16
0	1	0	0	56 – 63	380000h – 3FFFFFh	512KB	Upper 1/8
0	1	0	1	48 – 63	300000h – 3FFFFFh	1MB	Upper 1/4
0	1	1	0	32 – 63	200000h – 3FFFFFh	2MB	Upper 1/2
1	0	0	1	0	000000h – 00FFFFh	64KB	Lower 1/64
1	0	1	0	0 – 1	000000h – 01FFFFh	128KB	Lower 1/32
1	0	1	1	0 – 3	000000h – 03FFFFh	256KB	Lower 1/16
1	1	0	0	0 – 7	000000h – 07FFFFh	512KB	Lower 1/8
1	1	0	1	0 – 15	000000h – 0FFFFFh	1MB	Lower 1/4
1	1	1	0	0 – 31	000000h – 1FFFFFh	2MB	Lower 1/2
X	1	1	1	0 – 63	000000h – 3FFFFFh	4MB	All

Note:

1. X = don't care
2. The device is ready to accept a Chip Erase instruction if, and only if, all Block Protect (BP2, BP1, BP0) are 0.

A25L016

Status Register Content				(16M-Bit) Memory Protection			
TB	BP2	BP1	BP0	Block(s)	Addresses	Density	Portion
X	0	0	0	None	None	None	None
0	0	0	1	31	1F0000h – 1FFFFFh	64KB	Upper 1/32
0	0	1	0	30 – 31	1E0000h – 1FFFFFh	128KB	Upper 1/16
0	0	1	1	28 – 31	1C0000h – 1FFFFFh	256KB	Upper 1/8
0	1	0	0	24 – 31	180000h – 1FFFFFh	512KB	Upper 1/4
0	1	0	1	16 – 31	100000h – 1FFFFFh	1MB	Upper 1/2
1	0	0	1	0	000000h – 00FFFFh	64KB	Upper 1/32
1	0	1	0	0 – 1	000000h – 01FFFFh	128KB	Lower 1/16
1	0	1	1	0 – 3	000000h – 03FFFFh	256KB	Lower 1/8
1	1	0	0	0 – 7	000000h – 07FFFFh	512KB	Lower 1/4
1	1	0	1	0 – 15	000000h – 0FFFFFh	1MB	Lower 1/2
X	1	1	X	0 – 31	000000h – 1FFFFFh	2MB	All

Note:

1. X = don't care
2. The device is ready to accept a Chip Erase instruction if, and only if, all Block Protect (BP2, BP1, BP0) are 0.

Hold Condition

The Hold ($\overline{HOLD}$) signal is used to pause any serial communications with the device without resetting the clocking sequence. However, taking this signal Low does not terminate any Write Status Register, Program or Erase cycle that is currently in progress.

To enter the Hold condition, the device must be selected, with Chip Select ($\overline{S}$) Low.

The Hold condition starts on the falling edge of the Hold ($\overline{HOLD}$) signal, provided that this coincides with Serial Clock (C) being Low (as shown in Figure 3.).

The Hold condition ends on the rising edge of the Hold ($\overline{HOLD}$) signal, provided that this coincides with Serial Clock (C) being Low.

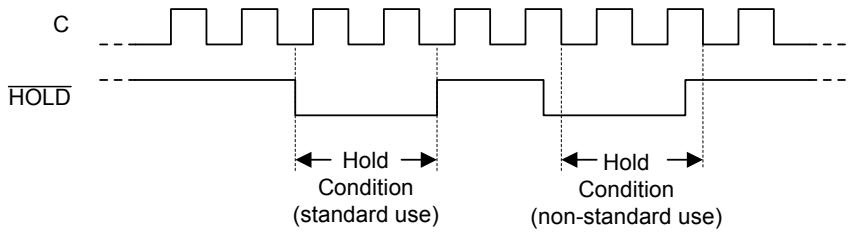
If the falling edge does not coincide with Serial Clock (C) being Low, the Hold condition starts after Serial Clock (C) next goes Low. Similarly, if the rising edge does not coincide with Serial Clock (C) being Low, the Hold condition ends after Serial Clock (C) next goes Low. This is shown in Figure 3.

During the Hold condition, the Serial Data Output (DO) is high impedance, and Serial Data Input (DIO) and Serial Clock (C) are Don't Care.

Normally, the device is kept selected, with Chip Select ($\overline{S}$) driven Low, for the whole duration of the Hold condition. This is to ensure that the state of the internal logic remains unchanged from the moment of entering the Hold condition.

If Chip Select ($\overline{S}$) goes High while the device is in the Hold condition, this has the effect of resetting the internal logic of the device. To restart communication with the device, it is necessary to drive Hold ($\overline{HOLD}$) High, and then to drive Chip Select ($\overline{S}$) Low. This prevents the device from going back to the Hold condition.

Figure 3. Hold Condition Activation



A25L032 MEMORY ORGANIZATION

The memory is organized as:
- 4,194,304 bytes (8 bits each)
- 64 blocks (64 Kbytes each)
- 1024 sectors (4 Kbytes each)
- 16,384 pages (256 bytes each)
- 64 OTP bytes located outside the main memory array

Each page can be individually programmed (bits are programmed from 1 to 0). The device is Sector, Block, or Chip Erasable (bits are erased from 0 to 1) but not Page Erasable.

Table 2. Memory Organization

A25L032 Address Table

Block	Sector	Address range	
63	1023	3FF000h	3FFFFFh
	⋮	⋮	⋮
	1008	3F0000h	3F0FFFh
62	1007	3EF000h	3EFFFFh
	⋮	⋮	⋮
	992	3E0000h	3E0FFFh
61	991	3DF000h	3DFFFFh
	⋮	⋮	⋮
	976	3D0000h	3D0FFFh
60	975	3CF000h	3CFFFFh
	⋮	⋮	⋮
	960	3C0000h	3C0FFFh
59	959	3BF000h	3BFFFFh
	⋮	⋮	⋮
	944	3B0000h	3B0FFFh
58	943	3AF000g	3AFFFFh
	⋮	⋮	⋮
	928	3A0000h	3A0FFFh
57	927	39F000h	39FFFFh
	⋮	⋮	⋮
	912	390000h	390FFFh
56	911	38F000h	38FFFFh
	⋮	⋮	⋮
	896	380000h	380FFFh
55	895	37F000h	37FFFFh
	⋮	⋮	⋮
	880	370000h	370FFFh
54	879	36F000h	36FFFFh
	⋮	⋮	⋮
	864	360000h	360FFFh
53	863	35F000h	35FFFFh
	⋮	⋮	⋮
	848	350000h	350FFFh

Block	Sector	Address range	
52	847	34F000h	34FFFFh
	⋮	⋮	⋮
	832	340000h	340FFFh
51	831	33F000h	33FFFFh
	⋮	⋮	⋮
	816	330000h	330FFFh
50	815	32F000h	32FFFFh
	⋮	⋮	⋮
	800	320000h	320FFFh
49	799	31F000h	31FFFFh
	⋮	⋮	⋮
	784	310000h	310FFFh
48	783	30F000h	30FFFFh
	⋮	⋮	⋮
	768	300000h	300FFFh
47	767	2FF000h	2FFFFFh
	⋮	⋮	⋮
	752	2F0000h	2F0FFFh
46	751	2EF000h	2EFFFFh
	⋮	⋮	⋮
	736	2E0000h	2E0FFFh
45	735	2DF000h	2DFFFFh
	⋮	⋮	⋮
	720	2D0000h	2D0FFFh
44	719	2CF000h	2CFFFFh
	⋮	⋮	⋮
	704	2C0000h	2C0FFFh
43	703	2BF000h	2BFFFFh
	⋮	⋮	⋮
	688	2B0000h	2B0FFFh
42	687	2AF000h	2AFFFFh
	⋮	⋮	⋮
	672	2A0000h	2A0FFFh

Memory Organization (continued)

Block	Sector	Address range	
41	671	29F000h	29FFFFh
	⋮	⋮	⋮
	656	290000h	290FFFh
40	655	28F000h	28FFFFh
	⋮	⋮	⋮
	640	280000h	280FFFh
39	639	27F000h	27FFFFh
	⋮	⋮	⋮
	624	270000h	270FFFh
38	623	26F000h	26FFFFh
	⋮	⋮	⋮
	608	260000h	260FFFh
37	607	25F000h	25FFFFh
	⋮	⋮	⋮
	592	250000h	250FFFh
36	591	24F000h	24FFFFh
	⋮	⋮	⋮
	576	240000h	240FFFh
35	575	23F000h	23FFFFh
	⋮	⋮	⋮
	560	230000h	230FFFh
34	559	22F000h	22FFFFh
	⋮	⋮	⋮
	544	220000h	220FFFh
33	543	21F000h	21FFFFh
	⋮	⋮	⋮
	528	210000h	210FFFh
32	527	20F000h	20FFFFh
	⋮	⋮	⋮
	512	200000h	200FFFh
31	511	1FF000h	1FFFFFh
	⋮	⋮	⋮
	496	1F0000h	1F0FFFh

Block	Sector	Address range	
30	495	1EF000h	1EFFFFh
	⋮	⋮	⋮
	480	1E0000h	1E0FFFh
29	479	1DF000h	1DFFFFh
	⋮	⋮	⋮
	464	1D0000h	1D0FFFh
28	463	1CF000h	1CFFFFh
	⋮	⋮	⋮
	448	1C0000h	1C0FFFh
27	447	1BF000h	1BFFFFh
	⋮	⋮	⋮
	432	1B0000h	1B0FFFh
26	431	1AF000h	1AFFFFh
	⋮	⋮	⋮
	416	1A0000h	1A0FFFh
25	415	19F000h	19FFFFh
	⋮	⋮	⋮
	400	190000h	190FFFh
24	399	18F000h	18FFFFh
	⋮	⋮	⋮
	384	180000h	180FFFh
23	383	17F000h	17FFFFh
	⋮	⋮	⋮
	368	170000h	170FFFh
22	367	16F000h	16FFFFh
	⋮	⋮	⋮
	352	160000h	160FFFh
21	351	15F000h	15FFFFh
	⋮	⋮	⋮
	336	150000h	150FFFh
20	335	14F000h	14FFFFh
	⋮	⋮	⋮
	320	140000h	140FFFh

Memory Organization (continued)

Block	Sector	Address range	
41	671	29F000h	29FFFFh
	⋮	⋮	⋮
	656	290000h	290FFFh
40	655	28F000h	28FFFFh
	⋮	⋮	⋮
	640	280000h	280FFFh
39	639	27F000h	27FFFFh
	⋮	⋮	⋮
	624	270000h	270FFFh
38	623	26F000h	26FFFFh
	⋮	⋮	⋮
	608	260000h	260FFFh
37	607	25F000h	25FFFFh
	⋮	⋮	⋮
	592	250000h	250FFFh
36	591	24F000h	24FFFFh
	⋮	⋮	⋮
	576	240000h	240FFFh
35	575	23F000h	23FFFFh
	⋮	⋮	⋮
	560	230000h	230FFFh
34	559	22F000h	22FFFFh
	⋮	⋮	⋮
	544	220000h	220FFFh
33	543	21F000h	21FFFFh
	⋮	⋮	⋮
	528	210000h	210FFFh
32	527	20F000h	20FFFFh
	⋮	⋮	⋮
	512	200000h	200FFFh
31	511	1FF000h	1FFFFFh
	⋮	⋮	⋮
	496	1F0000h	1F0FFFh

Block	Sector	Address range	
30	495	1EF000h	1EFFFFh
	⋮	⋮	⋮
	480	1E0000h	1E0FFFh
29	479	1DF000h	1DFFFFh
	⋮	⋮	⋮
	464	1D0000h	1D0FFFh
28	463	1CF000h	1CFFFFh
	⋮	⋮	⋮
	448	1C0000h	1C0FFFh
27	447	1BF000h	1BFFFFh
	⋮	⋮	⋮
	432	1B0000h	1B0FFFh
26	431	1AF000h	1AFFFFh
	⋮	⋮	⋮
	416	1A0000h	1A0FFFh
25	415	19F000h	19FFFFh
	⋮	⋮	⋮
	400	190000h	190FFFh
24	399	18F000h	18FFFFh
	⋮	⋮	⋮
	384	180000h	180FFFh
23	383	17F000h	17FFFFh
	⋮	⋮	⋮
	368	170000h	170FFFh
22	367	16F000h	16FFFFh
	⋮	⋮	⋮
	352	160000h	160FFFh
21	351	15F000h	15FFFFh
	⋮	⋮	⋮
	336	150000h	150FFFh
20	335	14F000h	14FFFFh
	⋮	⋮	⋮
	320	140000h	140FFFh

Memory Organization (continued)

Block	Sector	Address range	
19	319	13F000h	13FFFFh
	⋮	⋮	⋮
	304	130000h	130FFFh
18	303	12F000h	12FFFFh
	⋮	⋮	⋮
	288	120000h	120FFFh
17	287	11F000h	11FFFFh
	⋮	⋮	⋮
	272	110000h	110FFFh
16	271	10F000h	10FFFFh
	⋮	⋮	⋮
	256	100000h	100FFFh
15	255	FF000h	FFFFFh
	⋮	⋮	⋮
	240	F0000h	F0FFFh
14	239	EF000h	EFFFFh
	⋮	⋮	⋮
	224	E0000h	E0FFFh
13	223	DF000h	DFFFFh
	⋮	⋮	⋮
	208	D0000h	D0FFFh
12	207	CF000h	CFFFFh
	⋮	⋮	⋮
	192	C0000h	C0FFFh
11	191	BF000h	BFFFFh
	⋮	⋮	⋮
	176	B0000h	B0FFFh
10	175	AF000h	AFFFFh
	⋮	⋮	⋮
	160	A0000h	A0FFFh
9	159	9F000h	9FFFFh
	⋮	⋮	⋮
	144	90000h	90FFFh

Block	Sector	Address range	
8	143	8F000h	8FFFFh
	⋮	⋮	⋮
	128	80000h	80FFFh
7	127	7F000h	7FFFFh
	⋮	⋮	⋮
	112	70000h	70FFFh
6	111	6F000h	6FFFFh
	⋮	⋮	⋮
	96	60000h	60FFFh
5	95	5F000h	5FFFFh
	⋮	⋮	⋮
	80	50000h	50FFFh
4	79	4F000h	4FFFFh
	⋮	⋮	⋮
	64	40000h	40FFFh
3	63	3F000h	3FFFFh
	⋮	⋮	⋮
	48	30000h	30FFFh
2	47	2F000h	2FFFFh
	⋮	⋮	⋮
	32	20000h	20FFFh
1	31	1F000h	1FFFFh
	⋮	⋮	⋮
	16	10000h	10FFFh
0	15	0F000h	0FFFFh
	⋮	⋮	⋮
	4	04000h	04FFFh
	3	03000h	03FFFh
	2	02000h	02FFFh
	1	01000h	01FFFh
	0	00000h	00FFFh

A25L016 MEMORY ORGANIZATION

The memory is organized as:
- 2,097,152 bytes (8 bits each)
- 32 blocks (64 Kbytes each)
- 512 sectors (4 Kbytes each)
- 8192 pages (256 bytes each)
- 64 OTP bytes located outside the main memory array

Each page can be individually programmed (bits are programmed from 1 to 0). The device is Sector, Block, or Chip Erasable (bits are erased from 0 to 1) but not Page Erasable.

Table 3. Memory Organization

A25L016 Address Table

Block	Sector	Address range	
31	511	1FF000h	1FFFFFh
	⋮	⋮	⋮
	496	1F0000h	1F0FFFh
30	495	1EF000h	1EFFFFh
	⋮	⋮	⋮
	480	1E0000h	1E0FFFh
29	479	1DF000h	1DFFFFh
	⋮	⋮	⋮
	464	1D0000h	1D0FFFh
28	463	1CF000h	1CFFFFh
	⋮	⋮	⋮
	448	1C0000h	1C0FFFh
27	447	1BF000h	1BFFFFh
	⋮	⋮	⋮
	432	1B0000h	1B0FFFh
26	431	1AF000h	1AFFFFh
	⋮	⋮	⋮
	416	1A0000h	1A0FFFh
25	415	19F000h	19FFFFh
	⋮	⋮	⋮
	400	190000h	190FFFh
24	399	18F000h	18FFFFh
	⋮	⋮	⋮
	384	180000h	180FFFh
23	383	17F000h	17FFFFh
	⋮	⋮	⋮
	368	170000h	170FFFh
22	367	16F000h	16FFFFh
	⋮	⋮	⋮
	352	160000h	160FFFh
21	351	15F000h	15FFFFh
	⋮	⋮	⋮
	336	150000h	150FFFh
20	335	14F000h	14FFFFh
	⋮	⋮	⋮
	320	140000h	140FFFh
19	319	13F000h	13FFFFh
	⋮	⋮	⋮
	304	130000h	130FFFh
18	303	12F000h	12FFFFh
	⋮	⋮	⋮
	288	120000h	120FFFh
17	287	11F000h	11FFFFh
	⋮	⋮	⋮
	272	110000h	110FFFh
16	271	10F000h	10FFFFh
	⋮	⋮	⋮
	256	100000h	100FFFh
15	255	FF000h	FFFFFh
	⋮	⋮	⋮
	240	F0000h	F0FFFh
14	239	EF000h	EFFFFh
	⋮	⋮	⋮
	224	E0000h	E0FFFh
13	223	DF000h	DFFFFh
	⋮	⋮	⋮
	208	D0000h	D0FFFh
12	207	CF000h	CFFFFh
	⋮	⋮	⋮
	192	C0000h	C0FFFh
11	191	BF000h	BFFFFh
	⋮	⋮	⋮
	176	B0000h	B0FFFh
10	175	AF000h	AFFFFh
	⋮	⋮	⋮
	160	A0000h	A0FFFh

Memory Organization (continued)

Block	Sector	Address range	
9	159	9F000h	9FFFFh
	⋮	⋮	⋮
	144	90000h	90FFFh
8	143	8F000h	8FFFFh
	⋮	⋮	⋮
	128	80000h	80FFFh
7	127	7F000h	7FFFFh
	⋮	⋮	⋮
	112	70000h	70FFFh
6	111	6F000h	6FFFFh
	⋮	⋮	⋮
	96	60000h	60FFFh
5	95	5F000h	5FFFFh
	⋮	⋮	⋮
	80	50000h	50FFFh
4	79	4F000h	4FFFFh
	⋮	⋮	⋮
	64	40000h	40FFFh

Block	Sector	Address range	
3	63	3F000h	3FFFFh
	⋮	⋮	⋮
	48	30000h	30FFFh
2	47	2F000h	2FFFFh
	⋮	⋮	⋮
	32	20000h	20FFFh
1	31	1F000h	1FFFFh
	⋮	⋮	⋮
	16	10000h	10FFFh
0	15	0F000h	0FFFFh
	⋮	⋮	⋮
	4	04000h	04FFFh
	3	03000h	03FFFh
	2	02000h	02FFFh
	1	01000h	01FFFh
	0	00000h	00FFFh

INSTRUCTIONS

All instructions, addresses and data are shifted in and out of the device, most significant bit first.

Serial Data Input (DIO) is sampled on the first rising edge of Serial Clock (C) after Chip Select ($\overline{S}$) is driven Low. Then, the one-byte instruction code must be shifted in to the device, most significant bit first, on Serial Data Input (DIO), each bit being latched on the rising edges of Serial Clock (C).

The instruction set is listed in Table 4.

Every instruction sequence starts with a one-byte instruction code. Depending on the instruction, this might be followed by address bytes, or by data bytes, or by both or none.

In the case of a Read Data Bytes (READ), Read Data Bytes at Higher Speed (Fast_Read), Read OTP (ROTP), Read Identification (RDID), Read Electronic Manufacturer and Device Identification (REMS), Read Status Register (RDSR) or Release from Deep Power-down, Read Device Identification and Read Electronic Signature (RES) instruction, the shifted-in instruction sequence is followed by a data-out sequence. Chip Select ($\overline{S}$) can be driven High after any bit of the data-out sequence is being shifted out.

In the case of a Page Program (PP), Program OTP (POTP), Dual Input Fast Program (DIFP), Sector Erase (SE), Block Erase (BE), Chip Erase (CE), Write Status Register (WRSR), Write Enable (WREN), Write Disable (WRDI) or Deep Power-down (DP) instruction, Chip Select ($\overline{S}$) must be driven High exactly at a byte boundary, otherwise the instruction is rejected, and is not executed. That is, Chip Select ($\overline{S}$) must driven High when the number of clock pulses after Chip Select ($\overline{S}$) being driven Low is an exact multiple of eight.

All attempts to access the memory array during a Write Status Register cycle, Program cycle or Erase cycle are ignored, and the internal Write Status Register cycle, Program cycle or Erase cycle continues unaffected.

Table 4. Instruction Set

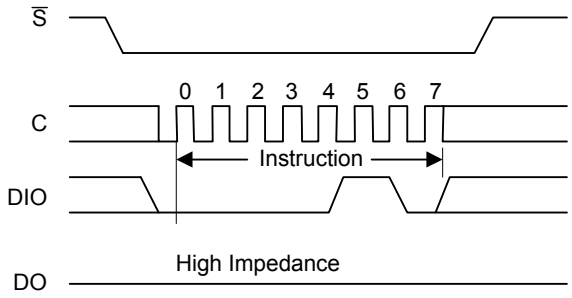
Instruction	Description	One-byte Instruction Code		Address Bytes	Dummy Bytes	Data Bytes
WREN	Write Enable	0000 0110	06h	0	0	0
WRDI	Write Disable	0000 0100	04h	0	0	0
RDSR	Read Status Register	0000 0101	05h	0	0	1 to ∞
WRSR	Write Status Register	0000 0001	01h	0	0	1
READ	Read Data Bytes	0000 0011	03h	3	0	1 to ∞
FAST_READ	Read Data Bytes at Higher Speed	0000 1011	0Bh	3	1	1 to ∞
ROTP	Read OTP (Read 64 bytes of OTP area)	0100 1011	4Bh	3	1	1 to ∞
POTP	Program OTP (Program 64 bytes of OTP area)	0100 0010	42h	3	0	1 to 64
DIFP	Dual Input Fast Program	1010 0010	A2h	3	0	1 to 256
FAST_READ_DUAL_OUTPUT	Read Data Bytes at Higher Speed by Dual Output (1)	00111011	3Bh	3	1	1 to ∞
FAST_READ_DUAL_INPUT-OUTPUT	Read Data Bytes at Higher Speed by Dual Input and Dual Output (1)	10111011	BBh	3(2)	1(2)	1 to ∞
PP	Page Program	0000 0010	02h	3	0	1 to 256
SE	Sector Erase	0010 0000	20h	3	0	0
BE	Block Erase	1101 1000	D8h	3	0	0
CE	Chip Erase	1100 0111	C7h	0	0	0
DP	Deep Power-down	1011 1001	B9h	0	0	0
RDID	Read Device Identification	1001 1111	9Fh	0	0	1 to ∞
REMS	Read Electronic Manufacturer & Device Identification	1001 0000	90h	1(3)	2	1 to ∞
RES	Release from Deep Power-down, and Read Electronic Signature	1010 1011	ABh	0	3	1 to ∞
	Release from Deep Power-down			0	0	0

Note: (1) DIO = (D_6, D_4, D_2, D_0)
DO = (D_7, D_5, D_3, D_1)
(2) Dual Input, DIO = (A22, A20, A18, ……, A6, A4, A2, A0)
DO = (A23, A21, A19, ……., A7, A5, A3, A1)
(3) ADD= (00h) will output manufacturer's ID first and ADD=(01h) will output device ID first

Write Enable (WREN)

The Write Enable (WREN) instruction (Figure 4.) sets the Write Enable Latch (WEL) bit.
The Write Enable Latch (WEL) bit must be set prior to every Page Program (PP), Dual Input Fast Program (DIFP), Program OTP (POTP), Sector Erase (SE), Block Erase (BE), Chip Erase (CE) and Write Status Register (WRSR) instruction.
The Write Enable (WREN) instruction is entered by driving Chip Select ($\overline{S}$) Low, sending the instruction code, and then driving Chip Select ($\overline{S}$) High.

Figure 4. Write Enable (WREN) Instruction Sequence

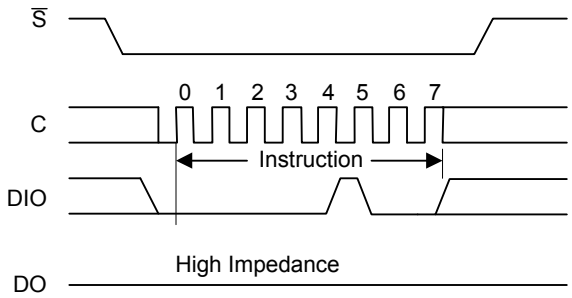


Write Disable (WRDI)

The Write Disable (WRDI) instruction (Figure 5.) resets the Write Enable Latch (WEL) bit.
The Write Disable (WRDI) instruction is entered by driving Chip Select ($\overline{S}$) Low, sending the instruction code, and then driving Chip The Write Enable Latch (WEL) bit is reset under the following conditions:

- Power-up
- Write Disable (WRDI) instruction completion
- Write Status Register (WRSR) instruction completion
- Page Program (PP) instruction completion
- Dual Input Fast Program (DIFP) instruction completion
- Program OTP (POTP) instruction completion
- Sector Erase (SE) instruction completion
- Block Erase (BE) instruction completion
- Chip Erase (CE) instruction completion

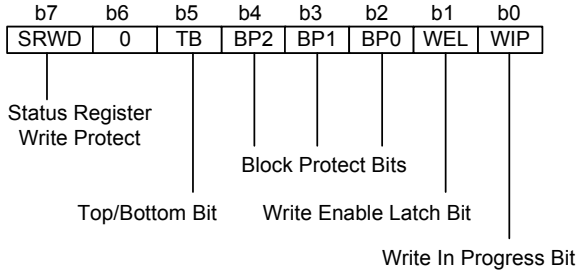
Figure 5. Write Disable (WRDI) Instruction Sequence



Read Status Register (RDSR)

The Read Status Register (RDSR) instruction allows the Status Register to be read. The Status Register may be read at any time, even while a Program, Erase or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write In Progress (WIP) bit before sending a new instruction to the device. It is also possible to read the Status Register continuously, as shown in Figure 6.

Table 5. Status Register Format



The status and control bits of the Status Register are as follows:

WIP bit. The Write In Progress (WIP) bit indicates whether the memory is busy with a Write Status Register, Program or Erase cycle. When set to 1, such a cycle is in progress, when reset to 0 no such cycle is in progress.

WEL bit. The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1 the internal Write Enable Latch is set, when set to 0 the internal Write Enable Latch is reset and no Write Status Register, Program or Erase instruction is accepted.

BP2, BP1, BP0 bits. The Block Protect (BP2, BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase instructions. These bits are written with the Write Status Register (WRSR) instruction. When one or more of the Block Protect (BP2, BP1, BP0) bits is set to 1, the relevant memory area (as defined in Table 1.) becomes protected against Page Program (PP), Sector Erase (SE), and Block Erase (BE) instructions. The Block Protect (BP2, BP1, BP0) bits can be written provided that the Hardware Protected mode has not been set. The Chip Erase (CE) instruction is executed if, and only if, all Block Protect (BP2, BP1, BP0) bits are 0.

TB bit

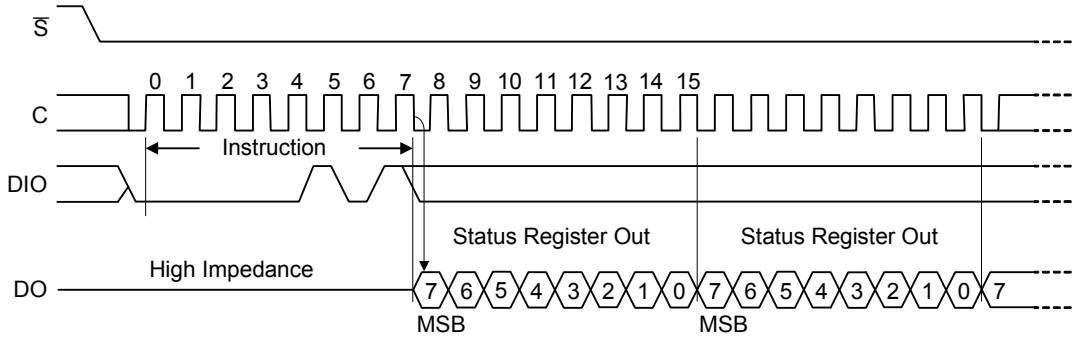
The Top/Bottom (TB) bit is non-volatile. It can be set and reset with the Write Status Register (WRSR) instruction provided that the Write Enable (WREN) instruction has been issued. The Top/Bottom (TB) bit is used in conjunction with the Block Protect (BP0, BP1,
BP2) bits to determine if the protected area defined by the Block Protect bits starts from the top or the bottom of the memory array:

- When TB is reset to '0' (default value), the area protected by the Block Protect bits starts from the top of the memory array (see Table 1: Protected area sizes)
- When TB is set to '1', the area protected by the Block Protect bits starts from the bottom of the memory array (see Table 1: Protected area sizes)

The TB bit cannot be written when the SRWD bit is set to '1' and the $\overline{W}$ pin is driven Low.

SRWD bit. The Status Register Write Disable (SRWD) bit is operated in conjunction with the Write Protect ($\overline{W}$) signal. The Status Register Write Disable (SRWD) bit and Write Protect ($\overline{W}$) signal allow the device to be put in the Hardware Protected mode (when the Status Register Write Disable (SRWD) bit is set to 1, and Write Protect ($\overline{W}$) is driven Low). In this mode, the non-volatile bits of the Status Register (SRWD, TB, BP2, BP1, BP0) become read-only bits and the Write Status Register (WRSR) instruction is no longer accepted for execution.

Figure 6. Read Status Register (RDSR) Instruction Sequence and Data-Out Sequence



Write Status Register (WRSR)

The Write Status Register (WRSR) instruction allows new values to be written to the Status Register. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded and executed, the device sets the Write Enable Latch (WEL).

The Write Status Register (WRSR) instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction code and the data byte on Serial Data Input (DIO).

The instruction sequence is shown in Figure 7. The Write Status Register (WRSR) instruction has no effect on b6, b5, b1 and b0 of the Status Register. b6 and b5 are always read as 0.

Chip Select ($\overline{S}$) must be driven High after the eighth bit of the data byte has been latched in. If not, the Write Status Register (WRSR) instruction is not executed. As soon as Chip Select ($\overline{S}$) is driven High, the self-timed Write Status Register cycle (whose duration is t_W) is initiated. While the Write Status Register cycle is in progress, the Status Register may still be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Write Status Register cycle, and is 0 when it is completed. When the cycle is completed, the Write Enable Latch (WEL) is reset.

The Write Status Register (WRSR) instruction allows the user to change the values of the Block Protect (BP2, BP1, BP0) bits, to define the size of the area that is to be treated as read-only, as defined in Table 1. The Write Status Register (WRSR) instruction also allows the user to set or reset the Status Register Write Disable (SRWD) bit in accordance with the Write Protect ($\overline{W}$) signal. The Status Register Write Disable (SRWD) bit and Write Protect ($\overline{W}$) signal allow the device to be put in the Hardware Protected Mode (HPM). The Write Status Register (WRSR) instruction is not executed once the Hardware Protected Mode (HPM) is entered.

Figure 7. Write Status Register (WRSR) Instruction Sequence

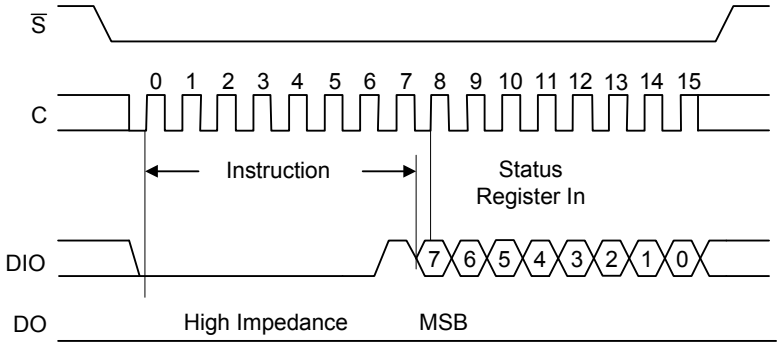


Table 6. Protection Modes

$\overline{W}$ Signal	SRWD Bit	Mode	Write Protection of the Status Register	Memory Content	
				Protected Area[1]	Unprotected Area[1]
1	0	Software Protected (SPM)	Status Register is Writable (if the WREN instruction has set the WEL bit) The values in the SRWD, TB, BP2, BP1, and BP0 bits can be changed	Protected against Page Program, Dual Input Fast Program, Sector Erase, Block Erase, and Chip Erase	Ready to accept Page Program, Dual Input Fast Program, Sector Erase, and Block Erase instructions
0	0				
1	1				
0	1	Hardware Protected (HPM)	Status Register is Hardware write protected The values in the SRWD, TB, BP2, BP1, and BP0 bits cannot be changed	Protected against Page Program, Dual Input Fast Program, Sector Erase, Block Erase, and Chip Erase	Ready to accept Page Program, Dual Input Fast Program, Sector Erase, and Block Erase instructions

Note: 1. As defined by the values in the Block Protect (TB, BP2, BP1, BP0) bits of the Status Register, as shown in Table 1.

The protection features of the device are summarized in Table 6.

When the Status Register Write Disable (SRWD) bit of the Status Register is 0 (its initial delivery state), it is possible to write to the Status Register provided that the Write Enable Latch (WEL) bit has previously been set by a Write Enable (WREN) instruction, regardless of the whether Write Protect ($\overline{W}$) is driven High or Low.

When the Status Register Write Disable (SRWD) bit of the Status Register is set to 1, two cases need to be considered, depending on the state of Write Protect ($\overline{W}$):

- If Write Protect ($\overline{W}$) is driven High, it is possible to write to the Status Register provided that the Write Enable Latch (WEL) bit has previously been set by a Write Enable (WREN) instruction.
- If Write Protect (W) is driven Low, it is *not* possible to write to the Status Register *even* if the Write Enable Latch (WEL) bit has previously been set by a Write Enable (WREN) instruction. (Attempts to write to the Status Register are rejected, and are not accepted for execution). As a consequence, all the data bytes in the memory area that are software protected (SPM) by the Block Protect (BP2, BP1, BP0) bits of the Status Register, are also hardware protected against data modification.

Regardless of the order of the two events, the Hardware Protected Mode (HPM) can be entered:

- by setting the Status Register Write Disable (SRWD) bit after driving Write Protect ($\overline{W}$) Low
- or by driving Write Protect ($\overline{W}$) Low after setting the Status Register Write Disable (SRWD) bit.

The only way to exit the Hardware Protected Mode (HPM) once entered is to pull Write Protect ($\overline{W}$) High.

If Write Protect ($\overline{W}$) is permanently tied High, the Hardware Protected Mode (HPM) can never be activated, and only the Software Protected Mode (SPM), using the Block Protect (BP2, BP1, BP0) bits of the Status Register, can be used.

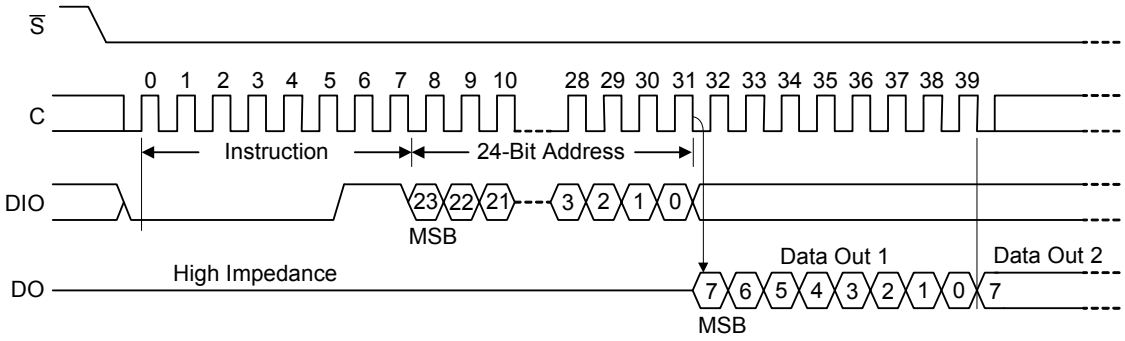
Read Data Bytes (READ)

The device is first selected by driving Chip Select ($\overline{S}$) Low. The instruction code for the Read Data Bytes (READ) instruction is followed by a 3-byte address (A23-A0), each bit being latched-in during the rising edge of Serial Clock (C). Then the memory contents, at that address, is shifted out on Serial Data Output (DO), each bit being shifted out, at a maximum frequency f_R, during the falling edge of Serial Clock (C).

The instruction sequence is shown in Figure 8. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes (READ) instruction. When the highest address is reached, the address counter rolls over to 000000h, allowing the read sequence to be continued indefinitely.

The Read Data Bytes (READ) instruction is terminated by driving Chip Select ($\overline{S}$) High. Chip Select ($\overline{S}$) can be driven High at any time during data output. Any Read Data Bytes (READ) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 8. Read Data Bytes (READ) Instruction Sequence and Data-Out Sequence



Note: Address bits A23 to A22 are Don't Care, for A25L032.
Address bits A23 to A21 are Don't Care, for A25L016.

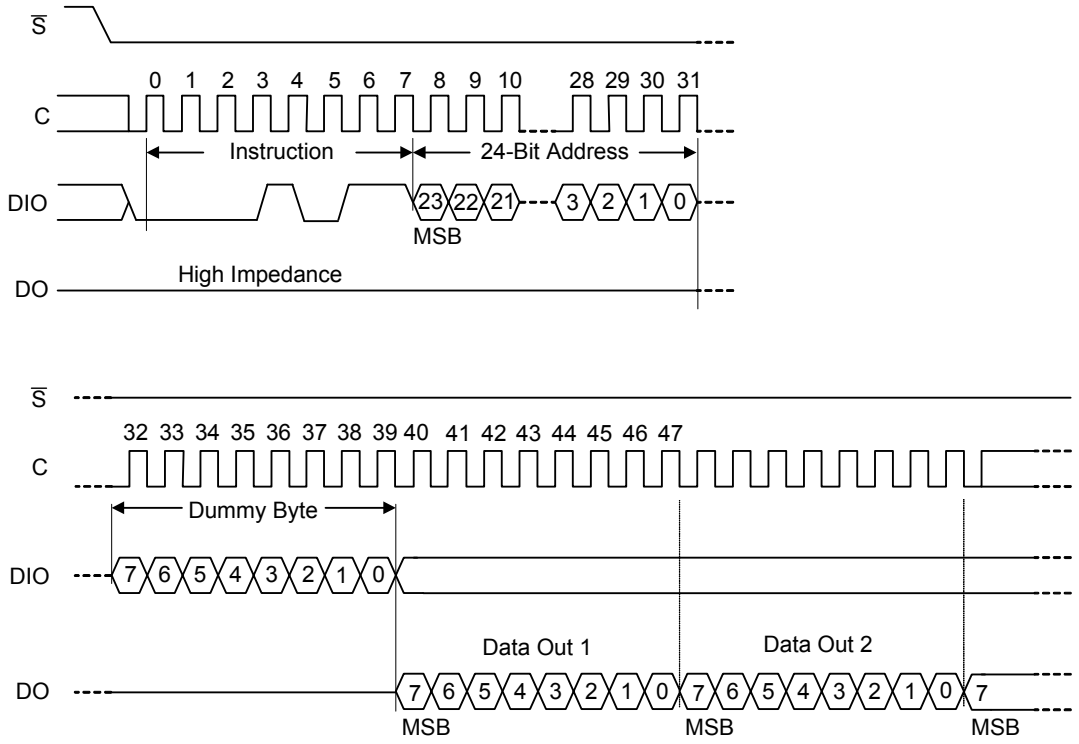
Read Data Bytes at Higher Speed (FAST_READ)

The device is first selected by driving Chip Select ($\overline{S}$) Low. The instruction code for the Read Data Bytes at Higher Speed (FAST_READ) instruction is followed by a 3-byte address (A23-A0) and a dummy byte, each bit being latched-in during the rising edge of Serial Clock (C). Then the memory contents, at that address, is shifted out on Serial Data Output (DO), each bit being shifted out, at a maximum frequency f_C, during the falling edge of Serial Clock (C).

The instruction sequence is shown in Figure 9. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes at Higher Speed (FAST_READ) instruction. When the highest address is reached, the address counter rolls over to 000000h, allowing the read sequence to be continued indefinitely.

The Read Data Bytes at Higher Speed (FAST_READ) instruction is terminated by driving Chip Select ($\overline{S}$) High. Chip Select ($\overline{S}$) can be driven High at any time during data output. Any Read Data Bytes at Higher Speed (FAST_READ) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 9. Read Data Bytes at Higher Speed (FAST_READ) Instruction Sequence and Data-Out Sequence



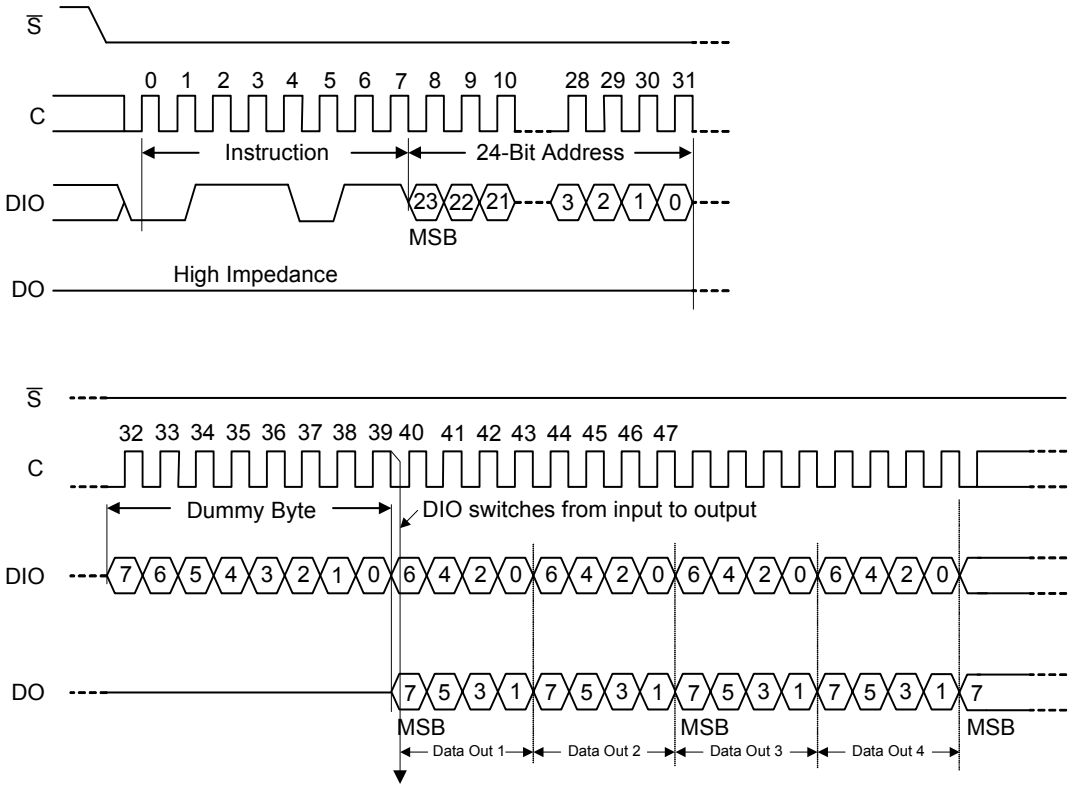
Note: Address bits A23 to A22 are Don't Care, for A25L032.
Address bits A23 to A21 are Don't Care, for A25L016.

Fast Read Dual Output (3Bh)

The Fast Read Dual Output (3Bh) instruction is similar to the Fast_Read (0Bh) instruction except the data is output on two pins, DO and DIO, instead of just DO. This allows data to be transferred from the A25L032/A25L016 at twice the rate of standard SPI devices.

Similar to the Fast Read instruction, the Fast Read Dual Output instruction can operate at the highest possible frequency of f_C (See AC Characteristics). This is accomplished by adding eight "dummy" clocks after the 24-bit address as shown in figure 10. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is "don't care". However, the DIO pin should be high-impedance prior to the falling edge of the first data out clock.

Figure 10. FAST_READ_DUAL_OUTPUT Instruction Sequence and Data-Out Sequence

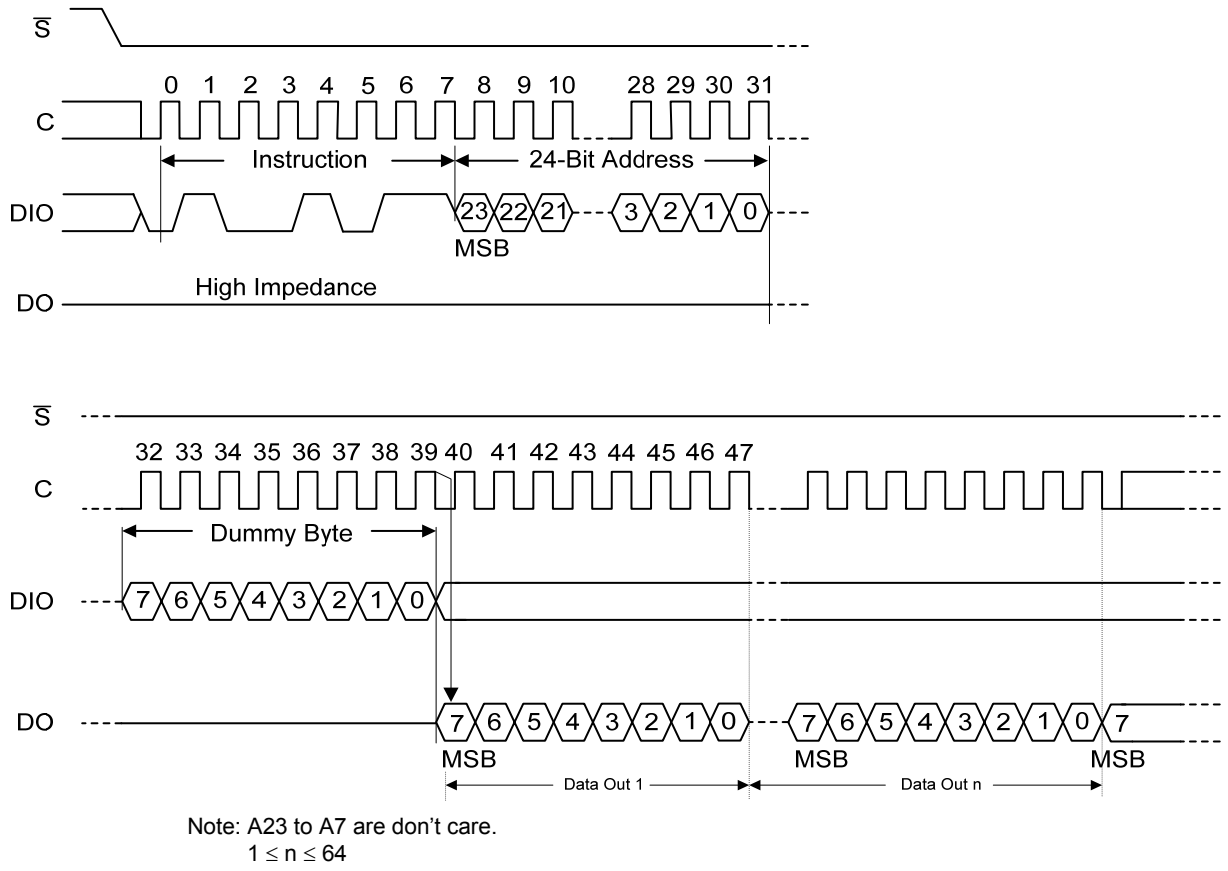


Note: Address bits A23 to A22 are Don't Care, for A25L032.
Address bits A23 to A21 are Don't Care, for A25L016.

Read OTP (ROTP)

The device is first selected by driving Chip Select ($\overline{S}$) Low. The instruction code for the Read OTP (ROTP) instruction is followed by a 3-byte address (A23- A0) and a dummy byte. Each bit is latched in on the rising edge of Serial Clock (C).
Then the memory contents at that address are shifted out on Serial Data output (DO).
Each bit is shifted out at the maximum frequency, fcmax, on the falling edge of Serial Clock (C).
The instruction sequence is shown in Figure 11.
The address is automatically incremented to the next higher address after each byte of data is shifted out.
The Read OTP (ROTP) instruction is terminated by driving Chip Select ($\overline{S}$) High. Chip Select ($\overline{S}$) can be driven High at any time during data output. Any Read OTP (ROTP) instruction issued while an Erase, Program or Write cycle is in progress, is rejected without having any effect on the cycle that is in progress.

Figure 11. Read OTP (ROTP) instruction and data-out sequence



Note: A23 to A7 are don't care.
$1 \le n \le 64$

Program OTP instruction (POTP)

The Program OTP instruction (POTP) is used to program at most 64 bytes to the OTP memory area (by changing bits from 1 to 0, only). Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL) bit.

The Program OTP instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction opcode, three address bytes and at least one data byte on Serial Data input (DIO).

Chip Select ($\overline{S}$) must be driven High after the eighth bit of the last data byte has been latched in, otherwise the Program OTP instruction is not executed.

The instruction sequence is shown in Figure 12.

As soon as Chip Select ($\overline{S}$) is driven High, the self-timed Page Program cycle (whose duration is t_{PP}) is initiated. While the Program OTP cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Program OTP cycle, and it is 0 when it is completed. At some unspecified time before the cycle is complete, the Write Enable Latch (WEL) bit is reset.

To lock the OTP memory:

Bit 0 of the OTP control byte, that is byte 63, (see Figure 13) is used to permanently lock the OTP memory array.

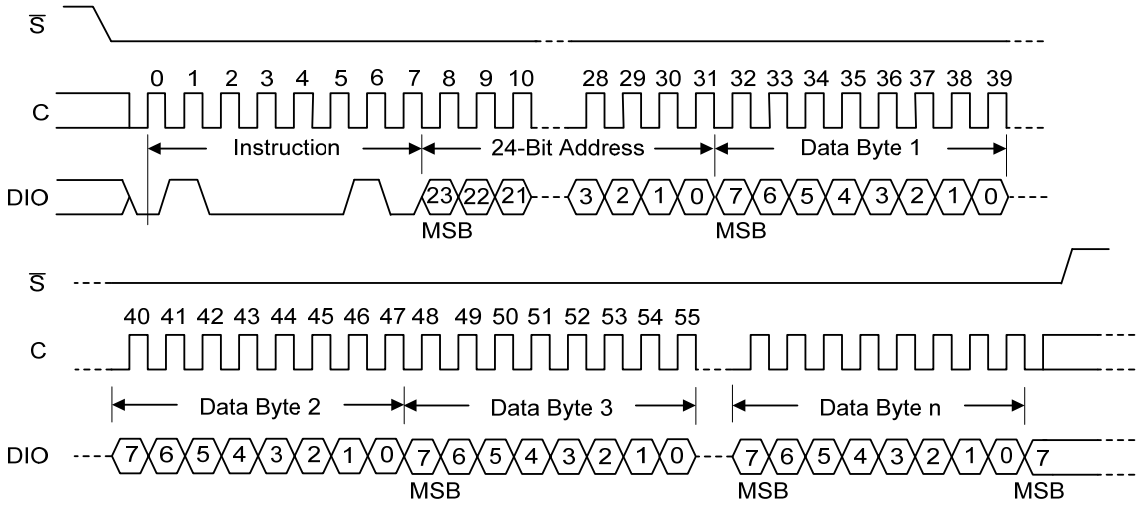
- When bit 0 of address 63h = '1', the OTP memory array can be programmed.
- When bit 0 of address 63h = '0', the OTP memory array are read-only and cannot be programmed anymore.

Once a bit of the OTP memory has been programmed to '0', it can no longer be set to '1'.

Therefore, as soon as bit 0 of address 63h (control byte) is set to '0', the 64 bytes of the OTP memory array become read-only in a permanent way.

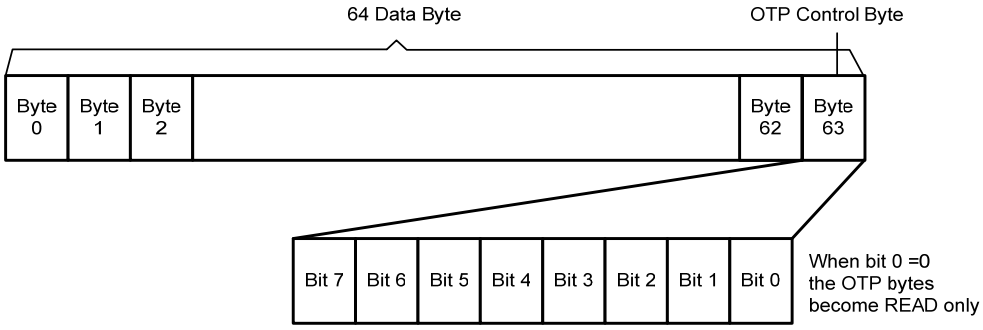
Any Program OTP (POTP) instruction issued while an Erase, Program or Write cycle is in progress is rejected without having any effect on the cycle that is in progress.

Figure 12. Program OTP (POTP) instruction sequence



Note: A23 to A7 are don't care.
$1 \le n \le 64$

Figure 13. How to permanently lock the 64 OTP bytes



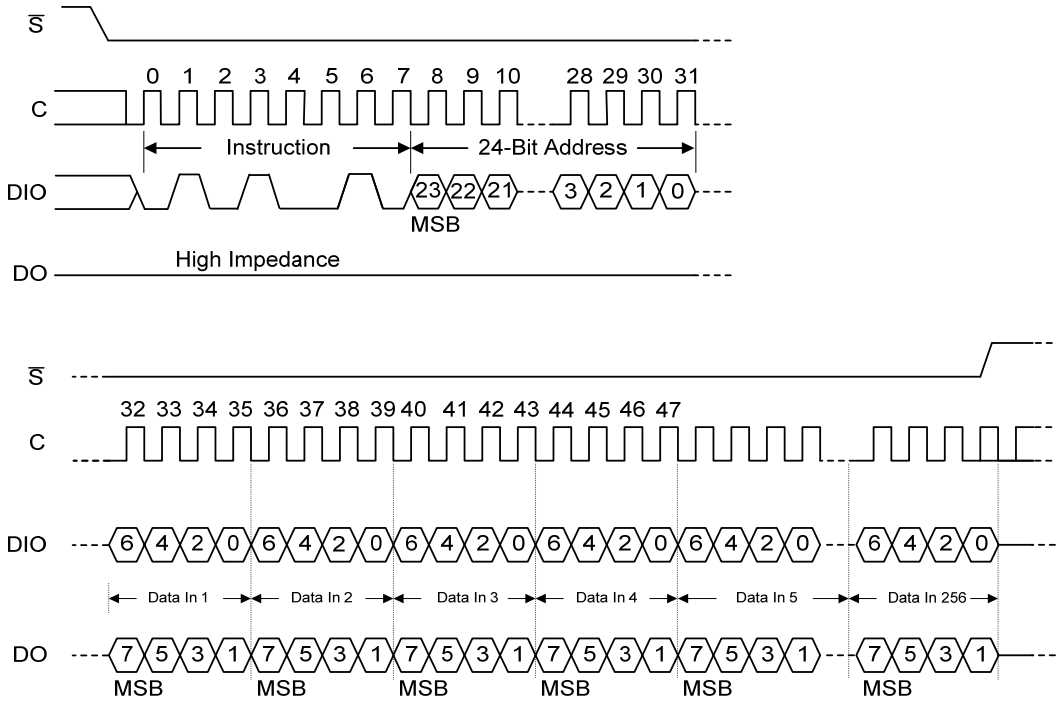
Dual Input Fast Program (DIFP)

The Dual Input Fast Program (DIFP) instruction is very similar to the Page Program (PP) instruction, except that the data are entered on two pins (pin DIO and pin DO) instead of only one. Inputting the data on two pins instead of one doubles the data transfer bandwidth compared to the Page Program (PP) instruction.
The Dual Input Fast Program (DIFP) instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction code, three address bytes and at least one data byte on Serial Data input (DIO).
If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits (A7-A0) are all zero). Chip Select ($\overline{S}$) must be driven Low for the entire duration of the sequence.
The instruction sequence is shown in Figure 14.
If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes in the same page.
For optimized timings, it is recommended to use the Dual Input Fast Program (DIFP) instruction to program all consecutive targeted bytes in a single sequence rather to using several Dual Input Fast Program (DIFP) sequences each containing only a few bytes.

Chip Select ($\overline{S}$) must be driven High after the eighth bit of the last data byte has been latched in, otherwise the Dual Input Fast Program (DIFP) instruction is not executed.

As soon as Chip Select ($\overline{S}$) is driven High, the self-timed Page Program cycle (whose duration is t_{PP}) is initiated. While the Dual Input Fast Program (DIFP) cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Page Program cycle, and 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.
A Dual Input Fast Program (DIFP) instruction applied to a page that is protected by the Block Protect (BP2, BP1, BP0) bits (see Table 1) is not executed.

Figure 14. Dual Input Fast Program (DIFP) instruction sequence



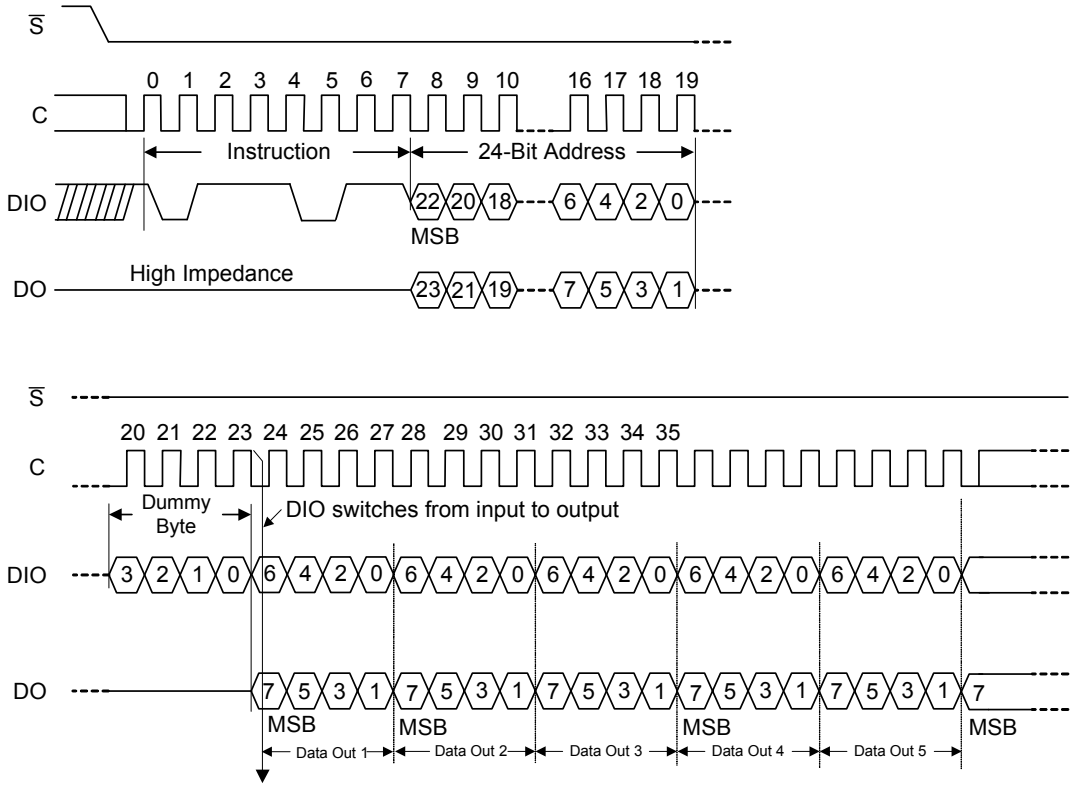
Note: A23 to A7 are don't care.

Fast Read Dual Input-Output (BBh)

The Fast Read Dual Input-Output (BBh) instruction is similar to the Fast_Read (0Bh) instruction except the data is input and output on two pins, DO and DIO, instead of just DO. This allows data to be transferred from the A25L032/A25L016 at twice the rate of standard SPI devices.

Similar to the Fast Read instruction, the Fast Read Dual Output instruction can operate at the highest possible frequency of f_C (See AC Characteristics). This is accomplished by adding four "dummy" clocks after the 24-bit address as shown in figure 15. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is "don't care". However, the DIO and DO pins should be high-impedance prior to the falling edge of the first data out clock.

Figure 15. FAST_READ_DUAL_INPUT-OUTPUT Instruction Sequence and Data-Out Sequence



Note: Address bits A23 to A22 are Don't Care, for A25L032.
Address bits A23 to A21 are Don't Care, for A25L016.

Page Program (PP)

The Page Program (PP) instruction allows bytes to be programmed in the memory (changing bits from 1 to 0). Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

The Page Program (PP) instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction code, three address bytes and at least one data byte on Serial Data Input (DIO). If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits (A7-A0) are all zero). Chip Select ($\overline{S}$) must be driven Low for the entire duration of the sequence.

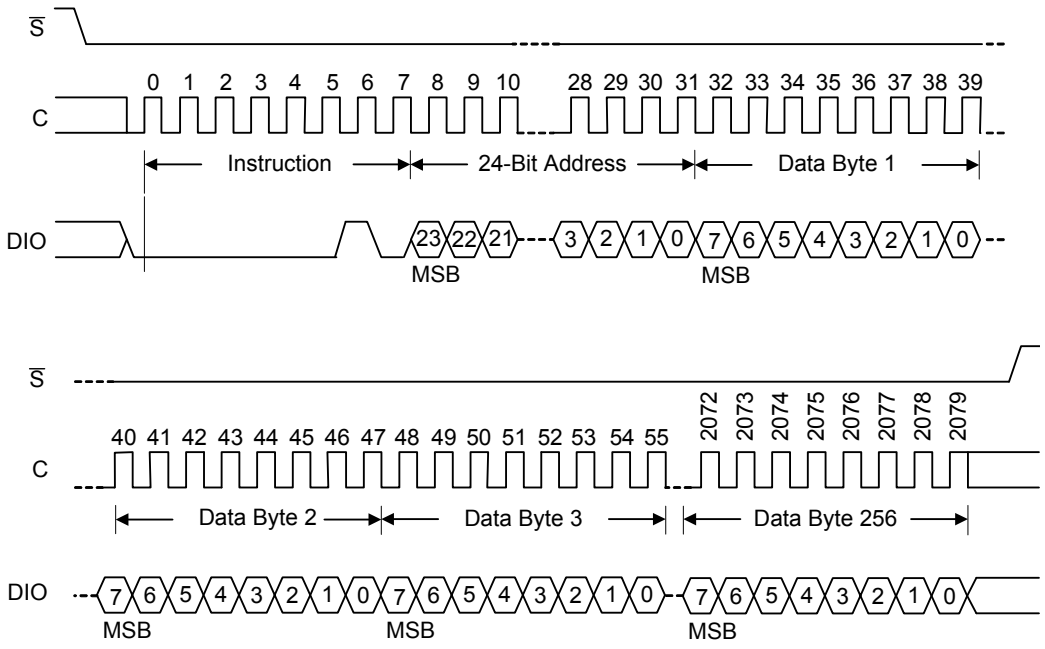
The instruction sequence is shown in Figure 16. If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 Data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page.

Chip Select ($\overline{S}$) must be driven High after the eighth bit of the last data byte has been latched in, otherwise the Page Program (PP) instruction is not executed.

As soon as Chip Select ($\overline{S}$) is driven High, the self-timed Page Program cycle (whose duration is t_{PP}) is initiated. While the Page Program cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Page Program (PP) instruction applied to a page which is protected by the Block Protect (BP2, BP1, BP0) bits (see table 1, table 2 and table 3) is not executed.

Figure 16. Page Program (PP) Instruction Sequence



Note: Address bits A23 to A22 are Don't Care, for A25L032.
Address bits A23 to A21 are Don't Care, for A25L016.

Sector Erase (SE)

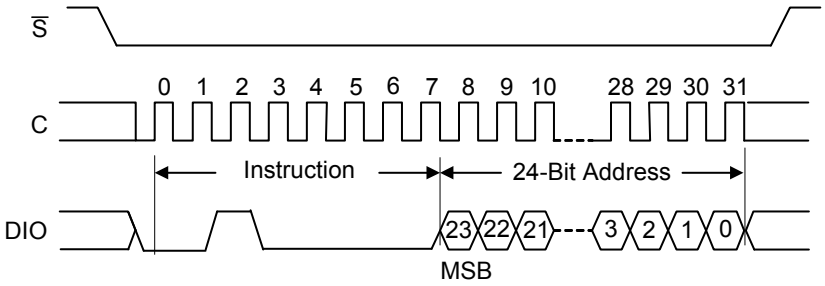
The Sector Erase (SE) instruction sets to 1 (FFh) all bits inside the chosen sector. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

The Sector Erase (SE) instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction code on Serial Data Input (DIO). Chip Select ($\overline{S}$) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in Figure 17. Chip Select ($\overline{S}$) must be driven High after the eighth bit of the instruction code has been latched in, otherwise the Sector Erase instruction is not executed. As soon as Chip Select ($\overline{S}$) is driven High, the self-timed Sector Erase cycle (whose duration is t_{SE}) is initiated. While the Sector Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Sector Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Sector Erase (SE) instruction applied to a page which is protected by the Block Protect (TB, BP2, BP1, BP0) bits (see table 1, table 2 and table 3) is not executed.

Figure 17. Sector Erase (SE) Instruction Sequence



Note: Address bits A23 to A22 are Don't Care, for A25L032.
Address bits A23 to A21 are Don't Care, for A25L016.

Block Erase (BE)

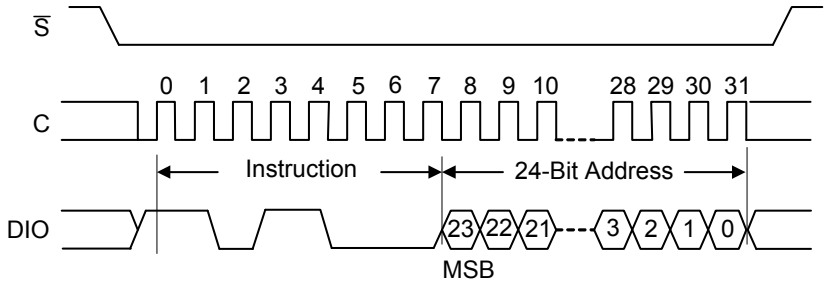
The Block Erase (BE) instruction sets to 1 (FFh) all bits inside the chosen block. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

The Block Erase (BE) instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction code on Serial Data Input (DIO). Chip Select ($\overline{S}$) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in Figure 18. Chip Select ($\overline{S}$) must be driven High after the eighth bit of the instruction code has been latched in, otherwise the Block Erase instruction is not executed. As soon as Chip Select ($\overline{S}$) is driven High, the self-timed Block Erase cycle (whose duration is t_{BE}) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Block Erase (BE) instruction applied to a page which is protected by the Block Protect (TB, BP2, BP1, BP0) bits (see table 1, table 2 and table 3) is not executed.

Figure 18. Block Erase (BE) Instruction Sequence



Note: Address bits A23 to A22 are Don't Care, for A25L032.
Address bits A23 to A21 are Don't Care, for A25L016.

Chip Erase (CE)

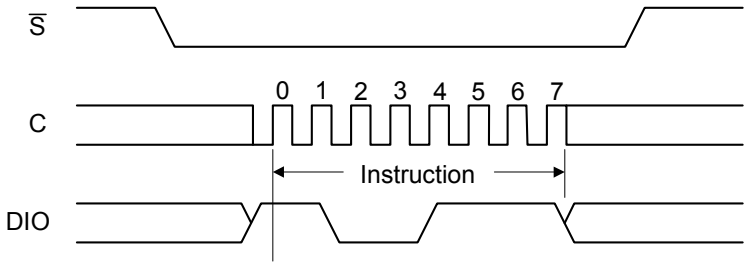
The Chip Erase (CE) instruction sets all bits to 1 (FFh). Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded, the device sets the Write Enable Latch (WEL).

The Chip Erase (CE) instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction code on Serial Data Input (DIO). Chip Select ($\overline{S}$) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in Figure 19. Chip Select ($\overline{S}$) must be driven High after the eighth bit of the instruction code has been latched in, otherwise the Block Erase instruction is not executed. As soon as Chip Select ($\overline{S}$) is driven High, the self-timed Chip Erase cycle (whose duration is t_{CE}) is initiated. While the Chip Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Chip Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

The Chip Erase (CE) instruction is executed only if all Block Protect (TB, BP2, BP1, BP0) bits are 0. The Chip Erase (CE) instruction is ignored if one, or more, blocks are protected.

Figure 19. Chip Erase (CE) Instruction Sequence



Note: Address bits A23 to A22 are Don't Care, for A25L032.
Address bits A23 to A21 are Don't Care, for A25L016.

Deep Power-down (DP)

Executing the Deep Power-down (DP) instruction is the only way to put the device in the lowest consumption mode (the Deep Power-down mode). It can also be used as an extra software protection mechanism, while the device is not in active use, since in this mode, the device ignores all Write, Program and Erase instructions.

Driving Chip Select ($\overline{S}$) High deselects the device, and puts the device in the Standby mode (if there is no internal cycle currently in progress). But this mode is not the Deep Power-down mode. The Deep Power-down mode can only be entered by executing the Deep Power-down (DP) instruction, to reduce the standby current (from I_{CC1} to I_{CC2}, as specified in DC Characteristics Table.).

Once the device has entered the Deep Power-down mode, all instructions are ignored except the Release from Deep Power-down and Read Electronic Signature (RES) instruction. This releases the device from this mode. The Release from Deep Power-down and Read Electronic Signature (RES) instruction also allows the Electronic Signature of the device to be output on Serial Data Output (DO).

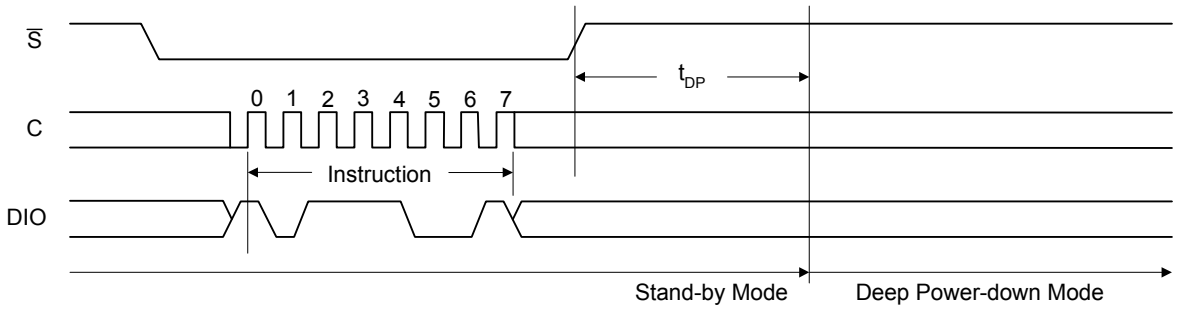
The Deep Power-down mode automatically stops at Power-down, and the device always Powers-up in the Standby mode.

The Deep Power-down (DP) instruction is entered by driving Chip Select ($\overline{S}$) Low, followed by the instruction code on Serial Data Input (DIO). Chip Select ($\overline{S}$) must be driven Low for the entire duration of the sequence. The instruction sequence is shown in Figure 20.

Chip Select ($\overline{S}$) must be driven High after the eighth bit of the instruction code has been latched in, otherwise the Deep Power-down (DP) instruction is not executed. As soon as Chip Select ($\overline{S}$) is driven High, it requires a delay of t_{DP} before the supply current is reduced to I_{CC2} and the Deep Power-down mode is entered.

Any Deep Power-down (DP) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 20. Deep Power-down (DP) Instruction Sequence



Read Device Identification (RDID)

The Read Identification (RDID) instruction allows the 8-bit manufacturer identification code to be read, followed by two bytes of device identification. The manufacturer identification is assigned by JEDEC, and has the value 37h. The device identification is assigned by the device manufacturer, and indicates the memory in the first bytes (30h), and the memory capacity of the device in the second byte (16h for A25L032, 15h for A25L016).

Any Read Identification (RDID) instruction while an Erase, or Program cycle is in progress, is not decoded, and has no effect on the cycle that is in progress.

The device is first selected by driving Chip Select ($\overline{S}$) Low. Then, the 8-bit instruction code for the instruction is shifted in. This is followed by the 24-bit device identification, stored in the memory, being shifted out on Serial Data Output (DO), each bit being shifted out during the falling edge of Serial Clock (C).

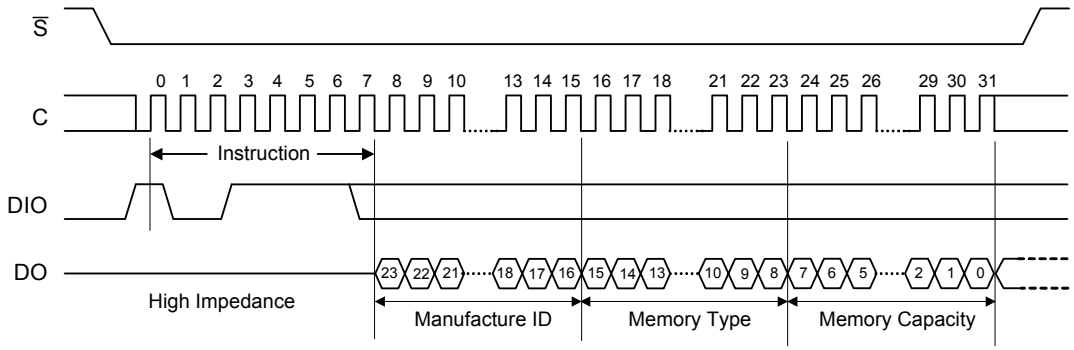
The instruction sequence is shown in Figure 21. The Read Identification (RDID) instruction is terminated by driving Chip Select ($\overline{S}$) High at any time during data output.

When Chip Select ($\overline{S}$) is driven High, the device is put in the Stand-by Power mode. Once in the Stand-by Power mode, the device waits to be selected, so that it can receive, decode and execute instructions.

Table 7. Read Identification (READ_ID) Data-Out Sequence

Manufacture Identification	Device Identification	
Manufacture ID	Memory Type	Memory Capacity
37h	30h	16h (A25L032)
		15h (A25L016)

Figure 21. Read Identification (RDID) Instruction Sequence and Data-Out Sequence



Read Electronic Manufacturer ID & Device ID (REMS)

The Read Electronic Manufacturer ID & Device ID (REMS) instruction allows the 8-bit manufacturer identification code to be read, followed by one byte of device identification. The manufacturer identification is assigned by JEDEC, and has the value 37h for AMIC. The device identification is assigned by the device manufacturer, and has the value 15h for A25L032, 14h for A25L016.

Any Read Electronic Manufacturer ID & Device ID (REMS) instruction while an Erase, or Program cycle is in progress, is not decoded, and has no effect on the cycle that is in progress.

The device is first selected by driving Chip Select ($\overline{S}$) Low. The 8-bit instruction code is followd by 2 dummy bytes and one byte address(A7~A0), each bit being latched-in on Serial Data Input (DIO) during the rising edge of Serial Clock (C).

If the one-byte address is set to 01h, then the device ID will be read first and then followed by the Manufacturer ID. On the other hand, if the one-byte address is set to 00h, then the Manufacturer ID will be read first and then followed by the device ID.

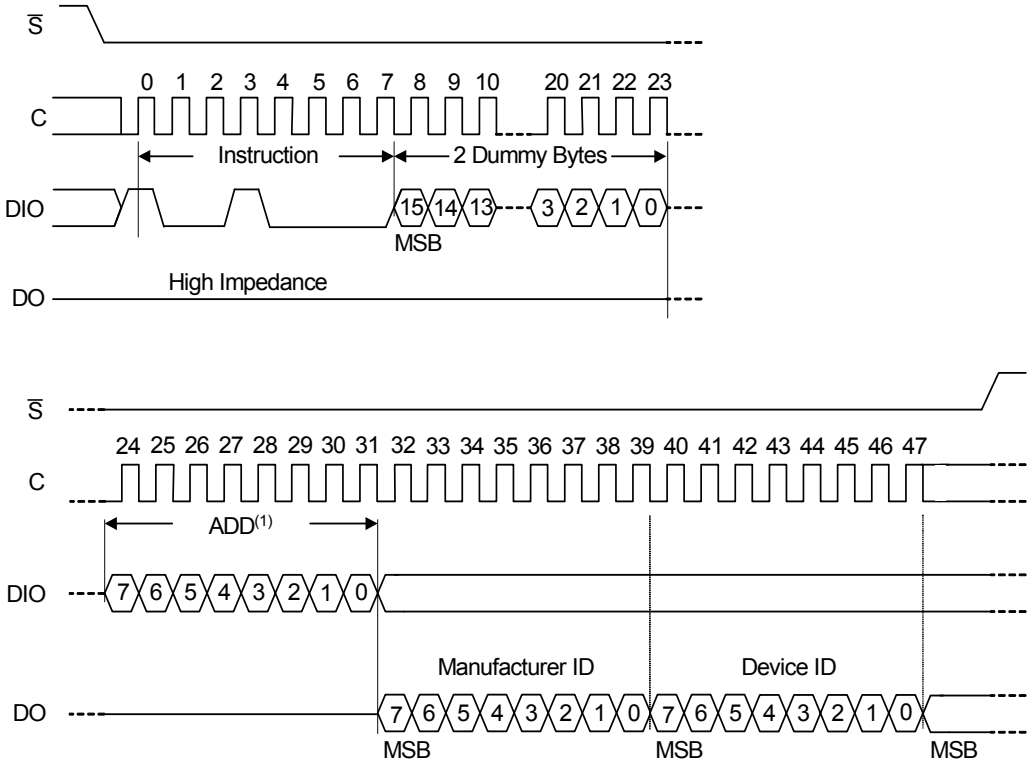
The instruction sequence is shown in Figure 22. The Read Electronic Manufacturer ID & Device ID (REMS) instruction is terminated by driving Chip Select ($\overline{S}$) High at any time during data output.

When Chip Select ($\overline{S}$) is driven High, the device is put in the Stand-by Power mode. Once in the Stand-by Power mode, the device waits to be selected, so that it can receive, decode and execute instructions.

Table 8. Read Electronic Manufacturer ID & Device ID (REMS) Data-Out Sequence

Manufacture Identification	Device Identification
37h	15h (A25L032)
	14h (A25L016)

Figure 22. Read Electronic Manufacturer ID & Device ID (REMS) Instruction Sequence and Data-Out Sequence



Notes:
(1) ADD=00h will output the manufacturer ID first and ADD=01h will output device ID first

Release from Deep Power-down and Read Electronic Signature (RES)

Once the device has entered the Deep Power-down mode, all instructions are ignored except the Release from Deep Power-down and Read Electronic Signature (RES) instruction. Executing this instruction takes the device out of the Deep Power-down mode.

The instruction can also be used to read, on Serial Data Output (DO), the 8-bit Electronic Signature, whose value for the *A25L032 is 15h, and for A25L016 is 14h.*

Except while an Erase, Program or Write Status Register cycle is in progress, the Release from Deep Power-down and Read Electronic Signature (RES) instruction always provides access to the 8-bit Electronic Signature of the device, and can be applied even if the Deep Power-down mode has not been entered.

Any Release from Deep Power-down and Read Electronic Signature (RES) instruction while an Erase, Program or Write Status Register cycle is in progress, is not decoded, and has no effect on the cycle that is in progress.

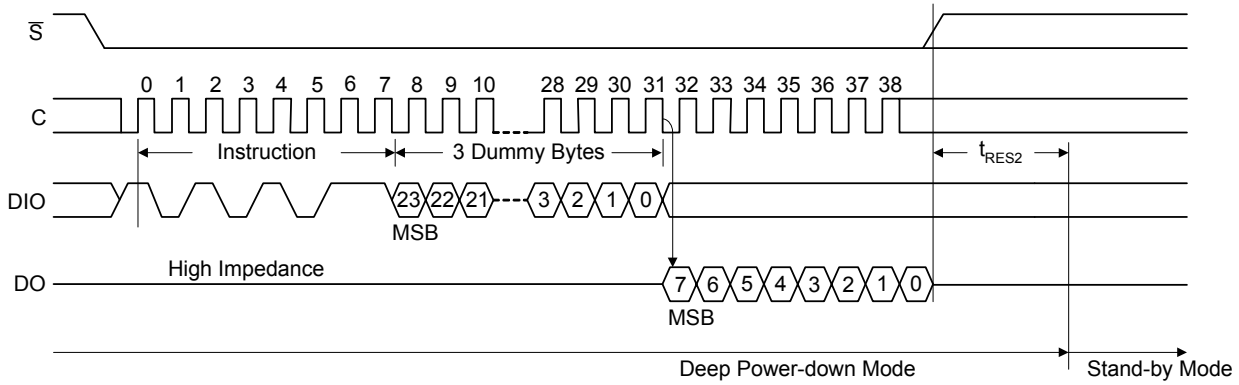
The device is first selected by driving Chip Select ($\overline{S}$) Low. The instruction code is followed by 3 dummy bytes, each bit being latched-in on Serial Data Input (DIO) during the rising edge of Serial Clock (C). Then, the 8-bit Electronic Signature, stored in the memory, is shifted out on Serial Data Output (DO), each bit being shifted out during the falling edge of Serial Clock (C).

The instruction sequence is shown in Figure 23.

The Release from Deep Power-down and Read Electronic Signature (RES) instruction is terminated by driving Chip Select ($\overline{S}$) High after the Electronic Signature has been read at least once. Sending additional clock cycles on Serial Clock (C), while Chip Select ($\overline{S}$) is driven Low, cause the Electronic Signature to be output repeatedly.

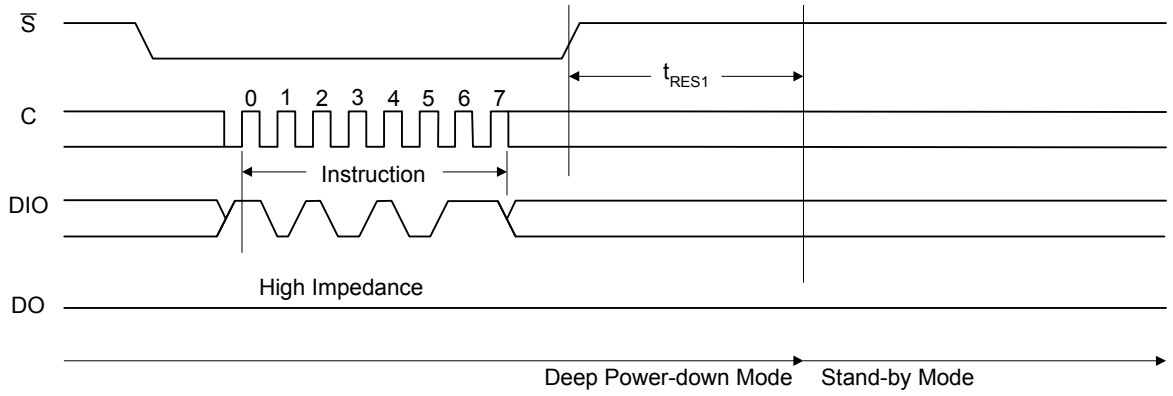
When Chip Select ($\overline{S}$) is driven High, the device is put in the Stand-by Power mode. If the device was not previously in the Deep Power-down mode, the transition to the Stand-by Power mode is immediate. If the device was previously in the Deep Power-down mode, though, the transition to the Stand-by Power mode is delayed by t_{RES2}, and Chip Select ($\overline{S}$) must remain High for at least t_{RES2} (max), as specified in AC Characteristics Table . Once in the Stand-by Power mode, the device waits to be selected, so that it can receive, decode and execute instructions.

Figure 23. Release from Deep Power-down and Read Electronic Signature (RES) Instruction Sequence and Data-Out Sequence



Note: The value of the 8-bit Electronic Signature, for the A25L032 is 15h, A25L016 is 14h.

Figure 24. Release from Deep Power-down (RES) Instruction Sequence



Driving Chip Select ($\overline{S}$) High after the 8-bit instruction byte has been received by the device, but before the whole of the 8-bit Electronic Signature has been transmitted for the first time (as shown in Figure 24.), still insures that the device is put into Stand-by Power mode. If the device was not previously in the Deep Power-down mode, the transition to the Stand-by Power mode is immediate. If the device was previously in the Deep Power-down mode, though, the transition to the Stand-by Power mode is delayed by t_{RES1}, and Chip Select ($\overline{S}$) must remain High for at least t_{RES1} (max), as specified in AC Characteristics Table. Once in the Stand-by Power mode, the device waits to be selected, so that it can receive, decode and execute instructions.

POWER-UP AND POWER-DOWN

At Power-up and Power-down, the device must not be selected (that is Chip Select ($\overline{S}$) must follow the voltage applied on V_{CC}) until V_{CC} reaches the correct value:

- V_{CC} (min) at Power-up, and then for a further delay of t_{VSL}
- V_{SS} at Power-down

Usually a simple pull-up resistor on Chip Select ($\overline{S}$) can be used to insure safe and proper Power-up and Power-down.

To avoid data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit is included. The logic inside the device is held reset while V_{CC} is less than the POR threshold value, V_{WI} – all operations are disabled, and the device does not respond to any instruction.

Moreover, the device ignores all Write Enable (WREN), Program OTP (POTP), Page Program (PP), Dual Input Fast Program (DIFP), Sector Erase (SE), Block Erase (BE), Chip Erase (CE) and Write Status Register (WRSR) instructions until a time delay of t_{PUW} has elapsed after the moment that V_{CC} rises above the VWI threshold. However, the correct operation of the device is not guaranteed if, by this time, V_{CC} is still below V_{CC}(min). No Write Status Register, Program or Erase instructions should be sent until the later of:

- t_{PUW} after V_{CC} passed the VWI threshold
- t_{VSL} afterV_{CC} passed the V_{CC}(min) level

These values are specified in Table 9.

If the delay, t_{VSL}, has elapsed, after V_{CC} has risen above V_{CC}(min), the device can be selected for READ instructions even if the t_{PUW} delay is not yet fully elapsed.

At Power-up, the device is in the following state:

- The device is in the Standby mode (not the Deep Power-down mode).
- The Write Enable Latch (WEL) bit is reset.

Normal precautions must be taken for supply rail decoupling, to stabilize the V_{CC} feed. Each device in a system should have the V_{CC} rail decoupled by a suitable capacitor close to the package pins. (Generally, this capacitor is of the order of 0.1µF).

At Power-down, when V_{CC} drops from the operating voltage, to below the POR threshold value, V_{WI}, all operations are disabled and the device does not respond to any instruction. (The designer needs to be aware that if a Power-down occurs while a Write, Program or Erase cycle is in progress, some data corruption can result.)

Figure 25. Power-up Timing

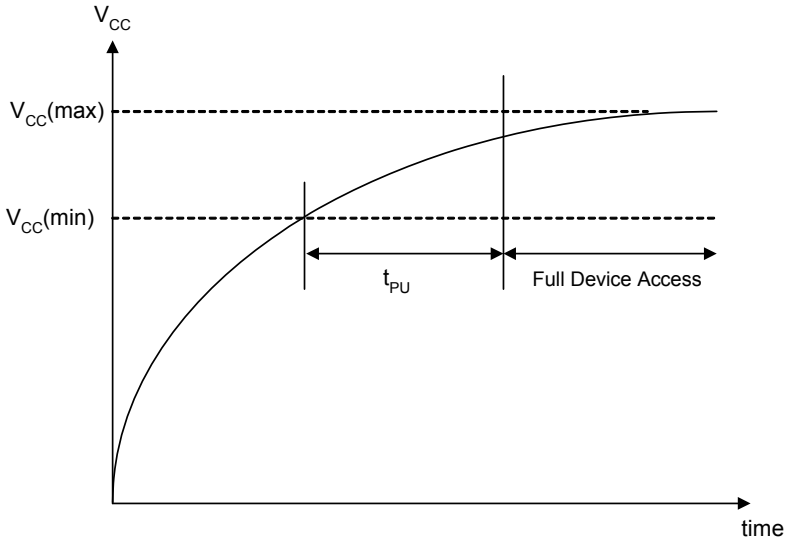


Table 9. Power-Up Timing

Symbol	Parameter	Min.	Max.	Unit
$V_{CC(min)}$	Vcc (minimum)	2.7		V
t_{PU}	Vcc (min) to device operation	10		ms

Note: These parameters are characterized only.

INITIAL DELIVERY STATE

The device is delivered with the memory array erased: all bits are set to 1 (each byte contains FFh). The Status Register contains 00h (all Status Register bits are 0).

Absolute Maximum Ratings*

Storage Temperature (TSTG) . . . . . -65°C to + 150°C
Lead Temperature during Soldering (Note 1)
D.C. Voltage on Any Pin to Ground Potential . . . . . -0.6V to VCC+0.6V
Transient Voltage (<20ns) on Any Pin to Ground Potential . . . . . -2.0V to VCC+2.0V
Supply Voltage (VCC) . . . . . -0.6V to +4.0V
Electrostatic Discharge Voltage (Human Body model) (VESD) (Note 2) . . . . . -2000V to 2000V

Notes:
1. Compliant with JEDEC Std J-STD-020B (for small body, Sn-Pb or Pb assembly).
2. JEDEC Std JESD22-A114A (C1=100 pF, R1=1500 Ω, R2=500 Ω)

*Comments

Stressing the device above the rating listed in the Absolute Maximum Ratings" table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the AMIC SURE Program and other relevant quality documents.

DC AND AC PARAMETERS

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC Characteristic tables that follow are derived from tests performed under the Measurement Conditions summarized in the relevant tables. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 10. Operating Conditions

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	2.7	3.6	V
T_A	Ambient Operating Temperature	–40	85	°C

Table 11. Data Retention and Endurance

Parameter	Condition	Min.	Max.	Unit
Erase/Program Cycles	At 85°C		100,000	Cycles per Sector
Data Retention	At 85°C		20	Years

Note: 1. This is preliminary data

Table 12. Capacitance

Symbol	Parameter	Test Condition	Min.	Max.	Unit
C_{OUT}	Output Capacitance (DO)	V_{OUT} = 0V		8	pF
C_{IN}	Input Capacitance (other pins)	V_{IN} = 0V		6	pF

Note: Sampled only, not 100% tested, at T_A=25°C and a frequency of 33 MHz.

Table 13. DC Characteristics

Symbol	Parameter	Test Condition	Min.	Max.	Unit
I_{LI}	Input Leakage Current			± 2	µA
I_{LO}	Output Leakage Current			± 2	µA
I_{CC1}	Standby Current	$\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}		50	µA
I_{CC2}	Deep Power-down Current	$\overline{S}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}		10	µA
I_{CC3}	Operating Current (READ)	C= 0.1V_{CC} / 0.9.V_{CC} at 50MHz, DO = open		20	mA
		C= 0.1V_{CC} / 0.9.V_{CC} at 33MHz, DO = open		15	mA
I_{CC4}	Operating Current (PP)	$\overline{S}$ = V_{CC}		15	mA
I_{CC5}	Operating Current (WRSR)	$\overline{S}$ = V_{CC}		15	mA
I_{CC6}	Operating Current (SE)	$\overline{S}$ = V_{CC}		15	mA
I_{CC7}	Operating Current (BE)	$\overline{S}$ = V_{CC}		15	mA
V_{IL}	Input Low Voltage		–0.5	0.3V_{CC}	V
V_{IH}	Input High Voltage		0.7V_{CC}	V_{CC}+0.4	V
V_{OL}	Output Low Voltage	I_{OL} = 1.6mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –100µA	V_{CC}–0.2		V

Note: 1. This is preliminary data at 85°C

Table 14. Instruction Times

Symbol	Alt.	Parameter	Min.	Typ.	Max.	Unit
t_W		Write Status Register Cycle Time		100	300	ms
t_{PP}		Page Program Cycle Time		3	5	ms
		Program OTP Cycle Time		2	3	ms
t_{SE}		Sector Erase Cycle Time		0.5	1	s
t_{BE}		Block Erase Cycle Time		1	3	s
t_{CE}		Chip Erase Cycle Time of A25L032		30	60	s
		Chip Erase Cycle Time of A25L016		15	30	s

Note: 1. At 85°C
2. This is preliminary data

Table 15. AC Measurement Conditions

Symbol	Parameter	Min.	Max.	Unit
C_L	Load Capacitance	30		pF
	Input Rise and Fall Times		5	ns
	Input Pulse Voltages	0.2V_{CC} to 0.8V_{CC}		V
	Input Timing Reference Voltages	0.3V_{CC} to 0.7V_{CC}		V
	Output Timing Reference Voltages	V_{CC} / 2		V

Note: Output Hi-Z is defined as the point where data out is no longer driven.

Figure 26. AC Measurement I/O Waveform

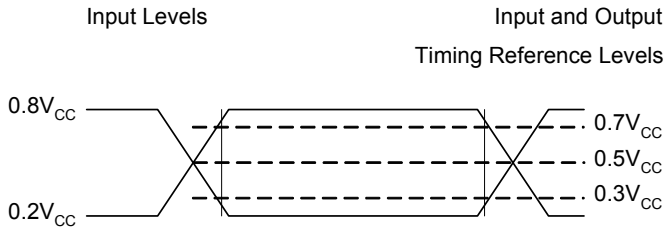


Table 16. AC Characteristics

Symbol	Alt.	Parameter	Min.	Typ.	Max.	Unit
f_C	f_C	Clock Frequency for the following instructions: FAST_READ, PP, SE, BE, DP, RES, RDID, WREN, WRDI, RDSR, WRSR (2.7V~3.6V) / (3V~3.6V)	D.C.		85/100	MHz
f_R		Clock Frequency for READ instructions	D.C.		50	MHz
t_{CH} [1]	t_{CLH}	Clock High Time	6			ns
t_{CL} [1]	t_{CLL}	Clock Low Time	5			ns
t_{CLCH} [2]		Clock Rise Time[3] (peak to peak)	0.1			V/ns
t_{CHCL} [2]		Clock Fall Time[3] (peak to peak)	0.1			V/ns
t_{SLCH}	t_{CSS}	$\overline{S}$ Active Setup Time (relative to C)	5			ns
t_{CHSL}		$\overline{S}$ Not Active Hold Time (relative to C)	5			ns
t_{DVCH}	t_{DSU}	Data In Setup Time	5			ns
t_{CHDX}	t_{DH}	Data In Hold Time	5			ns
t_{CHSH}		$\overline{S}$ Active Hold Time (relative to C)	5			ns
t_{SHCH}		$\overline{S}$ Not Active Setup Time (relative to C)	5			ns
t_{SHSL}	t_{CSH}	$\overline{S}$ Deselect Time	100			ns
t_{SHQZ} [2]	t_{DIS}	Output Disable Time			8	ns
t_{CLQV}	t_V	Clock Low to Output Valid			12/8	ns
t_{CLQX}	t_{HO}	Output Hold Time	0			ns
t_{HLCH}		$\overline{HOLD}$ Setup Time (relative to C)	5			ns
t_{CHHH}		$\overline{HOLD}$ Hold Time (relative to C)	5			ns
t_{HHCH}		HOLD Setup Time (relative to C)	5			ns
t_{CHHL}		HOLD Hold Time (relative to C)	5			ns
t_{HHQX} [2]	t_{LZ}	HOLD to Output Low-Z			8	ns
t_{HLQZ} [2]	t_{HZ}	$\overline{HOLD}$ to Output High-Z			8	ns
t_{WHSL} [4]		Write Protect Setup Time	20			ns
t_{SHWL} [4]		Write Protect Hold Time	100			ns
t_{DP} [2]		$\overline{S}$ High to Deep Power-down Mode			3	µs
t_{RES1} [2]		$\overline{S}$ High to Standby Mode without Electronic Signature Read			30	µs
t_{RES2} [2]		$\overline{S}$ High to Standby Mode with Electronic Signature Read			30	µs
t_W		Write Status Register Cycle Time		100	300	ms
t_{pp}		Page Program Cycle Time		3	5	ms
		Program OTP Cycle Time		2	3	ms
t_{SE}		Sector Erase Cycle Time		0.5	1.5	s
t_{BE}		Block Erase Cycle Time		1	3	s
t_{CE}		Chip Erase Cycle Time of A25L032		30	60	s
		Chip Erase Cycle Time of A25L016		15	30	s

Note: 1. $t_{CH} + t_{CL}$ must be greater than or equal to $1/f_C$
2. Value guaranteed by characterization, not 100% tested in production.
3. Expressed as a slew-rate.
4. Only applicable as a constraint for a WRSR instruction when SRWD is set at 1.

Figure 27. Serial Input Timing

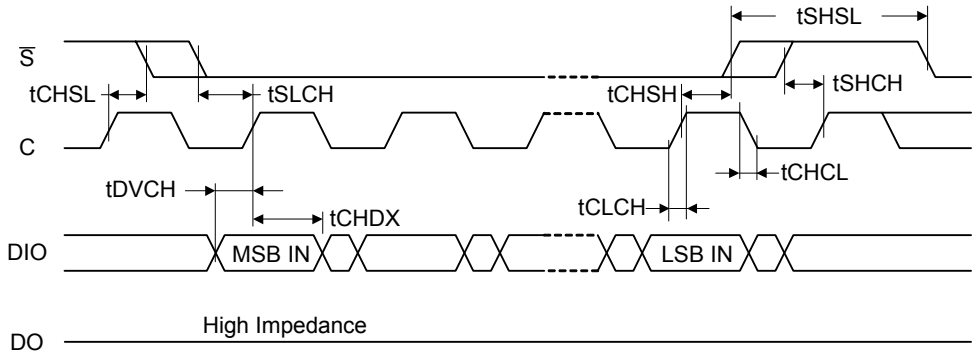


Figure 28. Write Protect Setup and Hold Timing during WRSR when SRWD=1

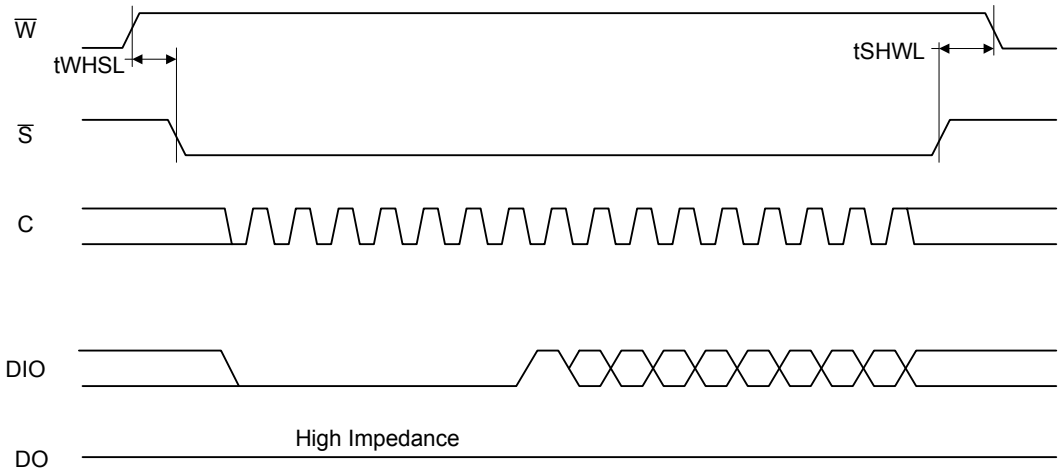


Figure 29. Hold Timing

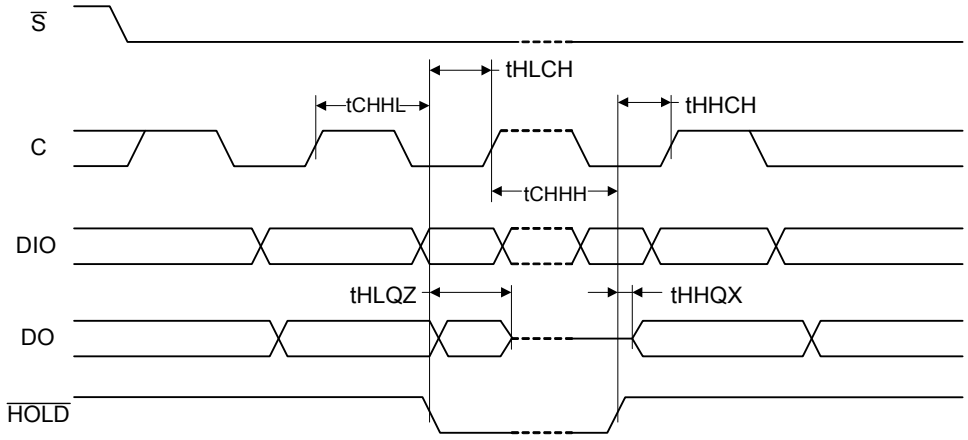
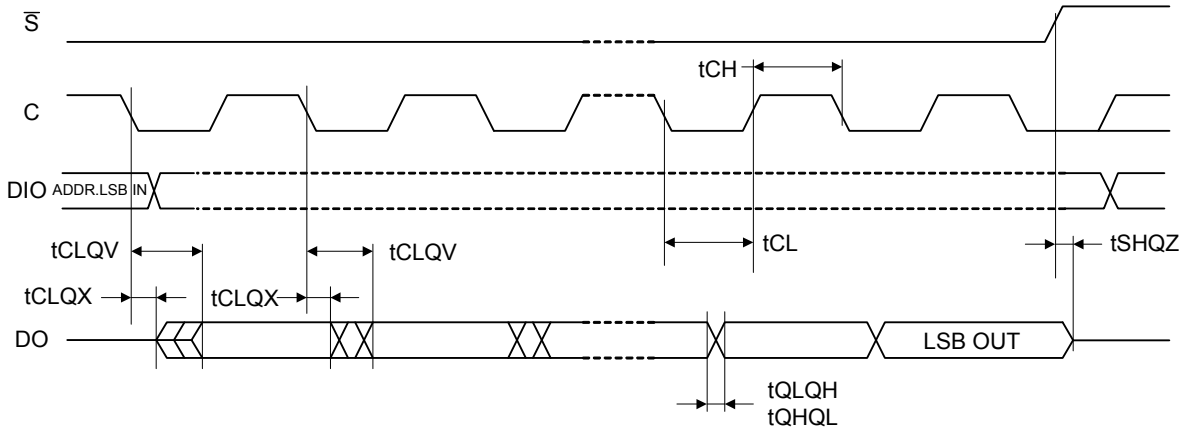
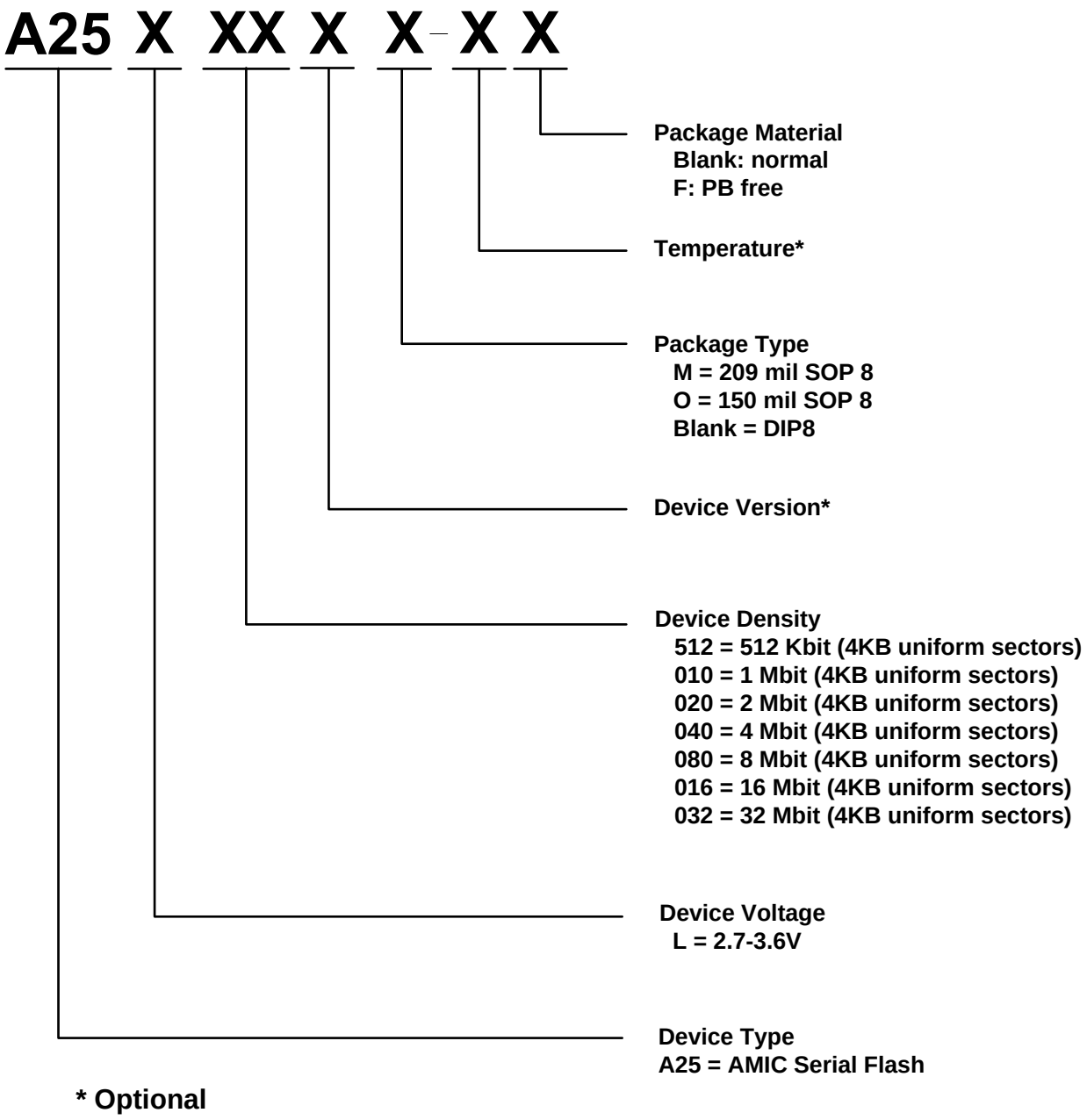


Figure 30. Output Timing



Part Numbering Scheme



*** Optional**

Ordering Information

Part No.	Speed (MHz) (2.7V~3.6V) / (3.0V~3.6V)	Active Read Current Typ. (mA)	Program/Erase Current Typ. (mA)	Standby Current Typ. (μ A)	Package
A25L032-F	85/100	20	15	50	8 Pin Pb-Free DIP (300 mil)
A25L032-UF					8 Pin Pb-Free DIP (300 mil)
A25L032M-F					8 Pb-Free Pin SOP (209mil)
A25L032M-UF					8 Pb-Free Pin SOP (209mil)

-U is for industrial operating temperature range: -40°C ~ +85°C

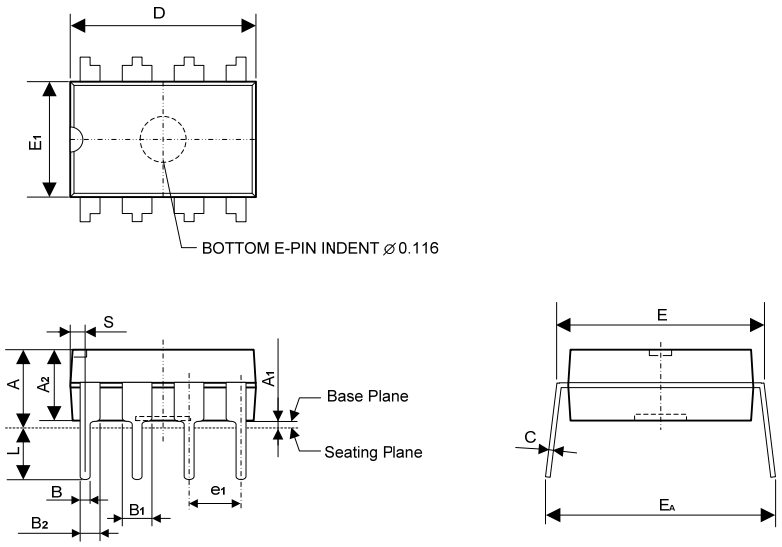
Part No.	Speed (MHz) (2.7V~3.6V) / (3.0V~3.6V)	Active Read Current Typ. (mA)	Program/Erase Current Typ. (mA)	Standby Current Typ. (μ A)	Package
A25L016-F	85/100	20	15	50	8 Pin Pb-Free DIP (300 mil)
A25L016-UF					8 Pin Pb-Free DIP (300 mil)
A25L016M-F					8 Pb-Free Pin SOP (209mil)
A25L016M-UF					8 Pb-Free Pin SOP (209mil)

-U is for industrial operating temperature range: -40°C ~ +85°C

Package Information

P-DIP 8L Outline Dimensions

unit: inches/mm



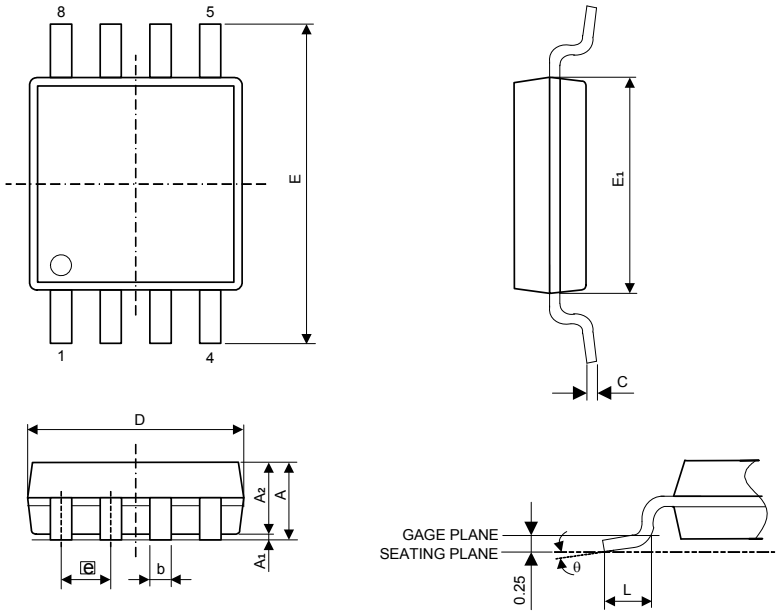
Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.180	-	-	4.57
A_1	0.015	-	-	0.38	-	-
A_2	0.128	0.130	0.136	3.25	3.30	3.45
B	0.014	0.018	0.022	0.36	0.46	0.56
B_1	0.050	0.060	0.070	1.27	1.52	1.78
B_2	0.032	0.039	0.046	0.81	0.99	1.17
C	0.008	0.010	0.013	0.20	0.25	0.33
D	0.350	0.360	0.370	8.89	9.14	9.40
E	0.290	0.300	0.315	7.37	7.62	8.00
E_1	0.254	0.260	0.266	6.45	6.60	6.76
e_1	-	0.100	-	-	2.54	-
L	0.125	-	-	3.18	-	-
E_A	0.345	-	0.385	8.76	-	9.78
S	0.016	0.021	0.026	0.41	0.53	0.66

Notes:

1. Dimension D and E_1 do not include mold flash or protrusions.
2. Dimension B_1 does not include dambar protrusion.
3. Tolerance: ±0.010” (0.25mm) unless otherwise specified.

Package Information

SOP 8L (209mil) Outline Dimensions unit: mm



Symbol	Dimensions in mm		
	Min	Nom	Max
A	1.75	1.95	2.16
A_1	0.05	0.15	0.25
A_2	1.70	1.80	1.91
b	0.35	0.42	0.48
C	0.19	0.20	0.25
D	5.13	5.23	5.33
E	7.70	7.90	8.10
E_1	5.18	5.28	5.38
e	1.27 BSC		
L	0.50	0.65	0.80
θ	0°	-	8°

Notes:

Maximum allowable mold flash is 0.15mm at the package ends and 0.25mm between leads