CY2256

Pentium™ and Cyrix 6x86 Compatible Clock Synthesizer/Driver for OPTi Viper™ Chipset

Features

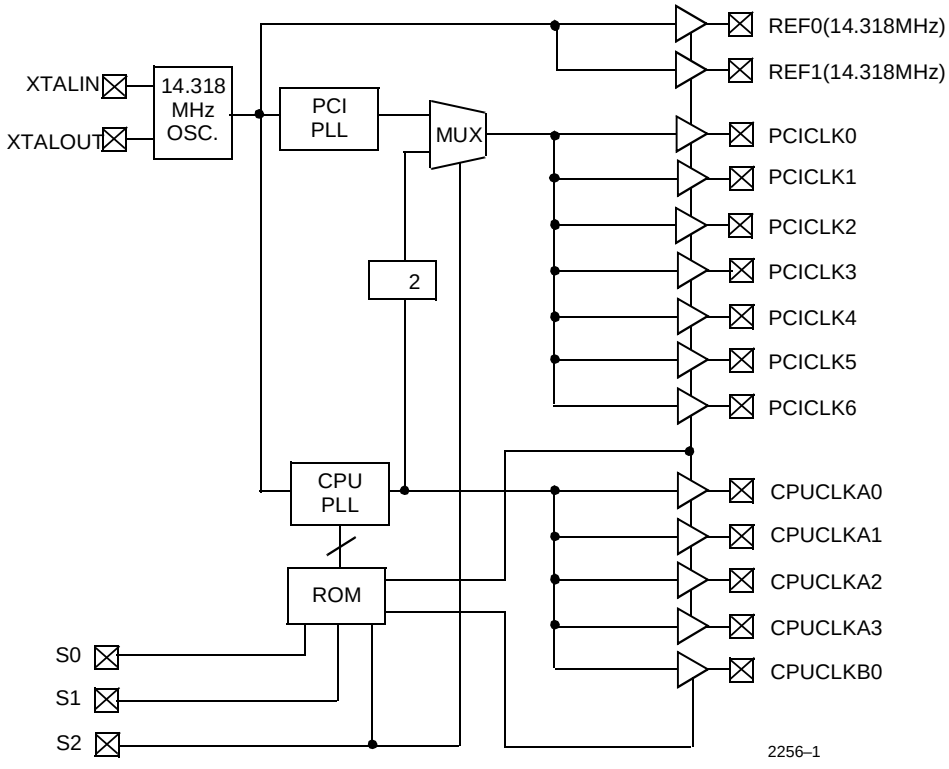
- **Multiple clock outputs to meet all requirements of Pentium™ or Cyrix 6x86-based motherboards using the OPTi Viper™ chipset**
  - **Five CPU clocks (CPUCLK) @ 75 MHz, 66.66 MHz, 60.0 MHz or 50.0 MHz, pin selectable**
  - **Seven PCI clocks (PCICLK) @ 25.0 MHz, 30.0 MHz or 33.3 MHz, pin selectable**
  - **Two Ref. clocks @ 14.318 MHz**
  - **Ref. 14.318 MHz Xtal oscillator input**
- **Low CPU and PCI clock jitter ≤ 250 ps cycle-to-cycle in synchronous PCI mode**
- **Low skew outputs**
  - **≤ 200 ps between CPU clocks**
  - **≤ 200 ps between PCI clocks**
  - **≤ 500 ps max. skew between CPU and PCI Clocks (in synchronous mode)**
- **Output duty cycle 45% min. to 55% max.**
- **Available in space-saving 28-pin SOIC and SSOP packages**
- **3.3V or 5.0V operation**
- **Internal pull-up resistors on select input**
- **Bank selectable CPU clock for synchronous DRAM support**

Functional Description

The CY2256 is a Clock Synthesizer/Driver chip for a Pentium or Cyrix 6x86-based PC using the OPTi Viper chipset. The CY2256 has low-skew outputs (≤ 200 ps between the CPU Clocks, ≤ 200 ps between the PCI Clocks). In addition, the CY2256 CPU clock outputs have less than 250 ps cycle-to-cycle jitter. Finally, both the PCI and CPU clock outputs meet the 1V/ns slew rate requirement of the Pentium processor-based system.

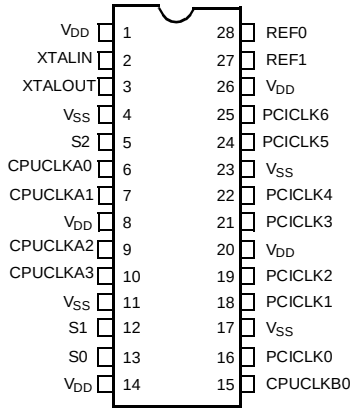
The CY2256 accepts a 14.318 MHz reference crystal or clock as its input. The CY2256 has two PLLs, one of which generates the CPU clocks, and the other generates the PCI clocks. The CY2256 runs off a 3.3V or 5.0V supply.

Logic Block Diagram



Pin Configuration

Top View
SOIC/SSOP



Note:
CPUCLK = CPU Clock
PCICLK = PCI Bus Clock

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Pin Summary

Name	Pin	Description
V_{DD}	1	Voltage supply
XTALIN[1]	2	Reference crystal input
XTALOUT[1]	3	Reference crystal feedback
V_{SS}	4	Ground
S2	5	CPU clock select input, bit 2 (internal pull-up resistor to V_{DD})
CPUCLKA0	6	CPU clock A output
CPUCLKA1	7	CPU clock A output
V_{DD}	8	Voltage supply
CPUCLKA2	9	CPU clock A output
CPUCLKA3	10	CPU clock A output
V_{SS}	11	Ground
S1	12	CPU clock select input, bit 1 (internal pull-up resistor to V_{DD})
S0	13	CPU clock select input, bit 0 (internal pull-up resistor to V_{DD})
V_{DD}	14	Voltage supply
CPUCLKB0	15	CPU clock B output
PCICLK0	16	PCI clock output
V_{SS}	17	Ground
PCICLK1	18	PCI clock output
PCICLK2	19	PCI clock output
V_{DD}	20	Voltage supply
PCICLK3	21	PCI clock output
PCICLK4	22	PCI clock output
V_{SS}	23	Ground
PCICLK5	24	PCI clock output
PCICLK6	25	PCI clock output
V_{DD}	26	Voltage supply
REF1	27	Reference clock output (14.318 MHz)
REF0	28	Reference clock output (14.318 MHz)

Function Table

S0	S1	S2	XTALIN Input	CPUCLKA	CPUCLKB	PCICLK	Ref. Clock Output	PCI Mode
0	0	0	14.318 MHz	50.0 MHz	50.0 MHz	25.0 MHz	14.318 MHz	Synch.
0	0	1	14.318 MHz	50.0 MHz	50.0 MHz	33.33 MHz	14.318 MHz	Asynch.
0	1	0	14.318 MHz	60.0 MHz	60.0 MHz	30.0 MHz	14.318 MHz	Synch.
0	1	1	14.318 MHz	60.0 MHz	60.0 MHz	33.33 MHz	14.318 MHz	Asynch.
1	0	0	14.318 MHz	66.66 MHz	66.66 MHz	33.33 MHz	14.318 MHz	Synch.
1	0	1	14.318 MHz	75.0 MHz	75.0 MHz	33.33 MHz	14.318 MHz	Asynch.
1	1	0	14.318 MHz	66.66 MHz	High-Z	33.33 MHz	14.318 MHz	Synch.
1	1	1	–	High-Z	High-Z	High-Z	High-Z	–

Notes:
1. For best accuracy, use a parallel-resonant crystal, C_{LOAD} = 18 pF.
2. TCLK is a test clock on the XTALIN input during test mode.

CPU and PCI Clock Driver Strengths

- Matched impedances on both rising and falling edges on the output drivers
- Output impedance: 25Ω (typical) measured at 1.5V

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage ..... –0.5 to +7.0V

Input Voltage .....–0.5V to V_{DD}+0.5

Storage Temperature (Non-Condensing)... –65°C to +150°C

Max. Soldering Temperature (10 sec)..... +260°C

Junction Temperature ..... +150°C

Package Power Dissipation..... 1W

Static Discharge Voltage ..... >2000V (per MIL-STD-883, Method 3015)

Operating Conditions[3]

Parameter	Description	Min.	Max.	Unit
V_{DD}	Supply Voltage	3.135	3.6	V
T_A	Operating Temperature, Ambient	0	70	°C
C_L	Max. Capacitive Load on CPUCLKA CPUCLKB PCICLK REF0 REF1		 30 30 30 15 30	pF
$f_{(REF)}$	Reference Frequency, Oscillator Nominal Value	14.318	14.318	MHz

Electrical Characteristics V_{DD} = 3.135V to 3.6V, T_A = 0°C to +70°C

Parameter	Description	Test Conditions			Min.	Max.	Unit
V_{IH}	High-level Input Voltage	Except Crystal Inputs			2.0		V
V_{IL}	Low-level Input Voltage	Except Crystal Inputs				0.8	V
V_{OH}	High-level Output Voltage	V_{DD} = V_{DD} Min.	I_{OH} = –23 mA	CPUCLKA/B	2.4		V
			I_{OH} = –23 mA	PCICLK			
			I_{OH} = –12 mA	REF0			
			I_{OH} = –16 mA	REF1			
V_{OL}	Low-level Output Voltage	V_{DD} = V_{DD} Min.	I_{OL} = 16 mA	CPUCLKA/B		0.4	V
			I_{OL} = 16 mA	PCICLK			
			I_{OL} = 8 mA	REF0			
			I_{OL} = 11 mA	REF1			
I_{IH}	Input High Current	V_{IH} = V_{DD}				5	µA
I_{IL}	Input Low Current	V_{IL} = 0V				100	µA
I_{OZ}	Output Leakage Current	Three-state			–10	+10	µA
I_{DD}	Power Supply Current	V_{DD} = 3.6V, V_{IN} = 0 or V_{DD}				90	mA

Note:

3. Electrical parameters are guaranteed with these operating conditions.

Switching Characteristics[4]

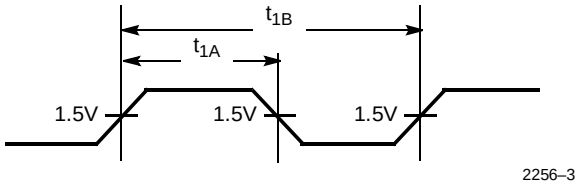
Parameter	Output	Description	Test Conditions	Min.	Max.	Unit
t_1	All	Output Duty Cycle[5]	$t_1 = t_{1A} \div t_{1B}$	45%	55%	
t_{1C}	CPUCLKA/B	CPU Clock HIGH Time	Measured at 2.4V	5.0		ns
t_{1C}	PCICLK	PCI Clock HIGH Time[6]	Measured at 2.4V	12.0		ns
t_{1D}	CPUCLKA/B	CPU Clock LOW Time	Measured at 0.4V	5.0		ns
t_{1D}	PCICLK	PCI Clock LOW Time[6]	Measured at 0.4V	12.0		ns
t_2	CPUCLKA/B	CPU Clock Rising and Falling Edge Rate	Measured between 0.4V and 2.4V	1	4.0	V/ns
t_3	CPUCLKA/B	CPU Clock Rise Time	Measured between 0.4V and 2.4V	0.5	2.0	ns
t_4	CPUCLKA/B	CPU Clock Fall Time	Measured between 2.4V and 0.4V	0.5	2.0	ns
t_2	PCICLK	PCI Clock Rising and Falling Edge Rate	Measured between 0.4V and 2.4V	1	4	V/ns
t_2	REFCLK	Reference Clock Rising and Falling Edge Rate	Measured between 0.4V and 2.4V	0.5		V/ns
t_5	CPUCLKA	CPU-CPU Clock Skew	Measured at 1.5V		200	ps
t_6	PCICLK	PCI-PCI Clock Skew	Measured at 1.5V		200	ps
t_7	CPUCLKA/B, PCICLK	CPU-PCI Clock Skew[7]	Measured at 1.5V		500	ps
t_8	CPUCLKA/B	Cycle-Cycle Clock Jitter[7]	CPU Clock jitter		250	ps
t_9	CPUCLKA/B	Power-up Time	CPU clock stabilization from power-up		3	ms
t_{10}	PCICLK	Power-up Time	PCI clock stabilization from power-up		3	ms

Notes:

4. All parameters specified with outputs fully loaded.
5. Duty cycle is measured at 1.5V.
6. A LOW and HIGH time of 12 ns corresponds to a PCICLK frequency of 33.33 MHz. For PCICLK frequencies of 30 MHz and 25 MHz, the LOW and HIGH times are each respectively 13.33 ns and 16 ns.
7. Synchronous mode only

Switching Waveforms

Duty Cycle Timing



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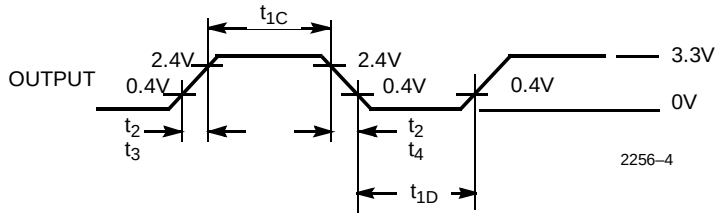
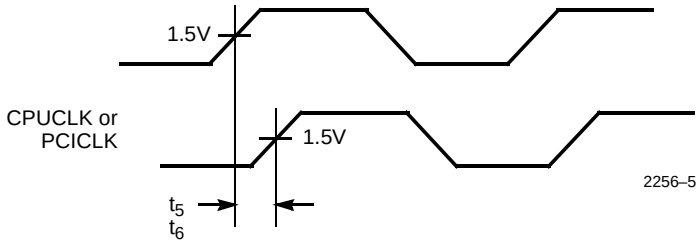
Switching Waveforms (continued)

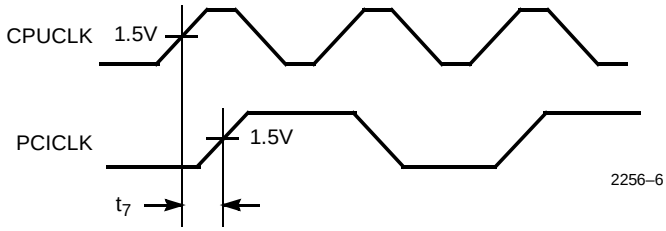
All Outputs Rise/Fall Time



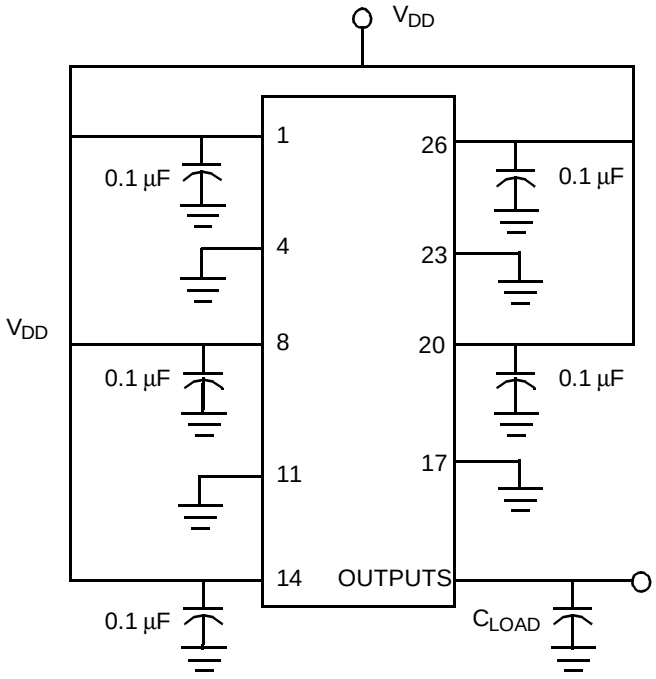
Clock Skew



CPU–PCI Clock Skew



Test Circuit



Note: All capacitors should be placed as close to each pin as possible.

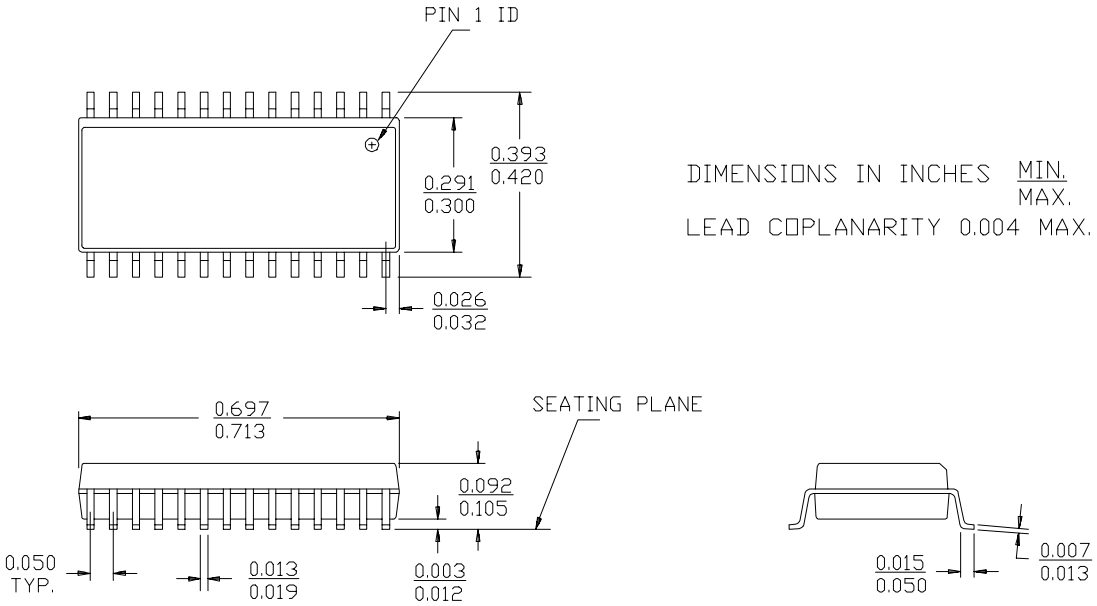
Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
CY2256SC-1	S21	28-Pin SOIC	Commercial
CY2256PVC-1	O28	28-Pin SSOP	Commercial

Document #: 38-00515-A

Package Diagrams

28-Lead (300-Mil) Molded SOIC S21



28-Lead Shrunk Small Outline Package O28