CY28RS680

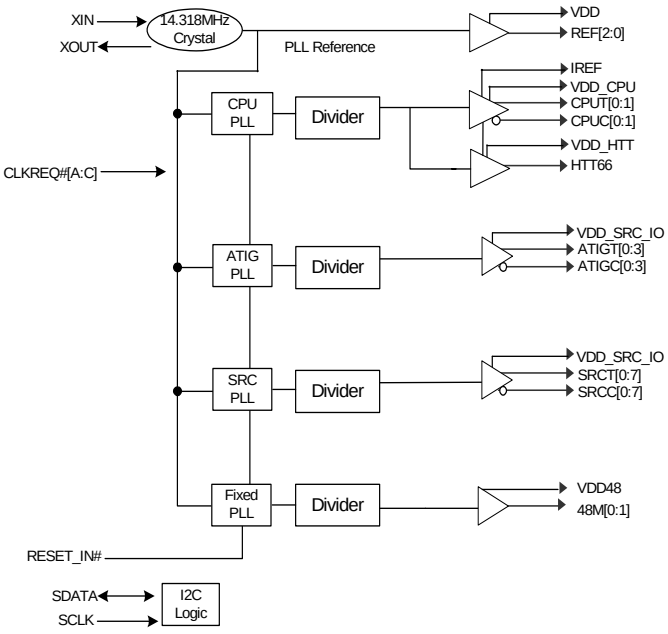
Clock Generator for ATI® RS5XX/6XX Chipsets

Features

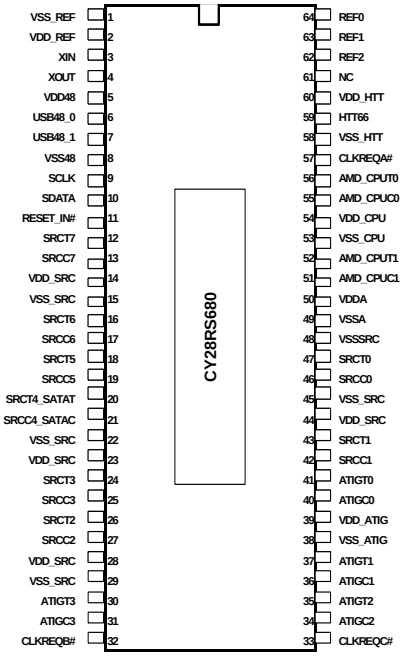
- Supports AMD® CPU
- Selectable CPU frequencies
- 200 MHz differential CPU clock pairs (25% over/ 50% under clocked)
- 100 MHz differential ATI Graphics clocks (100% over/10% under clocked)
- 100 MHz differential SRC clocks (10% over/under clocked)
- 48 MHz USB clock
- 66 MHz HyperTransport™ clock
- I^2C support with readback capabilities
- Ideal Lexmark Spread Spectrum profile for maximum electromagnetic interference (EMI) reduction
- 3.3V power supply
- 64-pin TSSOP packages

CPU	SRC	HTT66	ATIG	REF	USB_48
x2	x8	x1	X4	x 3	x 2

Block Diagram



Pin Configuration



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Pin Descriptions

Pin No.	Name	Type	Description
1	VSS_REF	PWR	GND for REF, XTAL
2	VDD_REF	PWR	3.3V power supply for REF, XTAL
3	XIN	I	14.318 MHz Crystal Input
4	XOUT	O	14.318 MHz Crystal Output
5	VDD_48	PWR	3.3V power supply for USB outputs
6, 7	USB_48 [1:0]	O, SE	48 MHz clock output. Intel® Type-3A buffer.
8	VSS_48	GND	Ground for USB outputs
9	SCLK	I,PU	SMBus-compatible SCLOCK.This pin has an internal pull up, but is tri-stated in power down.
10	SDATA	I/O,PU	SMBus-compatible SDATA.This pin has an internal pull up, but is tri-stated in power down.
11	RESET_IN#	I	3.3V LVTTL Input (Negative Edge Triggered) When this pin is asserted LOW, all PLLs will transition to a safe default frequency. This may be the POR defaults or a safe value stored in SMBUS registers.
12, 13	SRCT/C[7]	O, DIF	100 MHz differential serial reference clock. Intel Type-SR buffer. (10% overclocking support through SMBUS)
14	VDD_SRC	PWR	3.3V power supply for SRC outputs
15	VSS_SRC	GND	Ground for SRC outputs
16, 17, 18, 19, 20, 21	SRCT/C[6:4]	O, DIF	100 MHz differential serial reference clock. Intel Type-SR buffer. (10% overclocking support through SMBUS)
22	VSS_SRC	GND	Ground for SRC outputs
23	VDD_SRC	PWR	3.3V power supply for SRC outputs
24, 25, 26, 27	SRCT/C[3:2]	O, DIF	100 MHz differential serial reference clock. Intel Type-SR buffer. (10% overclocking support through SMBUS)
28	VDD_SRC	PWR	3.3V power supply for SRC outputs
29	VSS_SRC	GND	Ground for SRC outputs
30,31	ATIGT/C3	O, DIF	Differential Selectable serial reference clock. Intel Type-SR buffer. Includes 50% overclock support through SMBUS
32, 33	CLKREQ#[B:C]	I, SE, PU	Output Enable control for SRCT/C. Output enable control required by Minicard specification. This pin has an internal pull up. 0 = Selected SRC output is enabled. 1 = Selected SRC output is disabled
34, 35, 36, 37	ATIGT/C[2:1]	O, DIF	Differential Selectable serial reference clock. Intel Type-SR buffer. Includes 50% overclock support through SMBUS
38	VSS_ATIG	GND	Ground for ATIG outputs
39	VDD_ATIG	PWR	3.3V power supply for ATIG outputs
40, 41	ATIGT/C0	O, DIF	Differential Selectable serial reference clock. Intel Type-SR buffer. Includes 50% overclock support through SMBUS
42, 43	SRCT/C1	O, DIF	100 MHz differential serial reference clock. Intel Type-SR buffer. (10% overclocking support through SMBUS)
44	VDD_SRC	PWR	3.3V power supply for SRC outputs
45	VSS_SRC	GND	Ground for SRC outputs
46,47	SRCT/C0	O, DIF	100 MHz differential serial reference clock. Intel Type-SR buffer. (10% overclocking support through SMBUS)
48	VSS_SRC	GND	Ground for SRC outputs
49	VSSA	GND	Analog Ground
50	VDDA	PWR	3.3V Analog Power for PLLs

Pin Descriptions (continued)

Pin No.	Name	Type	Description
51, 52, 55, 56	CPUT/C[1:0]	O, DIF	Differential CPU clock output. Intel Type-SR buffer
53	VSS_CPU	GND	Ground for CPU outputs
54	VDD_CPU	PWR	3.3V power supply for CPU outputs
57	CLKREQ#A	I, SE, PU	Output Enable control for SRCT/C. Output enable control required by Minicard specification. This pin has an internal pull up. 0 = Selected SRC output is enabled. 1 = Selected SRC output is disabled.
58	VSS_HTT	PWR	Ground for HyperTransport outputs
59	HTT66	O, SE	66 MHz clock output. Intel Type-5 buffer.
60	VDD_HTT	PWR	3.3V power supply for HyperTransport outputs
61	NC	I	No Connect
62, 63, 64	REF[2:0]	O, SE	14.318 MHz REF clock output. Intel Type-5 buffer.

Serial Data Interface

To enhance the flexibility and function of the clock synthesizer, a two-signal serial interface is provided. Through the Serial Data Interface, various device functions, such as individual clock output buffers, can be individually enabled or disabled. The registers associated with the Serial Data Interface initialize to their default setting upon power up, and therefore use of this interface is optional. Clock device register changes are normally made upon system initialization, if any are required. The interface cannot be used during system operation for power management functions.

Data Protocol

The clock driver serial protocol accepts byte write, byte read, block write, and block read operations from the controller. For block write/read operation, the bytes must be accessed in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after any complete byte has been transferred. For byte write and byte read operations, the system controller can access individually indexed bytes. The offset of the indexed byte is encoded in the command code, as described in Table 1.

The block write and block read protocol is outlined in Table 2 while Table 3 outlines the corresponding byte write and byte read protocol. The slave receiver address is 11010010 (D2h).

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Table 1. Command Code Definition

Bit	Description
7	0 = Block read or block write operation, 1 = Byte read or byte write operation
(6:5)	Chip select address, set to ‘00’ to access device
(4:0)	Byte offset for byte read or byte write operation. For block read or block write operations, these bits should be '00000'

Table 2. Block Read and Block Write Protocol

Block Write Protocol		Block Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
8:2	Slave address – 7 bits	8:2	Slave address – 7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
18:11	Command Code – 8 bits	18:11	Command Code – 8 bits
19	Acknowledge from slave	19	Acknowledge from slave
27:20	Byte Count – 8 bits	20	Repeat start
28	Acknowledge from slave	27:21	Slave address – 7 bits
36:29	Data byte 1 – 8 bits	28	Read = 1
37	Acknowledge from slave	29	Acknowledge from slave
45:38	Data byte 2 – 8 bits	37:30	Byte Count from slave – 8 bits
46	Acknowledge from slave	38	Acknowledge
....	Data Byte /Slave Acknowledges	46:39	Data byte 1 from slave – 8 bits
....	Data Byte N – 8 bits	47	Acknowledge
....	Acknowledge from slave	55:48	Data byte 2 from slave – 8 bits
....	Stop	56	Acknowledge
		....	Data bytes from slave / Acknowledge
		....	Data Byte N from slave – 8 bits
		....	NOT Acknowledge

Table 3. Byte Read and Byte Write Protocol

Byte Write Protocol		Byte Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
8:2	Slave address – 7 bits	8:2	Slave address – 7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
18:11	Command Code – 8 bits	18:11	Command Code – 8 bits
19	Acknowledge from slave	19	Acknowledge from slave
27:20	Data byte – 8 bits	20	Repeated start
28	Acknowledge from slave	27:21	Slave address – 7 bits
29	Stop	28	Read
		29	Acknowledge from slave
		37:30	Data from slave – 8 bits
		38	NOT Acknowledge
		39	Stop

Control Registers

Byte 0: Output Enable Register 0

Bit	@Pup	Name	Description
7	1	SRC[T/C]7	SRC[T/C]7 Output Enable 0 = Disable (Hi-Z), 1 = Enable
6	1	SRC[T/C]6	SRC[T/C]6 Output Enable 0 = Disable (Hi-Z), 1 = Enable
5	1	SRC[T/C]5	SRC[T/C]5 Output Enable 0 = Disable (Hi-Z), 1 = Enable
4	1	SRC[T/C]4	SRC[T/C]4 Output Enable 0 = Disable (Hi-Z), 1 = Enable
3	1	SRC[T/C]3	SRC[T/C]3 Output Enable 0 = Disable (Hi-Z), 1 = Enable
2	1	SRC[T/C]2	SRC[T/C]2 Output Enable 0 = Disable (Hi-Z), 1 = Enable
1	1	SRC[T/C]1	SRC[T/C]1 Output Enable 0 = Disable (Hi-Z), 1 = Enable
0	1	SRC [T/C]0	SRC[T/C]0 Output Enable 0 = Disable (Hi-Z), 1 = Enable

Byte 1: Output Enable Register 1

Bit	@Pup	Name	Description
7	1	Reserved	Reserved
6	1	Reserved	Reserved
5	1	ATIG[T/C]3	ATIG[T/C]3 Output Enable 0 = Disable (Hi-Z), 1 = Enable
4	1	ATIG[T/C]2	ATIG[T/C]2 Output Enable 0 = Disable (Hi-Z), 1 = Enable
3	1	ATIG[T/C]1	ATIG[T/C]1 Output Enable 0 = Disable (Hi-Z), 1 = Enable
2	1	ATIG[T/C]0	ATIG[T/C]0 Output Enable 0 = Disable (Hi-Z), 1 = Enable

Byte 1: Output Enable Register 1 (continued)

Bit	@Pup	Name	Description
1	1	Reserved	Reserved
0	1	CPU[T/C]1	CPU[T/C]1 Output Enable 0 = Disable (Hi-Z), 1 = Enable

Byte 2: Output Enable Register 2

Bit	@Pup	Name	Description
7	1	CPU[T/C]0	CPU[T/C]0 Output Enable 0 = Disable (Hi-Z), 1 = Enable
6	1	USB_48_1	USB_48_1 Output Enable 0 = Disable (Hi-Z), 1 = Enable
5	1	USB_48_0	USB_48_0 Output Enable 0 = Disable (Hi-Z), 1 = Enable
4	1	REF_2	REF_2 Output Enable 0 = Disable (Hi-Z), 1 = Enable
3	1	REF_1	REF_1 Output Enable 0 = Disable (Hi-Z), 1 = Enable
2	1	REF_0	REF_0 Output Enable 0 = Disable (Hi-Z), 1 = Enable
1	1	HTT66	HTT66 Output Enable 0 = Disable (Hi-Z), 1 = Enable
0	0	CPU Spread Enable	CPU_PLL (PLL1) Spread Spectrum Enable 0= Spread Off, 1 = Spread On

Byte 3: SW_FREQ Selection Register

Bit	@Pup	Name	Description
7	0	Reserved	Reserved
6	0	Reserved	Reserved
5	0	Reserved	Reserved
4	1	ATIG_OC_SEL1	
3	0	ATIG_OC_SEL0	
2	0	FSEL_C	SW Frequency Selection Bits
1	1	FSEL_B	
0	0	FSEL_A	

SEL1	SEL0	ATIG Output	N
0	0	111.33–166 MHz	166–250
1	0	100–125 MHz	200–250
X	1	166–256 MHz	166–256

Byte 4: Spread Spectrum Control Register

Bit	@Pup	Name	Description
7	0	CPU_SS1	CPU(PLL1) Spread Spectrum Selection 00: –0.5% (peak to peak) 01: ±0.25% (peak to peak) 10: –1.0% (peak to peak) 11: ±0.5% (peak to peak)
6	0	CPU_SS0	
5	0	ATIG_SS0	ATIG(PLL2) Spread Spectrum Selection 00: –0.5% (peak to peak) 01: –1.0% (peak to peak)

Byte 4: Spread Spectrum Control Register (continued)

Bit	@Pup	Name	Description
4	0	ATIG_SS_OFF	ATIG_PLL (PLL2) Spread Spectrum Enable 0 = Spread Off, 1 = Spread On
3	0	SRC_SS_OFF	SRC_PLL (PLL3) Spread Spectrum Enable 0 = Spread Off, 1 = Spread On
2	1	USB48	USB48 Output Drive Strength 0 = 1x, 1 = 2x
1	0	Reserved	Reserved
0	0	REF	REF Output Drive Strength 0 = 1x, 1 = 2x

Byte 5: System Configuration Register

Bit	@Pup	Name	Description
7	0	Reserved	Reserved
6	0	Reserved	Reserved
5	0	Reserved	Reserved
4	0	Reserved	Reserved
3	0	Reserved	Reserved
2	0	Reserved	Reserved
1	1	Reserved	Reserved
0	0	CLKREQA#	CLKREQA# Controls SRC0 0 = Not controlled, 1 = Controlled

Byte 6: Revision and Device ID

Bit	@Pup	Name	Description
7	0		Revision Code Bit 3
6	0		Revision Code Bit 2
5	1		Revision Code Bit 1
4	1		Revision Code Bit 0
3	0		Device ID Bit 3
2	0		Device ID Bit 2
1	1		Device ID Bit 1
0	0		Device ID Bit 0

Byte 7: Vendor ID

Bit	@Pup	Name	Description
7	0	Reserved	Reserved
6	0	Reserved	Reserved
5	0	Reserved	Reserved
4	0	Reserved	Reserved
3	1		Vendor ID Bit 3
2	0		Vendor ID Bit 2
1	0		Vendor ID Bit 1
0	0		Vendor ID Bit 0

Byte 8: SRC PLL (PLL3) Overclocking Register

Bit	@Pup	Name	Description
7	0	SRC_N[7]	N counter Control bit [7:0]
6	0	SRC_N[6]	N counter Control bit [7:0]
5	0	SRC_N[5]	N counter Control bit [7:0]
4	0	SRC_N[4]	N counter Control bit [7:0]
3	0	SRC_N[3]	N counter Control bit [7:0]
2	0	SRC_N[2]	N counter Control bit [7:0]
1	0	SRC_N[1]	N counter Control bit [7:0]
0	0	SRC_N[0]	N counter Control bit [7:0]

Byte 9: Clock Request Mapping Register

Bit	@Pup	Name	Description
7	0	CLKREQC#	CLKREQC# Controls ATIG3 0 = Not controlled, 1 = Controlled
6	0	CLKREQC#	CLKREQC# Controls ATIG2 0 = Not controlled, 1 = Controlled
5	0	CLKREQC#	CLKREQC# Controls ATIG1 0 = Not controlled, 1 = Controlled
4	1	CLKREQC#	CLKREQC# Controls ATIG0 0 = Not controlled, 1 = Controlled
3	0	CLKREQB#	CLKREQB# Controls SRC7 0 = Not controlled, 1 = Controlled
2	1	CLKREQB#	CLKREQB# Controls SRC6 0 = Not controlled, 1 = Controlled
1	0	CLKREQB#	CLKREQB# Controls SRC5 0 = Not controlled, 1 = Controlled
0	0	CLKREQB#	CLKREQB# Controls SRC4 0 = Not controlled, 1 = Controlled

Byte 10: Dynamic Frequency Register4

Bit	@Pup	Name	Description
7	0	Reserved	Reserved
6	1	Reserved	Reserved
5	1	Diff_VOUT2	Differential Output Level Setting Diff_VOUT [2:0] 111 = 0.96V 110 = 0.93V 101 = 0.90V default 100 = 0.86V 011 = 0.82V 010 = 0.77V 001 = 0.71V 000 = 0.63V
4	0	Diff_VOUT1	
3	1	Diff_VOUT0	
2	0	Reserved	Reserved
1	0	SMSW_SEL_Bypass	Smooth switch on/off 0 = On 1 = Off
0	0	SMSW_SEL	Smooth Switch Select 0 = Select CPU_PLL (PLL1). 1 = Select ATIG_PLL (PLL2)

Byte 11: WDT System Register

Bit	@Pup	Name	Description
7	0	Recovery_Frequency	This bit allows selection of the frequency setting that the clock will be restored to once the system is rebooted 0 = Use HW settings, 1 = Recovery N[8:0]
6	0	Reserved	Reserved
5	1	Reserved	Reserved
4	0	Reserved	Reserved
3	0	Reserved	Reserved
2	0	Reserved	Reserved
1	0	Reserved	Reserved
0	0	Reserved	Reserved

Byte 12: CPU DAF Register1

Bit	@Pup	Name	Description
7	0	CPU_DAF_N[7]	If Prog_CPU_EN is set, the values programmed in CPU_DAF_N[8:0] and CPU_DAF_M[6:0] will be used to determine the CPU output frequency. The setting of the FS_Override bit determines the frequency ratio for CPU and other output clocks. When it is cleared, the same frequency ratio stated in the Latched FS[D:A] register will be used. When it is set, the frequency ratio stated in the FSEL[3:0] register will be used.
6	0	CPU_DAF_N[6]	
5	0	CPU_DAF_N[5]	
4	0	CPU_DAF_N[4]	
3	0	CPU_DAF_N[3]	
2	0	CPU_DAF_N[2]	
1	0	CPU_DAF_N[1]	
0	0	CPU_DAF_N[0]	

Byte 13: CPU DAF Register2

Bit	@Pup	Name	Description
7	0	CPU_DAF_N[8]	If Prog_CPU_EN is set, the values programmed in CPU_DAF_N[8:0] and CPU_DAF_M[6:0] will be used to determine the CPU output frequency. The setting of the FS_Override bit determines the frequency ratio for CPU and other output clocks. When it is cleared, the same frequency ratio stated in the Latched FS[D:A] register will be used. When it is set, the frequency ratio stated in the FSEL[3:0] register will be used.
6	0	CPU_DAF_M[6]	
5	0	CPU_DAF_M[5]	
4	0	CPU_DAF_M[4]	
3	0	CPU_DAF_M[3]	
2	0	CPU_DAF_M[2]	
1	0	CPU_DAF_M[1]	
0	0	CPU_DAF_M[0]	

Byte 14: ATIG DAF Register1

Bit	@Pup	Name	Description
7	0	ATIG_DAF_N[7]	If Prog_ATIG_EN is set, the values programmed in ATIG_DAF_N[8:0] will be used to determine the ATIG output frequency.
6	0	ATIG_DAF_N[6]	
5	0	ATIG_DAF_N[5]	
4	0	ATIG_DAF_N[4]	
3	0	ATIG_DAF_N[3]	
2	0	ATIG_DAF_N[2]	
1	0	ATIG_DAF_N[1]	
0	0	ATIG_DAF_N[0]	

Byte 15: WDT Recovery Register

Bit	@Pup	Name	Description
7	0	RECOVERY_N[7]	Used when RESET_IN# is asserted or the Watchdog timer times out. This will be the safe value or last known good frequency of the CPU. It is set by the user before engaging in any overclocking exercise. M values revert to those set by the FS[C:A] pins
6	0	RECOVERY_N[6]	
5	0	RECOVERY_N[5]	
4	0	RECOVERY_N[4]	
3	0	RECOVERY_N[3]	
2	0	RECOVERY_N[2]	
1	0	RECOVERY_N[1]	
0	0	RECOVERY_N[0]	

Byte 16: Overclocking Support Register

Bit	@Pup	Name	Description
7	0	ATIG_N8	ATIG DAF bit N8
6	1	Reserved	Reserved
5	0	Reserved	Reserved
4	0	Prog_SRC_EN	Enables the setting of SRC_PLL (PLL3) N values via byte 8 0 = Disable, 1 = Enable
3	0	Prog_ATIG_EN	Enables the setting of ATIG_PLL (PLL2) N values via byte 17 0 = Disable, 1 = Enable
2	0	Prog_CPU_EN	Enables the setting of CPU_PLL (PLL1) M and N values via byte 15 and 16 0 = Disable, 1 = Enable
1	0	Reserved	Reserved
0	0	Recovery_N8	CPU Safe recovery bit 8 for RESET_IN and Watchdog timer timeout.

Table 4. Crystal Recommendations

Frequency (Fund)	Cut	Loading	Load Cap	Drive (max.)	Shunt Cap (max.)	Motional (max.)	Tolerance (max.)	Stability (max.)	Aging (max.)
14.31818 MHz	AT	Parallel	20 pF	0.1 mW	5 pF	0.016 pF	35 ppm	30 ppm	5 ppm

Crystal Recommendations

The CY28RS680 requires a Parallel Resonance Crystal. Substituting a series resonance crystal will cause the CY28RS680 to operate at the wrong frequency and violate the ppm specification. For most applications there is a 300-ppm frequency shift between series and parallel crystals due to incorrect loading.

Crystal Loading

Crystal loading plays a critical role in achieving low ppm performance. To realize low ppm performance, the total capacitance the crystal will see must be considered to calculate the appropriate capacitive loading (CL).

Figure 1 shows a typical crystal configuration using the two trim capacitors. An important clarification for the following discussion is that the trim capacitors are in series with the crystal not parallel. It is a common misconception that load capacitors are in parallel with the crystal and should be approximately equal to the load capacitance of the crystal. This is not true.

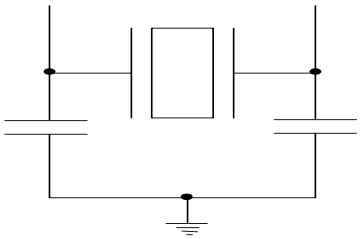


Figure 1. Crystal Capacitive Clarification

Calculating Load Capacitors

In addition to the standard external trim capacitors, trace capacitance and pin capacitance must also be considered to correctly calculate crystal loading. As mentioned previously, the capacitance on each side of the crystal is in series with the crystal. This means the total capacitance on each side of the crystal must be twice the specified crystal load capacitance (CL). While the capacitance on each side of the crystal is in series with the crystal, trim capacitors (Ce1,Ce2) should be calculated to provide equal capacitive loading on both sides.

Use the following formulas to calculate the trim capacitor values for Ce1 and Ce2.

Load Capacitance (each side)

$$Ce = 2 * CL - (Cs + Ci)$$

Total Capacitance (as seen by the crystal)

$$CLe = \frac{1}{\left(\frac{1}{Ce1 + Cs1 + Ci1} + \frac{1}{Ce2 + Cs2 + Ci2}\right)}$$

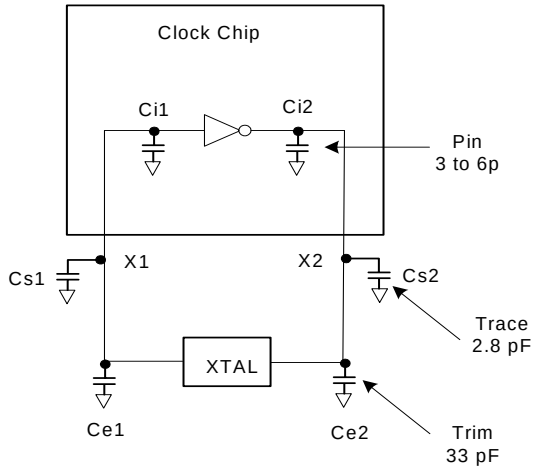


Figure 2. Crystal Loading Example

CL.....Crystal load capacitance

CLe..... Actual loading seen by crystal using standard value trim capacitors

Ce..... External trim capacitors

Cs.....Stray capacitance (terraced)

Ci .....Internal capacitance (lead frame, bond wires etc.)

CLK_REQ[A:C]# Description

The CLKREQ#[A:C] signals are active LOW inputs used for clean stopping and starting of selected SRC outputs. The CLKREQ# signal is a debounced signal in that its state must remain unchanged during two consecutive rising edges of DIFC to be recognized as a valid assertion or deassertion. (The assertion and deassertion of this signal is absolutely asynchronous.)

CLK_REQ[A:C]# Assertion

The impact of asserting the CLKREQ#[A:C] pins is that all DIF outputs that are set in the control registers to stoppable via assertion of CLKREQ#[A:C] are to be stopped after their next transition. The final state of all stopped DIF signals is tri-state; both SRCT clock and SRCC clock outputs will be driven tri-state.

CLK_REQ[A:C]# Deassertion

All differential outputs that were stopped are to resume normal operation in a glitch free manner. The maximum latency from the deassertion to active outputs is between 2 and 6 SRC clock periods (2 clocks are shown) with all SRC outputs resuming simultaneously.

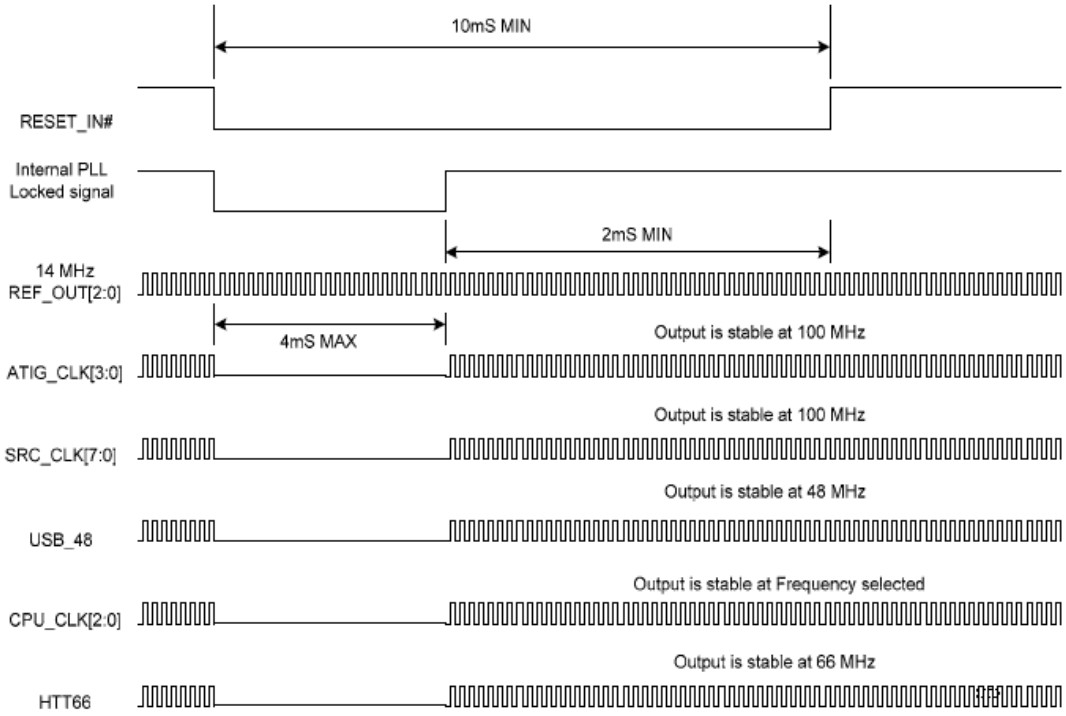


Figure 3. RESET_IN# Assertion/Deassertion Waveform

RESET_IN# Assertion

RESET_IN# is a negative edge triggered signal. When asserted, all PLLs will revert back to a safe default frequency. The clock output will be allowed to turn off for a maximum of 4 ms. After this time the PLLs will output a locked clock at a preselected safe frequency. The safe frequency is either based upon the power on reset default values or upon the value stored in the safe frequency register. The safe frequency register is accessible via SMBUS (Bytes 18 & 19). The clock outputs must be stable at the correct safe frequency at least 2 ms before the deassertion of RESET_IN#.

Dial-A-Frequency (CPU. SRC and ATIG)

Figure 1 shows a classical PLL block circuit. The PLL is designed to allow overclocking capabilities. The RS680 implement a Spectra Linear feature called Dial-A-Frequency (DAF). This feature allows users to overclock their systems by slowly stepping up the CPU, SRC, or ATIG frequency. When the programmable output frequency feature is enabled, the CPU, SRC and ATIG frequencies are determined by the following equation:

Fout= G * N/M or Fout = G2 * N, where G2 = G/M

or

Fout = (N*Fout)/(M*O)

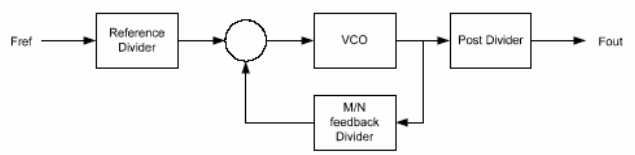


Figure 1 - Classical PLL

'N' and 'M' are the values programmed in Programmable Frequency Select N-Value Register and M-Value Register, respectively. 'G' stands for the PLL Gear Constant, which is determined by the programmed value of FS[C:A]. See tables below for the Gear Constant for each Frequency selection. The SRC and ATIG only allow the user control of the N register; the M value is fixed and documented in the tables below. The user may change only the N value if required. In this mode, the user writes the desired N value into the DAF I2C registers. CPU overclocking allows the user to change both the M and N values.

Note: For the CPU overclocking, the user cannot change only the M value but must change both the M and the N values at the same time, if they require a change to the M value.

Associated Register Bits

Prog_CPU_EN - This bit enables CPU DAF mode. By default, it is not set. When set, the operating frequency is determined by the values entered into the CPU_DAF_N register. Note: The CPU_DAF_N and M registers must contain valid values before Prog_CPU_EN is set. Default = 0, (No DAF).

CPU_DAF_N - There are nine bits (for 512 values) to linearly change the CPU frequency (limited by VCO range). Default =0, (0000). The allowable values for N are detailed in the frequency select table.

CPU_DAF_M - There are 7 bits (for 128 values) to linearly change the CPU frequency (limited by VCO range). Default =0. The allowable values for M are detailed in the frequency select table.

Prog_SRC_EN -This bit enables SRC DAF mode. By default, it is not set. When set, the operating frequency is determined by the values entered into the SRC_DAF_N register. Note: The SRC_DAF_N register must contain valid values before Prog_SRC_EN is set. Default = 0, (No DAF).

SRC_DAF_N - There are nine bits (for 512 values) to linearly change the SRC frequency (limited by VCO range). However, it should be noted that the two MSB are hardwired and only N[7:0] are required to be program in the SMBus. Default =0, (0000). The allowable values for N are detailed in the frequency select table.

Prog_ATIG_EN -This bit enables ATIG DAF mode. By default, it is not set. When set, the operating frequency is determined by the values entered into the ATIG_DAF_N register. Note: The SRC_DAF_N register must contain valid values before Prog_ATIG_EN is set. Default = 0, (No DAF

ATIG_DAF_N - There are eight bits (for 256 values) to linearly change the ATIG frequency (limited by VCO range). Default = 0, (0000). The allowable values for N are detailed in the frequency select table.

Software Frequency Select

This mode allows the user to select the CPU output frequencies using the Software Frequency select bits in the SMBUS register. FSEL - There are three bits (for 8 combinations) to select predetermined CPU frequencies from a table. The table selections are detailed in.

Smooth Switching

The device contains one smooth switch circuit, which is shared by the CPU PLL and SRC PLL. The smooth switch circuit ensures that when the output frequency changes by overclocking, the transition from the old frequency to the new frequency is a slow, smooth transition containing no glitches. The rate of change of output frequency when using the smooth switch circuit is less than 1 MHz/0.667 µs. The frequency overshoot and undershoot will be less than 2%.

The smooth switch circuit can be assigned auto or manual mode. In auto mode, the clock generator will assign smooth

switch automatically when the PLL will perform overclocking. For manual mode, the smooth switch circuit can be assigned to either PLL via SMBUS. By default the smooth switch circuit is set to auto mode. Either PLL can still be overclocked when it does not have control of the smooth switch circuit, but it is not guaranteed to transition to the new frequency without large frequency glitches.

Note: Do not enable overclocking and change the N values of both PLLs in the same SMBUS block write and use smooth switch mechanism on spread spectrum on/off.

Table 5. Overclocking Table of the RS680

		SMB Reg Bits	**Pins**	**Comments**
CPU Overclocking	**Function**			
	Dial-A-Freq	Byte10<0> - Smooth Switch Select Byte13<7>,Byte12<7:0> - CPU_DAF_N[8:0] Byte13<6:0> - CPU_DAF_M[6:0] Byte16<2> - Prog_CPU_EN	None	Refer to the Table-3 for the M and N values that could be loaded into the DAF registers.
	FSEL	FSEL_[C:A] -Byte3<2:0> - ***SW*** Frequency Select	FSC, FSB, FSA	Refer to the Table-3 CPU OC
HTT Overclocking				Overclocked by the same % as the CPU
ATIG Overclocking	Dial-A-Freq	Byte16<7>,Byte14<7:0> ATIG_DAF_N[8:0] Byte16<3> - Prog_ATIG_EN To support 100% Overclocking the appropriate band has to be chosen using: ATIG_OC_SEL1 -Byte3<4> ATIG_OC_SEL0 -Byte3<3>	None	Refer to the Table-4 ATIG OC SEL1 & SEL0 I2C bits have been implemented as the FSE pin and PCI_OC_SEL on the b30m08a (Lakeport)
SRC Overclocking	Dial-A-Freq	Byte8<7:0> - SRC_DAF_N[7:0] Byte16<4> - Prog_SRC_EN	None	Refer to the Table-5 SRC OC

Table 6.) Default Divider for all differential clocks

Clock	M Divider	N Divider	O Divider
CPU	60	200	4
ATIG	60	200	8
SRC	8	447	8

Table 7.) Frequency Table for the CPU Clock (CPU PLLPLL)

FSC	FSB	FSA	CPU Actual (MHz)	N Actual	N Max	M | Gear Ratio
0	0	0	266.67	200	255	60 | 80
0	0	1	133.33	200	279	60 | 40
0	1	0	200	200	280	60 | 60
0	1	1	166.67	175	252	63 | 60
1	0	0	333.33	175	247	63 | 120
1	0	1	100			
1	1	0	400	200	260	60 | 120

Table 8.)Frequency Table for the ATIG Clock (PCIEX PLL)

Freq Band	SEL1	SEL0	ATIG o/p (MHz)	Range of N	M | O(out div) Fref = 240MHz
1	0	0	111.33 -167	167 -250	60 | 6
2	1	0	100 -125	200 -250	60 | 8
3	X	1	166 -256	167 -256	60 | 4

Table 9.)Frequency Table for the SRC Clock PLLPLL

S.No	N	Fsrc (MHz)	N-Binary[7:0]	Comments
1	376	84	101111000	**Fref = 14.31818MHz M = 8 | O = 8**
2	380	85	101111100	
3	384	86	110000000	
4	389	87	110000101	
5	393	88	110001001	
6	398	89	110001110	
7	402	90	110010010	
8	407	91	110010111	
9	411	92	110011011	
10	416	93	110100000	
11	420	94	110100100	
12	425	95	110101001	
13	429	96	110101101	
14	434	97	110110010	
15	438	98	110110110	
16	443	99	110111011	
17	447	100	110111111	
18	452	101	111000100	
19	456	102	111001000	
20	460	103	111001100	
21	465	104	111010001	
22	469	105	111010101	
23	474	106	111011010	
24	478	107	111011110	
25	483	108	111100011	
26	487	109	111100111	
27	492	110	111101100	
28	496	111	111110000	
29	501	112	111110101	
30	505	113	111111001	
31	510	114	111111110	

NOTE: N[8] bit is hardwired to a logic "1".
The SMBus register only requires changes to N[7:0]

AC Electrical Specifications

Parameter	Description	Condition	Min.	Max.	Unit
Crystal					
T_{DC}	XIN Duty Cycle	The device will operate reliably with input duty cycles up to 30/70 but the REF clock duty cycle will not be within specification	47.5	52.5	%
T_{PERIOD}	XIN Period	When XIN is driven from an external clock source	69.841	71.0	ns
T_R / T_F	XIN Rise and Fall Times	Measured between $0.3V_{DD}$ and $0.7V_{DD}$	–	10.0	ns
T_{CCJ}	XIN Cycle to Cycle Jitter	As an average over 1-µs duration	–	500	ps
L_{ACC}	Long-term Accuracy	Over 150 ms	–	300	ppm
CPU Outputs					
T_R / T_F	Output Slew Rate	Measured @ test load using VOCM ±400 mV, 0.85 to 1.65	2	7	V/ns
V_{DIFF}	Differential Voltage	Measured at load single ended	0.4	2.3	V
L_{ACC}	Long Term Accuracy		–300	300	ppm
T_{SKEW}	Any CPU to CPU Clock Skew	Measured at crossing point V_{OX}	–	250	ps
ΔV_{DIFF}	Change in VDIFF_DC Magnitude	Measured at load single ended	–150	150	mV
V_{CM}	Common Mode Voltage	Measured at load single ended	0.984	1.45	V
ΔV_{CM}	Change in V_{CM}	Measured at load single ended	–200	200	mV
T_{DC}	Duty Cycle	Measured at V_{OX}	45	53	%
T_{JCYC}	Cycle to Cycle Jitter	Measured at V_{OX}	0	85	ps
SRC					
T_{DC}	SRCT and SRCC Duty Cycle	Measured at crossing point V_{OX}	45	55	%
T_{PERIOD}	100 MHz SRCT and SRCC Period	Measured at crossing point V_{OX}	9.997001	10.00300	ns
$T_{PERIODSS}$	100 MHz SRCT and SRCC Period, SSC	Measured at crossing point V_{OX}	9.997001	10.05327	ns
$T_{PERIODAbs}$	100 MHz SRCT and SRCC Absolute Period	Measured at crossing point V_{OX}	10.12800	9.872001	ns
$T_{PERI-ODSSAbs}$	100 MHz SRCT and SRCC Absolute Period, SSC	Measured at crossing point V_{OX}	9.872001	10.17827	ns
T_{SKEW}	Any SRCT/C to SRCT/C Clock Skew	Measured at crossing point V_{OX}	–	250	ps
T_{CCJ}	SRCT/C Cycle to Cycle Jitter	Measured at crossing point V_{OX}	–	125	ps
L_{ACC}	SRCT/C Long Term Accuracy	Measured at crossing point V_{OX}	–300	300	ppm
T_R / T_F	SRCT and SRCC Rise and Fall Times	Measured differentially from ±150mV	2.5	8	V/ns
T_{RFM}	Rise/Fall Matching	Determined as a fraction of $2*(T_R - T_F)/(T_R + T_F)$	–	20	%
ΔT_R	Rise TimeVariation		–	125	ps
ΔT_F	Fall Time Variation		–	125	ps
V_{HIGH}	Voltage High	Measured singled-ended, including overshoot		1.15	V
V_{LOW}	Voltage Low	Measured singled-ended, including undershoot	–0.3	–	V
V_{OX}	Crossing Point Voltage at 0.7V Swing		250	550	mV
ATIG					
T_{DC}	ATIGT and ATIGC Duty Cycle	Measured at crossing point V_{OX}	45	55	%
T_{PERIOD}	100 MHz ATIGT and ATIGC Period	Measured at crossing point V_{OX}	9.997001	10.00300	ns
$T_{PERIODSS}$	100 MHz ATIGT and ATIGC Period, SSC	Measured at crossing point V_{OX}	9.997001	10.05327	ns

AC Electrical Specifications (continued)

Parameter	Description	Condition	Min.	Max.	Unit
$T_{PERIODAbs}$	100 MHz ATIGT and ATIGC Absolute Period	Measured at crossing point V_{OX}	10.12800	9.872001	ns
$T_{PERI-ODSSAbs}$	100 MHz ATIGT and ATIGC Absolute Period, SSC	Measured at crossing point V_{OX}	9.872001	10.17827	ns
T_{SKEW}	Any ATIGT/C to ATIGT/C Clock Skew	Measured at crossing point V_{OX}	–	250	ps
T_{CCJ}	ATIGT/C Cycle to Cycle Jitter	Measured at crossing point V_{OX}	–	125	ps
L_{ACC}	ATIGT/C Long Term Accuracy	Measured at crossing point V_{OX}	–300	300	ppm
T_R / T_F	ATIGT and ATIGC Rise and Fall Times	Measured differentially from ±150mV	2.5	8	V/ns
T_{RFM}	Rise/Fall Matching	Determined as a fraction of $2*(T_R – T_F)/(T_R + T_F)$	–	20	%
ΔT_R	Rise Time Variation		–	125	ps
ΔT_F	Fall Time Variation		–	125	ps
V_{HIGH}	Voltage High	Measured singled-ended, including overshoot		1.15	V
V_{LOW}	Voltage Low	Measured singled-ended, including undershoot	–0.3	–	V
V_{OX}	Crossing Point Voltage at 0.7V Swing		250	550	mV
HTT66 HyperTransport Output					
F66	Operating Frequency			66.67	MHz
T_{DC}	Duty Cycle	Measured at 1.5V	45	55	%
T_R / T_F	Slew Rate	Measured at 20% and 60%	0.9	8.25	V/ns
T_{CCJ}	Cycle to Cycle jitter	Measured at 1.5V		250	ps
T_{LTJ}	Long Term jitter	Measured at 1.5V		1000	ps
USB					
T_{DC}	Duty Cycle	Measurement at 1.5V	45	55	%
T_{PERIOD}	Period	Measurement at 1.5V	20.83229	20.83437	ns
$T_{PERIODAbs}$	Absolute Period	Measurement at 1.5V	20.48125	21.18542	ns
T_{HIGH}	USB High Time	Measurement at 2.4V	8.094	10.256	nS
T_{LOW}	USB Low Time	Measurement at 0.4V	7.694	10.250	nS
T_R / T_F	Rise and Fall Times	Measured between 0.8V and 2.0V	1.0	3.5	V/ns
T_{CCJ}	Cycle to Cycle Jitter	Measurement at 1.5V	–	150	ps
L_{ACC}	USB Long Term Accuracy	Measurement at 1.5V	–50	50	ppm
T_{LTJ}	Long Term Jitter	Measurement at 1.5V@1 µs	–	1000	ps
REF					
T_{DC}	REF Duty Cycle	Measurement at 1.5V	45	55	%
T_{PERIOD}	REF Period	Measurement at 1.5V	69.8203	69.8622	ns
$T_{PERIODAbs}$	REF Absolute Period	Measurement at 1.5V	68.82033	70.86224	ns
T_R / T_F	REF Rise and Fall Times	Measured between 0.8V and 2.0V	1.0	4.0	V/ns
T_{CCJ}	REF Cycle to Cycle Jitter	Measurement at 1.5V	–	250	ps
T_{LTJ}	Long Term Jitter	Measurement at 1.5V@10 µs	–	250	ps
ENABLE/DISABLE and SET-UP					
T_{STABLE}	Clock Stabilization from Power Up		–	1.8	ms
T_{SS}	Stopclock Set-up Time		10.0	–	ns
T_{SH}	Stopclock Hold Time		0	–	ns

Test and Measurement Set-up

For HT66, PCI, USB Single-ended Signals and Reference

The following diagrams show the test load configurations for the single-ended PCI, USB, and REF output signals.

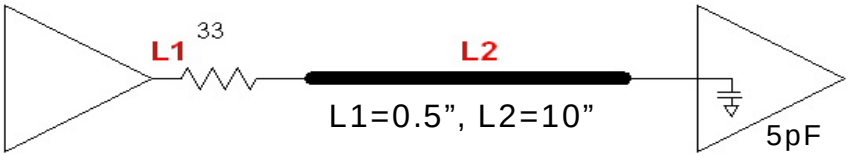


Figure 4. Single-ended HT66/PCI/USB Load Configuration

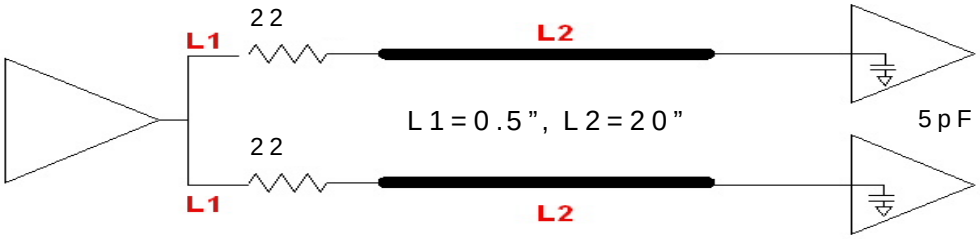


Figure 5. Single-ended REF Load Configuration

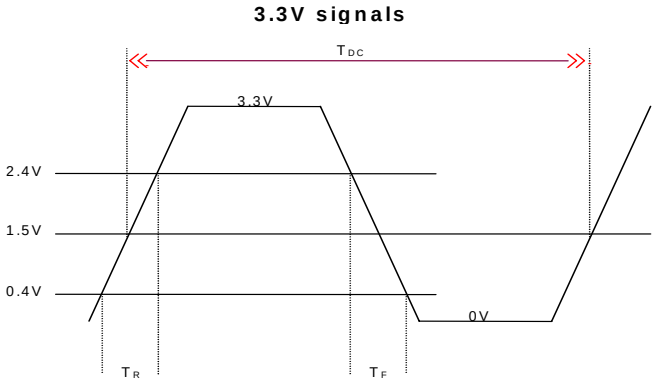
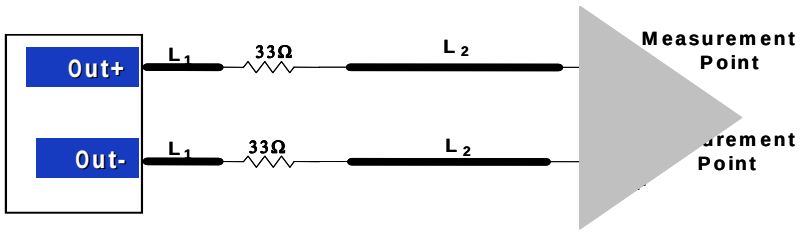


Figure 6. Single-ended Output Signals (for AC Parameters Measurement)

For SRC/ATIG Output Signals

The following diagram shows the test load configuration for the differential SRC/ATIG outputs.



L1=0.5", L2=10"

Figure 7. 0.7V Load Configuration

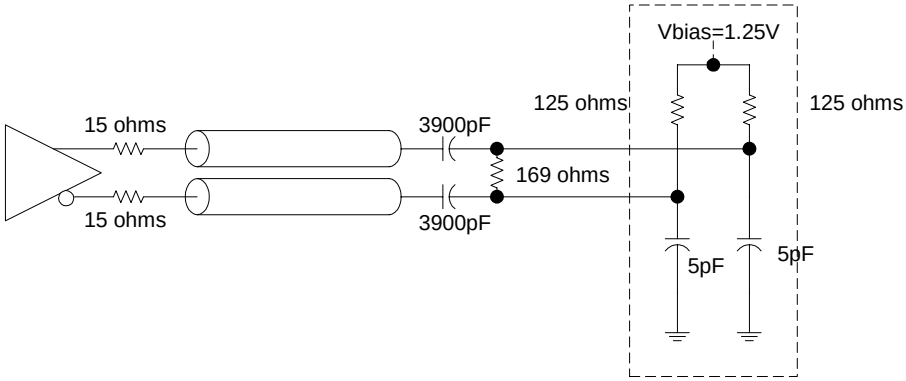


Figure 8. CPU Output Load Configuration

Ordering Information

Part Number	Package Type	Product Flow
Lead-free		
CY28RS680ZXC	64-pin TSSOP	Commercial, 0° to 70°C
CY28RS680ZXCT	64-pin TSSOP – Tape and Reel	Commercial, 0° to 70°C

Package Drawing and Dimensions

64-Lead Thin Shrunk Small Outline Package (6 mm x 17 mm) Z64