CY28RS680-2

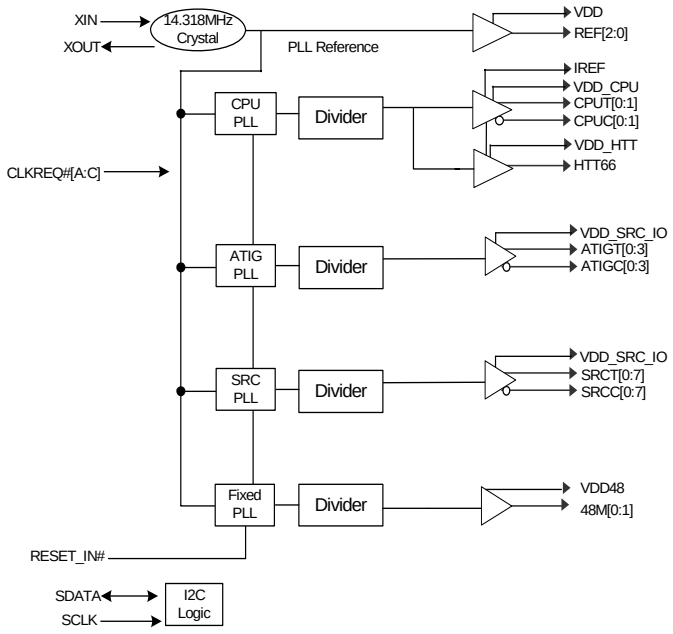
Clock Generator for ATI® RS5XX/6XX Chipsets

Features

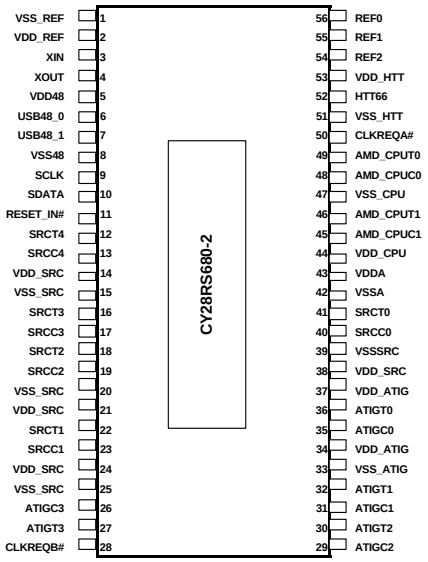
- Supports AMD® CPU
- Selectable CPU frequencies
- 200 MHz differential CPU clock pairs (100% over/ 50% under clocked)
- 100 MHz differential ATI Graphics clocks (100% over/10% under clocked)
- 100 MHz differential SRC clocks (10% over/under clocked)
- 48 MHz USB clock
- 66 MHz HyperTransport™ clock
- I^2C support with readback capabilities
- Ideal Lexmark Spread Spectrum profile for maximum electromagnetic interference (EMI) reduction
- 3.3V power supply
- 56-pin TSSOP/SSOP packages

CPU	SRC	HTT66	ATIG	REF	USB_48
x2	x5	x1	X4	x 3	x 2

Block Diagram



Pin Configuration



56 TSSOP/SSOP

2200 Laurelwood Road, Santa Clara, CA 95054 Tel:(408) 855-0555 Fax:(408) 855-0550 www.SpectraLinear.com

Pin Description

Pin No.	Name	Type	Description
1	VSS_REF	PWR	GND for REF, XTAL
2	VDD_REF	PWR	3.3V power supply for REF, XTAL
3	XIN	I	14.318 MHz Crystal Input
4	XOUT	O	14.318 MHz Crystal Output
5	VDD_48	PWR	3.3V power supply for USB outputs
6, 7	USB_48 [1:0]	O, SE	48 MHz clock output. Intel® Type-3A buffer.
8	VSS_48	GND	Ground for USB outputs
9	SCLK	I,PU	SMBus-compatible SCLOCK.This pin has an internal pull-up, but is tri-stated in power-down.
10	SDATA	I/O,PU	SMBus-compatible SDATA.This pin has an internal pull-up, but is tri-stated in power-down.
11	RESET_IN#	I, PU	3.3V LVTTL Input (Negative Edge Triggered) When this pin is asserted LOW, all PLLs will transition to a safe default frequency. This may be the POR defaults or a safe value stored in SMBUS registers.
12, 13	SRCT/C[4]	O, DIF	100 MHz differential serial reference clock. Intel Type-SR buffer. (10% overclocking support through SMBUS)
14	VDD_SRC	PWR	3.3V power supply for SRC outputs
15	VSS_SRC	GND	Ground for SRC outputs
16, 17, 18, 19	SRCT/C[3:2]	O, DIF	100 MHz differential serial reference clock. Intel Type-SR buffer. (10% overclocking support through SMBUS)
20	VSS_SRC	GND	Ground for SRC outputs
21	VDD_SRC	PWR	3.3V power supply for SRC outputs
22, 23	SRCT/C1	O, DIF	100 MHz differential serial reference clock. Intel Type-SR buffer. (10% overclocking support through SMBUS)
24	VDD_SRC	PWR	3.3V power supply for SRC outputs
25	VSS_SRC	GND	Ground for SRC outputs
26,27	ATIGT/C3	O, DIF	Differential Selectable serial reference clock. Intel Type-SR buffer. Includes 50% overclock support through SMBUS
28	CLKREQ#B	I, SE, PU	Output Enable control for SRCT/C. Output enable control required by Minicard specification. This pin has an internal pull up. 0 = selected SRC output is enabled. 1 = selected SRC output is disabled.
29, 30, 31, 32	ATIGT/C[2:1]	O, DIF	Differential Selectable serial reference clock. Intel Type-SR buffer. Includes 50% overclock support through SMBUS
33	VSS_ATIG	GND	Ground for ATIG outputs
34, 37	VDD_ATIG	PWR	3.3V power supply for ATIG outputs
35, 36	ATIGT/C0	O, DIF	Differential Selectable serial reference clock. Intel Type-SR buffer. Includes 50% overclock support through SMBUS
38	VDD_SRC	PWR	3.3V power supply for SRC outputs
39	VSS_SRC	GND	Ground for SRC outputs
40,41	SRCT/C0	O, DIF	100 MHz differential serial reference clock. Intel Type-SR buffer. (10% overclocking support through SMBUS)
42	VSSA	GND	Analog Ground
43	VDDA	PWR	3.3V Analog Power for PLLs
44	VDD_CPU	PWR	3.3V power supply for CPU outputs
45, 46, 48, 49	CPUT/C[1:0]	O, DIF	Differential CPU clock output. Intel Type-SR buffer.
47	VSS_CPU	GND	Ground for CPU outputs
50	CLKREQ#A	I, SE, PU	Output Enable control for SRCT/C. Output enable control required by Minicard specification. This pin has an internal pull-up. 0 = selected SRC output is enabled. 1 = selected SRC output is disabled.

Pin Description

Pin No.	Name	Type	Description
51	VSS_HTT	PWR	Ground for HyperTransport outputs
52	HTT66	O, SE	66 MHz clock output. Intel Type-5 buffer.
53	VDD_HTT	PWR	3.3V power supply for HyperTransport outputs
54, 55, 56	REF[2:0]	O, SE	14.318-MHz REF clock output. Intel Type-5 buffer.

Serial Data Interface

To enhance the flexibility and function of the clock synthesizer, a two-signal serial interface is provided. Through the Serial Data Interface, various device functions, such as individual clock output buffers, can be individually enabled or disabled. The registers associated with the Serial Data Interface initialize to their default setting upon power-up, and therefore use of this interface is optional. Clock device register changes are normally made upon system initialization, if any are required. The interface cannot be used during system operation for power management functions.

Data Protocol

The clock driver serial protocol accepts byte write, byte read, block write, and block read operations from the controller. For block write/read operation, the bytes must be accessed in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after any complete byte has been transferred. For byte write and byte read operations, the system controller can access individually indexed bytes. The offset of the indexed byte is encoded in the command code, as described in *Table 1*.

The block write and block read protocol is outlined in *Table 2* while *Table 3* outlines the corresponding byte write and byte read protocol. The slave receiver address is 11010010 (D2h).

Table 1. Command Code Definition

Bit	Description
7	0 = Block read or block write operation, 1 = Byte read or byte write operation
(6:5)	Chip select address, set to ‘00’ to access device
(4:0)	Byte offset for byte read or byte write operation. For block read or block write operations, these bits should be '00000'

Table 2. Block Read and Block Write Protocol

Block Write Protocol		Block Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
8:2	Slave address – 7 bits	8:2	Slave address – 7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
18:11	Command Code – 8 bits	18:11	Command Code – 8 bits
19	Acknowledge from slave	19	Acknowledge from slave
27:20	Byte Count – 8 bits	20	Repeat start
28	Acknowledge from slave	27:21	Slave address – 7 bits
36:29	Data byte 1 – 8 bits	28	Read = 1
37	Acknowledge from slave	29	Acknowledge from slave
45:38	Data byte 2 – 8 bits	37:30	Byte Count from slave – 8 bits
46	Acknowledge from slave	38	Acknowledge
....	Data Byte /Slave Acknowledges	46:39	Data byte 1 from slave – 8 bits
....	Data Byte N – 8 bits	47	Acknowledge
....	Acknowledge from slave	55:48	Data byte 2 from slave – 8 bits
....	Stop	56	Acknowledge
		....	Data bytes from slave / Acknowledge
		....	Data Byte N from slave – 8 bits
		....	NOT Acknowledge

Table 3. Byte Read and Byte Write Protocol

Byte Write Protocol		Byte Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
8:2	Slave address – 7 bits	8:2	Slave address – 7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
18:11	Command Code – 8 bits	18:11	Command Code – 8 bits
19	Acknowledge from slave	19	Acknowledge from slave
27:20	Data byte – 8 bits	20	Repeated start
28	Acknowledge from slave	27:21	Slave address – 7 bits
29	Stop	28	Read
		29	Acknowledge from slave
		37:30	Data from slave – 8 bits
		38	NOT Acknowledge
		39	Stop

Control Registers

Byte 0: Output Enable Register 0

Bit	@Pup	Name	Description
7	1	Reserved	Reserved
6	1	Reserved	Reserved
5	1	Reserved	Reserved
4	1	SRC[T/C]4	SRC[T/C]4 Output Enable 0 = Disable (Hi-Z), 1 = Enable
3	1	SRC[T/C]3	SRC[T/C]3 Output Enable 0 = Disable (Hi-Z), 1 = Enable
2	1	SRC[T/C]2	SRC[T/C]2 Output Enable 0 = Disable (Hi-Z), 1 = Enable
1	1	SRC[T/C]1	SRC[T/C]1 Output Enable 0 = Disable (Hi-Z), 1 = Enable
0	1	SRC [T/C]0	SRC[T/C]0 Output Enable 0 = Disable (Hi-Z), 1 = Enable

Byte 1: Output Enable Register 1

Bit	@Pup	Name	Description
7	1	Reserved	Reserved
6	1	Reserved	Reserved
5	1	ATIG[T/C]3	ATIG[T/C]3 Output Enable 0 = Disable (Hi-Z), 1 = Enable
4	1	ATIG[T/C]2	ATIG[T/C]2 Output Enable 0 = Disable (Hi-Z), 1 = Enable
3	1	ATIG[T/C]1	ATIG[T/C]1 Output Enable 0 = Disable (Hi-Z), 1 = Enable
2	1	ATIG[T/C]0	ATIG[T/C]0 Output Enable 0 = Disable (Hi-Z), 1 = Enable
1	1	Reserved	Reserved
0	1	CPU[T/C]1	CPU[T/C]1 Output Enable 0 = Disable (Hi-Z), 1 = Enable

Byte 2: Output Enable Register 2

Bit	@Pup	Name	Description
7	1	CPU[T/C]0	CPU[T/C]0 Output Enable 0 = Disable (Hi-Z), 1 = Enable
6	1	USB_48_1	USB_48_1 Output Enable 0 = Disable (Hi-Z), 1 = Enable
5	1	USB_48_0	USB_48_0 Output Enable 0 = Disable (Hi-Z), 1 = Enable
4	1	REF_2	REF_2 Output Enable 0 = Disable (Hi-Z), 1 = Enable
3	1	REF_1	REF_1 Output Enable 0 = Disable (Hi-Z), 1 = Enable
2	1	REF_0	REF_0 Output Enable 0 = Disable (Hi-Z), 1 = Enable
1	1	HTT66	HTT66 Output Enable 0 = Disable (Hi-Z), 1 = Enable
0	0	CPU Spread Enable	CPU_PLL (PLL1) Spread Spectrum Enable 0= Spread Off, 1 = Spread On

Byte 3: SW_FREQ Selection Register

Bit	@Pup	Name	Description
7	0	Reserved	Reserved
6	0	Reserved	Reserved
5	0	Reserved	Reserved
4	1	ATIG_OC_SEL1	
3	0	ATIG_OC_SEL0	
2	0	FSEL_C	SW Frequency Selection Bits
1	0	FSEL_B	
0	0	FSEL_A	

SEL1	SEL0	ATIG Output	N
0	0	111.33–167 MHz	167–250
1	0	100–125 MHz	200–250
X	1	166–256 MHz	167–256

Byte 4: Spread Spectrum Control Register

Bit	@Pup	Name	Description
7	0	CPU_SS1	CPU(PLL1) Spread Spectrum Selection 00: –0.5% (peak to peak) 01: ±0.25% (peak to peak) 10: –1.0% (peak to peak) 11: ±0.5% (peak to peak)
6	0	CPU_SS0	
5	0	ATIG_SS0	ATIG(PLL2) Spread Spectrum Selection 00: –0.5% (peak to peak) 01: –1.0% (peak to peak)
4	0	ATIG_SS_OFF	ATIG_PLL (PLL2) Spread Spectrum Enable 0 = Spread Off, 1 = Spread On
3	0	SRC_SS_OFF	SRC_PLL (PLL3) Spread Spectrum Enable 0 = Spread Off, 1 = Spread On
2	0	USB48	USB48 Output Drive Strength 0 = 1x, 1 = 2x
1	0	Reserved	Reserved
0	0	REF	REF Output Drive Strength 0 = 1X, 1 = 2x

Byte 5: System Configuration Register

Bit	@Pup	Name	Description
7	0	Reserved	Reserved
6	0	Reserved	Reserved
5	0	Reserved	Reserved
4	0	Reserved	Reserved
3	0	Reserved	Reserved
2	0	Reserved	Reserved
1	1	Reserved	Reserved
0	0	CLKREQA#	CLKREQA# Controls SRC0 0 = Not controlled, 1 = Controlled

Byte 6: Revision and Device ID

Bit	@Pup	Name	Description
7	0		Revision Code Bit 3
6	0		Revision Code Bit 2
5	0		Revision Code Bit 1
4	0		Revision Code Bit 0
3	0		Device ID Bit 3
2	0		Device ID Bit 2
1	1		Device ID Bit 1
0	1		Device ID Bit 0

Byte 7: Vendor ID

Bit	@Pup	Name	Description
7	0	Reserved	Reserved
6	0	Reserved	Reserved
5	0	Reserved	Reserved
4	0	Reserved	Reserved
3	1		Vendor ID Bit 3
2	0		Vendor ID Bit 2
1	0		Vendor ID Bit 1
0	0		Vendor ID Bit 0

Byte 8: SRC PLL (PLL3) Overclocking Register

Bit	@Pup	Name	Description
7	0	SRC_N[7]	N counter Control bit [7:0]
6	0	SRC_N[6]	N counter Control bit [7:0]
5	0	SRC_N[5]	N counter Control bit [7:0]
4	0	SRC_N[4]	N counter Control bit [7:0]
3	0	SRC_N[3]	N counter Control bit [7:0]
2	0	SRC_N[2]	N counter Control bit [7:0]
1	0	SRC_N[1]	N counter Control bit [7:0]
0	0	SRC_N[0]	N counter Control bit [7:0]

Byte 9: Clock Request Mapping Register

Bit	@Pup	Name	Description
7	0	CLKREQC#	CLKREQC# Controls ATIG3 0 = Not controlled, 1 = Controlled

Byte 9: Clock Request Mapping Register (continued)

Bit	@Pup	Name	Description
6	0	CLKREQC#	CLKREQC# Controls ATIG2 0 = Not controlled, 1 = Controlled
5	0	CLKREQC#	CLKREQC# Controls ATIG1 0 = Not controlled, 1 = Controlled
4	1	CLKREQC#	CLKREQC# Controls ATIG0 0 = Not controlled, 1 = Controlled
3	0	Reserved	Reserved
2	0	Reserved	Reserved
1	0	Reserved	Reserved
0	0	Reserved	Reserved

Byte 10: Dynamic Frequency Register4

Bit	@Pup	Name	Description
7	0	Reserved	Reserved
6	1	Reserved	Reserved
5	0	Reserved	Reserved
4	1	Reserved	Reserved
3	1	Reserved	Reserved
2	0	Reserved	Reserved
1	0	SMSW_SEL_Bypass	Smooth switch on/off 0: on 1: off
0	0	SMSW_SEL	Smooth Switch Select 0: Select CPU_PLL (PLL1) 1: Select ATIG_PLL (PLL2)

Byte 11: WDT System Register

Bit	@Pup	Name	Description
7	0	Recovery_Frequency	This bit allows selection of the frequency setting that the clock will be restored to once the system is rebooted 0: Use HW settings, 1: Recovery N[8:0]
6	0	Timer_SEL	Timer_SEL selects the WD reset function at SRESET pin when WD time out. 0 = Reset and Reload Recovery_Frequency 1 = Only Reset
5	1	Time_Scale	Time_Scale allows selection of WD time scale 0 = 294 ms, 1 = 2.34 s
4	0	WD_Alarm	WD_Alarm is set to “1” when the watchdog times out. It is reset to “0” when the system clears the WD_TIMER time stamp.
3	0	WD_TIMER2	Watchdog timer time stamp selection 000: Reserved (test mode) 001: 1 * Time_Scale 010: 2 * Time_Scale 011: 3 * Time_Scale 100: 4 * Time_Scale 101: 5 * Time_Scale 110: 6 * Time_Scale 111: 7 * Time_Scale
2	0	WD_TIMER1	
1	0	WD_TIMER0	
0	0	WD_EN	Watchdog timer enable, when the bit is asserted, Watchdog timer is triggered and time stamp of WD_Timer is loaded 0 = Disable, 1 = Enable

Byte 12: CPU DAF Register1

Bit	@Pup	Name	Description
7	0	CPU_DAF_N[7]	If Prog_CPU_EN is set, the values programmed in CPU_DAF_N[8:0] and CPU_DAF_M[6:0] will be used to determine the CPU output frequency. The setting of the FS_Override bit determines the frequency ratio for CPU and other output clocks. When it is cleared, the same frequency ratio stated in the Latched FS[D:A] register will be used. When it is set, the frequency ratio stated in the FSEL[3:0] register will be used.
6	0	CPU_DAF_N[6]	
5	0	CPU_DAF_N[5]	
4	0	CPU_DAF_N[4]	
3	0	CPU_DAF_N[3]	
2	0	CPU_DAF_N[2]	
1	0	CPU_DAF_N[1]	
0	0	CPU_DAF_N[0]	

Byte 13: CPU DAF Register2

Bit	@Pup	Name	Description
7	0	CPU_DAF_N[8]	If Prog_CPU_EN is set, the values programmed in CPU_DAF_N[8:0] and CPU_DAF_M[6:0] will be used to determine the CPU output frequency. The setting of the FS_Override bit determines the frequency ratio for CPU and other output clocks. When it is cleared, the same frequency ratio stated in the Latched FS[D:A] register will be used. When it is set, the frequency ratio stated in the FSEL[3:0] register will be used.
6	0	CPU_DAF_M[6]	
5	0	CPU_DAF_M[5]	
4	0	CPU_DAF_M[4]	
3	0	CPU_DAF_M[3]	
2	0	CPU_DAF_M[2]	
1	0	CPU_DAF_M[1]	
0	0	CPU_DAF_M[0]	

Byte 14: ATIG DAF Register1

Bit	@Pup	Name	Description
7	0	ATIG_DAF_N[7]	If Prog_ATIG_EN is set, the values programmed in ATIG_DAF_N[8:0] will be used to determine the ATIG output frequency.
6	0	ATIG_DAF_N[6]	
5	0	ATIG_DAF_N[5]	
4	0	ATIG_DAF_N[4]	
3	0	ATIG_DAF_N[3]	
2	0	ATIG_DAF_N[2]	
1	0	ATIG_DAF_N[1]	
0	0	ATIG_DAF_N[0]	

Byte 15: WDT Recovery Register

Bit	@Pup	Name	Description
7	0	RECOVERY_N[7]	Used when RESET_IN# is asserted or the Watch Dog timer times out. This will be the safe value or last known good frequency of the CPU. It is set by the user before engaging in any overclocking exercise. M values revert to those set by the FS[C:A] pins
6	0	RECOVERY_N[6]	
5	0	RECOVERY_N[5]	
4	0	RECOVERY_N[4]	
3	0	RECOVERY_N[3]	
2	0	RECOVERY_N[2]	
1	0	RECOVERY_N[1]	
0	0	RECOVERY_N[0]	

Byte 16: Overclocking support Register

Bit	@Pup	Name	Description
7	0	ATIG_N8	ATIG DAF bit N8

Byte 16: Overclocking support Register (continued)

Bit	@Pup	Name	Description
6	1	FS[C:A]	FS_override 0 = Select operating frequency by FS[C:A] input pins 1 = Select operating frequency by FSEL[C:A] register values
5	0	DF_EN	Dynamic Frequency enable for CPU frequencies 0 = Disable, 1 = Enable
4	0	Prog_SRC_EN	Enables the setting of SRC_PLL (PLL3) N values via byte 8 0 = Disable, 1 = Enable
3	0	Prog_ATIG_EN	Enables the setting of ATIG_PLL (PLL2) N values via byte 17 0 = Disable, 1 = Enable
2	0	Prog_CPU_EN	Enables the setting of CPU_PLL (PLL1) M and N values via byte 15 and 16 0 = Disable, 1 = Enable
1	0	Watchdog Autorecovery	Watchdog Autorecovery Mode 0 = Disable (manual), 1 = Enable (Auto)
0	0	Recovery_N8	CPU Safe recovery bit 8 for RESET_IN and Watchdog timer timeout.

Table 4. Crystal Recommendations

Frequency (Fund)	Cut	Loading	Load Cap	Drive (max.)	Shunt Cap (max.)	Motional (max.)	Tolerance (max.)	Stability (max.)	Aging (max.)
14.31818 MHz	AT	Parallel	20 pF	0.1 mW	5 pF	0.016 pF	35 ppm	30 ppm	5 ppm

Crystal Recommendations

The CY28RS680-2 requires a Parallel Resonance Crystal. Substituting a series resonance crystal will cause the CY28RS680-2 to operate at the wrong frequency and violate the ppm specification. For most applications there is a 300-ppm frequency shift between series and parallel crystals due to incorrect loading.

Crystal Loading

Crystal loading plays a critical role in achieving low ppm performance. To realize low ppm performance, the total capacitance the crystal will see must be considered to calculate the appropriate capacitive loading (CL).

Figure 1 shows a typical crystal configuration using the two trim capacitors. An important clarification for the following discussion is that the trim capacitors are in series with the crystal not parallel. It's a common misconception that load capacitors are in parallel with the crystal and should be approximately equal to the load capacitance of the crystal. This is not true.

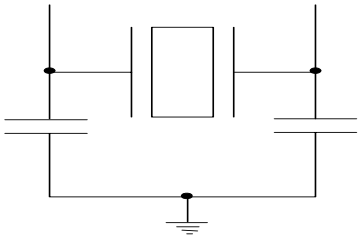


Figure 1. Crystal Capacitive Clarification

Calculating Load Capacitors

In addition to the standard external trim capacitors, trace capacitance and pin capacitance must also be considered to correctly calculate crystal loading. As mentioned previously, the capacitance on each side of the crystal is in series with the crystal. This means the total capacitance on each side of the crystal must be twice the specified crystal load capacitance (CL). While the capacitance on each side of the crystal is in series with the crystal, trim capacitors (Ce1,Ce2) should be calculated to provide equal capacitive loading on both sides.

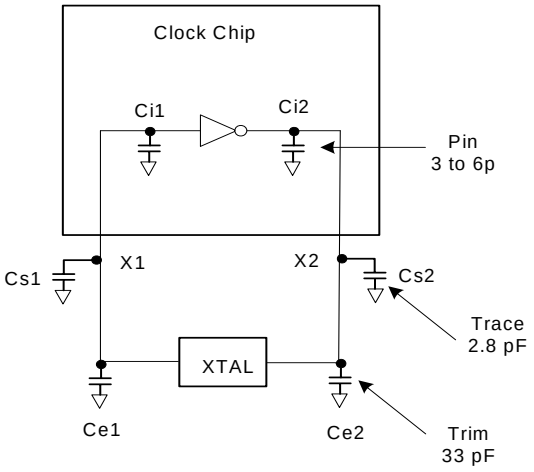


Figure 2. Crystal Loading Example

Use the following formulas to calculate the trim capacitor values for Ce1 and Ce2.

Load Capacitance (each side)

$$Ce = 2 * CL - (Cs + Ci)$$

Total Capacitance (as seen by the crystal)

$$CLe = \frac{1}{\left(\frac{1}{Ce1 + Cs1 + Ci1} + \frac{1}{Ce2 + Cs2 + Ci2}\right)}$$

CL ..... Crystal load capacitance

CLe .....Actual loading seen by crystal using standard value trim capacitors

Ce .....External trim capacitors

Cs ..... Stray capacitance (terraced)

Ci ..... Internal capacitance (lead frame, bond wires etc.)

CLK_REQ[A:C]# Description

The CLKREQ#[A:C] signals are active LOW inputs used for clean stopping and starting selected SRC outputs. The CLKREQ# signal is a de-bounced signal in that its state must remain unchanged during two consecutive rising edges of DIFC to be recognized as a valid assertion or deassertion. (The assertion and deassertion of this signal is absolutely asynchronous.)

CLK_REQ[A:C]# Assertion

The impact of asserting the CLKREQ#[A:C] pins is that all DIF outputs that are set in the control registers to stoppable via assertion of CLKREQ#[A:C] are to be stopped after their next transition. The final state of all stopped DIF signals is tristate, both SRCT clock and SRCC clock outputs will be driven Tristate.

CLK_REQ[A:C]# Deassertion

All differential outputs that were stopped are to resume normal operation in a glitch free manner. The maximum latency from the deassertion to active outputs is between 2 and 6 SRC clock periods (2 clocks are shown) with all SRC outputs resuming simultaneously.

RESET_IN# Assertion

The RESET_IN# is a negative edge triggered signal. When asserted, all PLLs will revert back to a safe default frequency. The clock output will be allowed to turn off for a maximum of 4 ms. After this time the PLLs will output a locked clock at a preselected safe frequency. The safe frequency is either based upon the power on reset default values or upon the value stored in the safe frequency register. The safe frequency register is accessible via SMBUS (Bytes 18 & 19). The clock outputs must be stable at the correct safe frequency at least 2 ms before the deassertion of RESET_IN#.

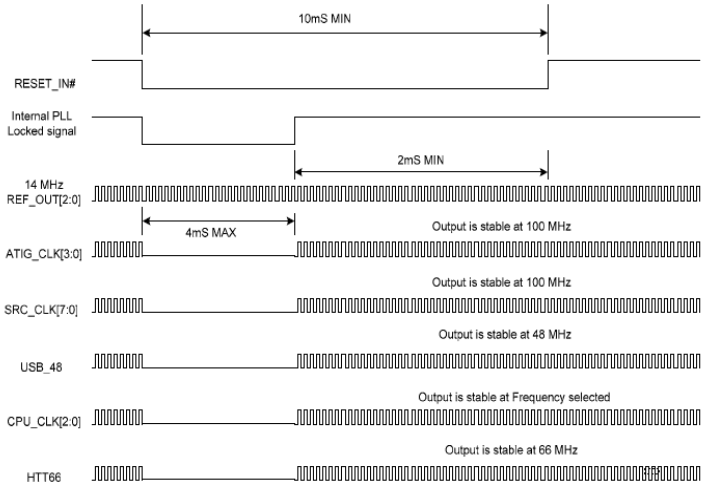


Figure 3. RESET_IN# Assertion/Deassertion Waveform

Absolute Maximum Conditions

Parameter	Description	Condition	Min.	Max.	Unit
V_{DD}	Core Supply Voltage		–0.5	4.6	V
V_{DDA}	Analog Supply Voltage		–0.5	4.6	V
V_{IN}	Input Voltage	Relative to V_{SS}	–0.5	V_{DD} + 0.5	VDC
T_S	Temperature, Storage	Non-functional	–65	+150	°C
T_A	Temperature, Operating Ambient	Functional	0	70	°C
T_J	Temperature, Junction	Functional	–	150	°C
ESD_{HBM}	ESD Protection (Human Body Model)	MIL-STD-883, Method 3015	2000	–	V
$Ø_{JC}$	Dissipation, Junction to Case	Mil-Spec 883E Method 1012.1	–	20	°C/W
$Ø_{JA}$	Dissipation, Junction to Ambient	JEDEC (JESD 51)	–	60	°C/W
UL-94	Flammability Rating	At 1/8 in.	V–0		
MSL	Moisture Sensitivity Level		1		

Multiple Supplies: The Voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

DC Electrical Specifications

Parameter	Description	Condition	Min.	Max.	Unit
VDD_REF, VDD_CPU, VDD_PCI, VDD_SRC, VDD_48	3.3V Operating Voltage	3.3V ± 5%	3.135	3.465	V
$V_{ILSMBUS}$	Input Low Voltage	SDATA, SCLK	–	1.0	V
$V_{IHSMBUS}$	Input High Voltage	SDATA, SCLK	2.2	-	V
V_{IL}	Input Low Voltage	V_{DD}	V_{SS} – 0.3	0.8	V
V_{IH}	Input High Voltage		2.0	V_{DD} + 0.3	V
I_{IL}	Input Leakage Current	Except Pull-ups or Pull-downs $0 < V_{IN} < V_{DD}$	–5	5	mA
V_{OL}	Output Low Voltage	I_{OL} = 1 mA	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = 1 mA	2.4	–	V
I_{OZ}	High-Impedance Output Current		–10	10	µA
C_{IN}	Input Pin Capacitance		3	5	pF
C_{OUT}	Output Pin Capacitance		3	5	pF
L_{IN}	Pin Inductance		–	7	nH
V_{XIH}	Xin High Voltage		0.7 * V_{DD}	V_{DD}	V
V_{XIL}	Xin Low Voltage		0	0.3 * V_{DD}	V
IDD	Dynamic Supply Current	At max load and frequency	–	250	mA

AC Electrical Specifications

Parameter	Description	Condition	Min.	Max.	Unit
Crystal					
T_{DC}	XIN Duty Cycle	The device will operate reliably with input duty cycles up to 30/70 but the REF clock duty cycle will not be within specification	47.5	52.5	%
T_{PERIOD}	XIN Period	When XIN is driven from an external clock source	69.841	71.0	ns
T_R / T_F	XIN Rise and Fall Times	Measured between 0.3V_{DD} and 0.7V_{DD}	–	10.0	ns
T_{CCJ}	XIN Cycle to Cycle Jitter	As an average over 1-µs duration	–	500	ps
L_{ACC}	Long-term Accuracy	Over 150 ms	–	300	ppm

AC Electrical Specifications (continued)

Parameter	Description	Condition	Min.	Max.	Unit
CPU outputs					
T_R / T_F	Output Slew Rate	Measured @ test load using VOCM ±400 mV, 0.85 to 1.65	2	7	V/ns
V_{DIFF}	Differential Voltage	Measured at load single ended	0.4	2.3	V
L_{ACC}	Long Term Accuracy		–300	300	ppm
T_{SKEW}	Any CPU to CPU Clock Skew	Measured at crossing point V_{OX}	–	250	ps
ΔV_{DIFF}	Change in VDIFF_DC Magnitude	Measured at load single ended	–150	150	mV
V_{CM}	Common Mode Voltage	Measured at load single ended	1.05	1.45	V
ΔV_{CM}	Change in V_{CM}	Measured at load single ended	–200	200	mV
T_{DC}	Duty Cycle	Measured at V_{OX}	45	53	%
T_{JCYC}	Cycle to Cycle Jitter	Measured at V_{OX}	0	85	ps
SRC					
T_{DC}	SRCT and SRCC Duty Cycle	Measured at crossing point V_{OX}	45	55	%
T_{PERIOD}	100-MHz SRCT and SRCC Period	Measured at crossing point V_{OX}	9.997001	10.00300	ns
$T_{PERIODSS}$	100-MHz SRCT and SRCC Period, SSC	Measured at crossing point V_{OX}	9.997001	10.05327	ns
$T_{PERIODAbs}$	100-MHz SRCT and SRCC Absolute Period	Measured at crossing point V_{OX}	10.12800	9.872001	ns
$T_{PERIODSSAbs}$	100-MHz SRCT and SRCC Absolute Period, SSC	Measured at crossing point V_{OX}	9.872001	10.17827	ns
T_{SKEW}	Any SRCT/C to SRCT/C Clock Skew	Measured at crossing point V_{OX}	–	250	ps
T_{CCJ}	SRCT/C Cycle to Cycle Jitter	Measured at crossing point V_{OX}	–	125	ps
L_{ACC}	SRCT/C Long Term Accuracy	Measured at crossing point V_{OX}	–300	300	ppm
T_R / T_F	SRCT and SRCC Rise and Fall Times	Measured from V_{OL} = 0.175 to V_{OH} = 0.525V	175	700	ps
T_{RFM}	Rise/Fall Matching	Determined as a fraction of $2*(T_R - T_F)/(T_R + T_F)$	–	20	%
ΔT_R	Rise TimeVariation		–	125	ps
ΔT_F	Fall Time Variation		–	125	ps
V_{HIGH}	Voltage High	Math averages *Figure 7*	660	850	mv
V_{LOW}	Voltage Low	Math averages *Figure 7*	–150	–	mv
V_{OX}	Crossing Point Voltage at 0.7V Swing		250	550	mV
V_{OVS}	Maximum Overshoot Voltage		–	V_{HIGH} + 0.3	V
V_{UDS}	Minimum Undershoot Voltage		–0.3	–	V
V_{RB}	Ring Back Voltage	See *Figure 7.* Measure SE	–	0.2	V
ATIG					
T_{DC}	ATIGT and ATIGC Duty Cycle	Measured at crossing point V_{OX}	45	55	%
T_{PERIOD}	100-MHz ATIGT and ATIGC Period	Measured at crossing point V_{OX}	9.997001	10.00300	ns
$T_{PERIODSS}$	100-MHz ATIGT and ATIGC Period, SSC	Measured at crossing point V_{OX}	9.997001	10.05327	ns
$T_{PERIODAbs}$	100-MHz ATIGT and ATIGC Absolute Period	Measured at crossing point V_{OX}	10.12800	9.872001	ns
$T_{PERIODSSAbs}$	100-MHz ATIGT and ATIGC Absolute Period, SSC	Measured at crossing point V_{OX}	9.872001	10.17827	ns
T_{SKEW}	Any ATIGT/C to ATIGT/C Clock Skew	Measured at crossing point V_{OX}	–	250	ps
T_{CCJ}	ATIGT/C Cycle to Cycle Jitter	Measured at crossing point V_{OX}	–	125	ps
L_{ACC}	ATIGT/C Long Term Accuracy	Measured at crossing point V_{OX}	–300	300	ppm

AC Electrical Specifications (continued)

Parameter	Description	Condition	Min.	Max.	Unit
T_R / T_F	ATIGT and ATIGC Rise and Fall Times	Measured from V_{OL} = 0.175 to V_{OH} = 0.525V	175	700	ps
T_{RFM}	Rise/Fall Matching	Determined as a fraction of $2*(T_R - T_F)/(T_R + T_F)$	–	20	%
ΔT_R	Rise Time Variation		–	125	ps
ΔT_F	Fall Time Variation		–	125	ps
V_{HIGH}	Voltage High	Math averages *Figure 7*	660	850	mv
V_{LOW}	Voltage Low	Math averages *Figure 7*	–150	–	mv
V_{OX}	Crossing Point Voltage at 0.7V Swing		250	550	mV
V_{OVS}	Maximum Overshoot Voltage		–	V_{HIGH} + 0.3	V
V_{UDS}	Minimum Undershoot Voltage		–0.3	–	V
V_{RB}	Ring Back Voltage	See *Figure 7.* Measure SE	–	0.2	V
HTT66 HyperTransport Output					
F66	Operating Frequency			66.67	MHz
T_{DC}	Duty Cycle	Measured at 1.5V	45	55	%
T_R / T_F	Slew Rate	Measured at 20% and 60%	0.9	4	V/ns
T_{CCJ}	Cycle to Cycle jitter	Measured at 1.5V		250	ps
T_{LTJ}	Long Term jitter	Measured at 1.5V		1000	ps
T_{SKEW}	HTT66 clock to PCI clock Skew	Measurement at 1.5V	-	500	ps
USB					
T_{DC}	Duty Cycle	Measurement at 1.5V	45	55	%
T_{PERIOD}	Period	Measurement at 1.5V	20.83125	20.83542	ns
$T_{PERIODAbs}$	Absolute Period	Measurement at 1.5V	20.48125	21.18542	ns
T_{HIGH}	USB High time	Measurement at 2.4V	8.094	10.036	nS
T_{LOW}	USB Low time	Measurement at 0.4V	7.694	9.836	nS
T_R / T_F	Rise and Fall Times	Measured between 0.8V and 2.0V	1.0	2.0	ns
T_{CCJ}	Cycle to Cycle Jitter	Measurement at 1.5V	–	300	ps
L_{ACC}	USB Long Term Accuracy	Measurement at 1.5V	–100	100	ppm
T_{LTJ}	Long Term Jitter	Measurement at 1.5V@1 µs	–	1000	ps
REF					
T_{DC}	REF Duty Cycle	Measurement at 1.5V	45	55	%
T_{PERIOD}	REF Period	Measurement at 1.5V	69.8203	69.8622	ns
$T_{PERIODAbs}$	REF Absolute Period	Measurement at 1.5V	68.82033	70.86224	ns
T_R / T_F	REF Rise and Fall Times	Measured between 0.8V and 2.0V	1.0	4.0	V/ns
T_{CCJ}	REF Cycle to Cycle Jitter	Measurement at 1.5V	–	500	ps
T_{LTJ}	Long Term Jitter	Measurement at 1.5V@10 µs	–	500	ps
ENABLE/DISABLE and SET-UP					
T_{STABLE}	Clock Stabilization from Power-up		–	1.8	ms
T_{SS}	Stopclock Set-up Time		10.0	–	ns
T_{SH}	Stopclock Hold Time		0	–	ns

Test and Measurement Set-up

For HT66, PCI, USB Single-ended Signals and Reference

The following diagrams show the test load configurations for the single-ended PCI, USB, and REF output signals.

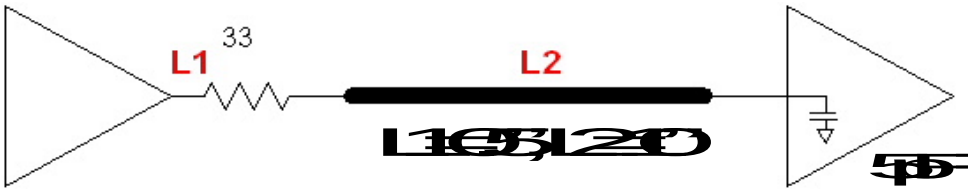


Figure 4. Single-ended HT66/PCI/USB Load Configuration

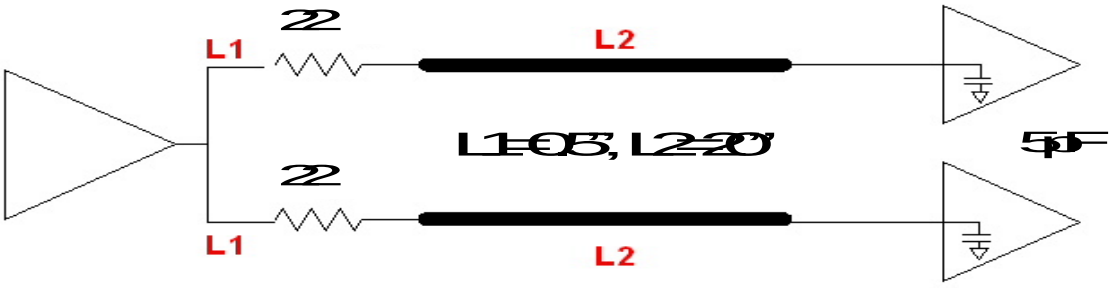


Figure 5. Single-ended REF Load Configuration

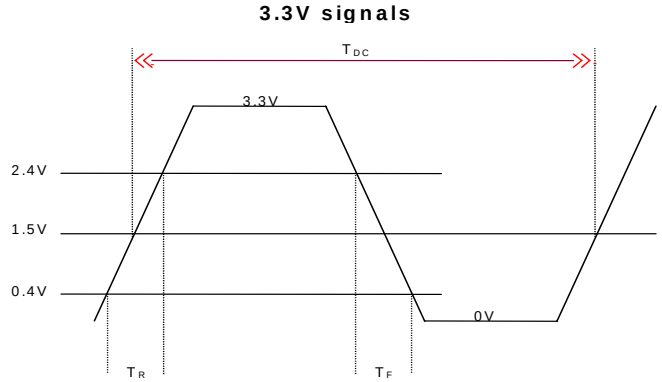


Figure 6. Single-ended Output Signals (for AC Parameters Measurement)

For SRC/ATIG Output Signals

The following diagram shows the test load configuration for the differential SRC/ATIG outputs.

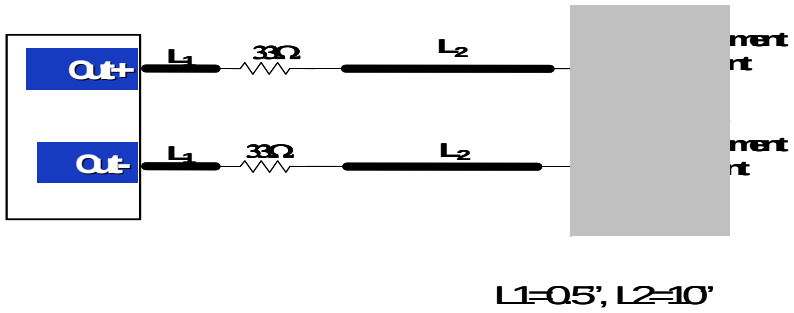


Figure 7. 0.7V Load Configuration

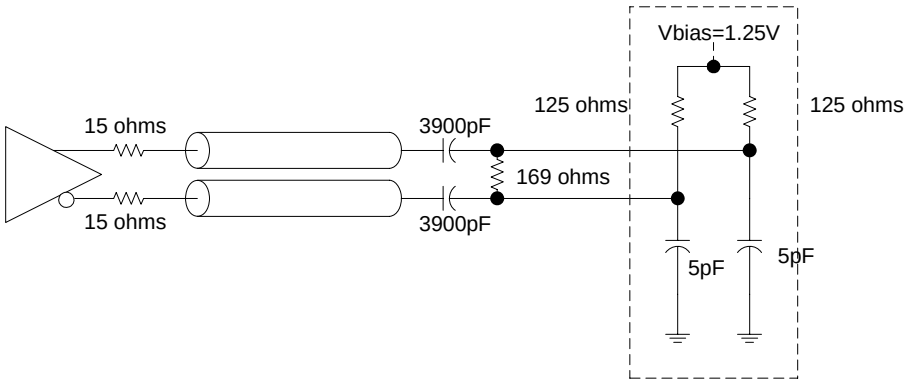


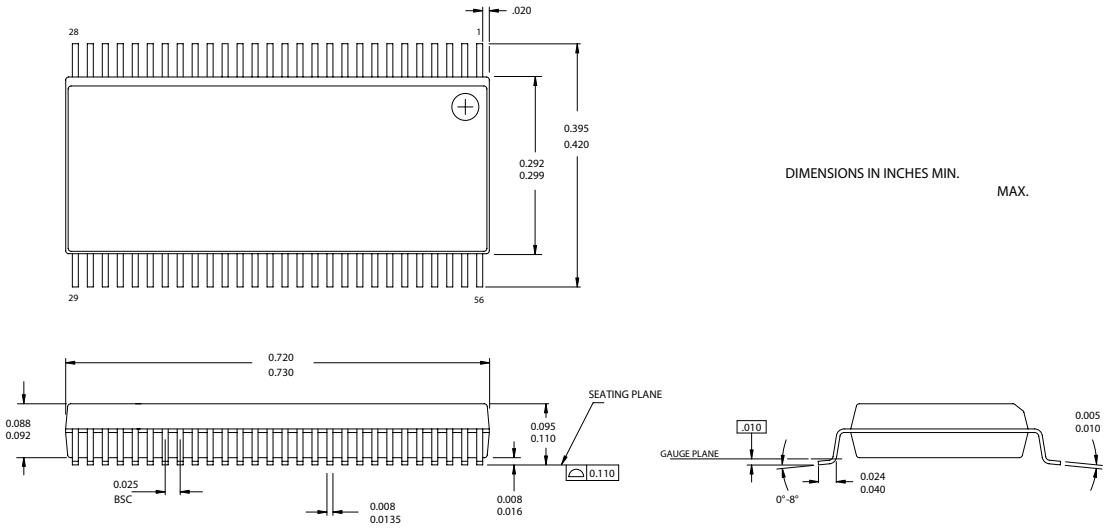
Figure 8. CPU Output Load Configuration

Ordering Information

Part Number	Package Type	Product Flow
Lead-free		
CY28RS680ZXC-2	56-pin TSSOP	Commercial, 0° to 70°C
CY28RS680ZXC-2T	56-pin TSSOP – Tape and Reel	Commercial, 0° to 70°C
CY28RS680OXC-2	56-pin SSOP	Commercial, 0° to 70°C
CY28RS680OXC-2	56-pin SSOP – Tape and Reel	Commercial, 0° to 70°C

Package Drawing and Dimensions

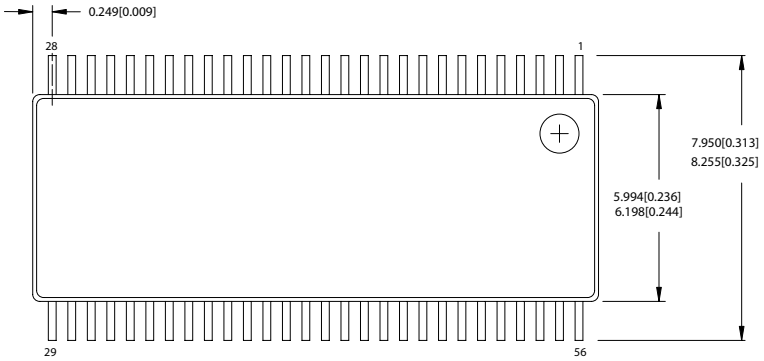
56-Lead Shrunk Small Outline Package O56



56-Lead Thin Shrunk Small Outline Package, Type II (6 mm x 12 mm) Z5624

NOTE :

1. JEDEC STD REF MO-153
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH
   MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.006 in (0.152 mm) PER SIDE
3. DIMENSIONS IN MM. [INCHES] MIN. MAX.
3. PACKAGE WEIGHT 0.42gms



PART #	
Z5624	STANDARD PKG.
ZZ5624	LEAD FREE PKG.