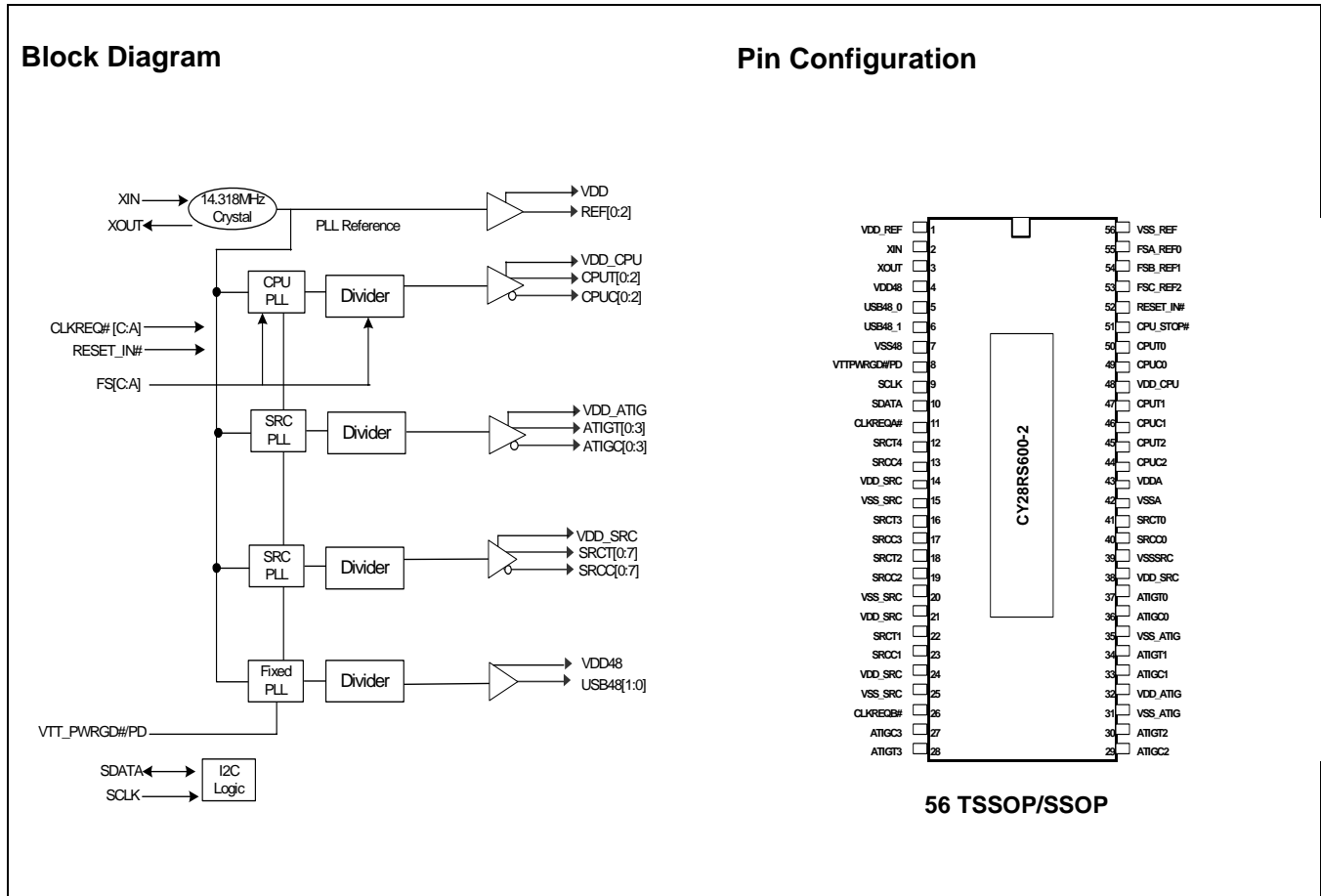


**Clock Generator for ATI® RS5XX, 6XX Chipsets**

**Features**

- Supports Intel® CPU
- Selectable CPU frequencies
- Differential CPU clock pairs (50% over/10% under clocked)
- 100 MHz differential ATI Graphics clocks (100% over/10% under clocked)
- 100 MHz differential SRC clocks (10% over/under clocked)
- 48 MHz USB clock
- I<sup>2</sup>C support with readback capabilities
- Ideal Lexmark Spread Spectrum profile for maximum electromagnetic interference (EMI) reduction
- 3.3V power supply
- 56-pin TSSOP/SSOP packages

CPU	SRC	ATIG	REF	USB_48
x3	x5	X4	x 3	x 2



**Pin Description**

Pin No.	Name	Type	Description
1	VDD_REF	PWR	3.3V power supply for REF, XTAL
2	XIN	I	14.318 MHz Crystal Input
3	XOUT	O	14.318 MHz Crystal Output
4	VDD_48	PWR	3.3V power supply for USB outputs
5,6	USB_48 [1:0]	O, SE	48 MHz clock output. Intel® Type-3A buffer
7	VSS_48	GND	Ground for USB outputs
8	VTT_PWRGD#/PD	I PD	3.3V LVTTTL input. This pin is a level sensitive strobe used to latch the FS_A, FS_B, and FS_C inputs. After asserting VTT_PWRGD# (active LOW), this pin becomes a realtime input for asserting power-down (active HIGH)
9	SCLK	I	SMBus-compatible SCLOCK. This pin has an internal pull-up, but is tri-stated in power-down.
10	SDATA	I/O	SMBus-compatible SDATA. This pin has an internal pull-up, but is tri-stated in power-down.
11, 26	CLKREQ#[A:B]	I, SE, PU	Output Enable control for SRCT/C. Output enable control required by Minicard specification. This pin has an internal pull-up. 0 = selected SRC output is enabled. 1 = selected SRC output is disabled.
12, 13, 16, 17, 18, 19, 20, 22, 23, 40, 41	SRCT/C[4:0]	O, DIF	100 MHz differential serial reference clock. Intel Type-SR buffer. (10% overclocking support through SMBUS)
14, 21, 24, 38	VDD_SRC	PWR	3.3V power supply for SRC outputs
15, 20, 25, 39	VSS_SRC	GND	Ground for SRC outputs
27, 28, 29, 30, 33, 34, 36, 37	ATIGT/C[3:0]	O, DIF	Differential Selectable serial reference clock. Intel Type-SR buffer. Includes 50% overclock support through SMBUS
31, 35	VSS_ATIG	GND	Ground for ATIG outputs
32	VDD_ATIG	PWR	3.3V power supply for ATIG outputs
42	VSSA	GND	Analog Ground
43	VDDA	PWR	3.3V Analog Power for PLLs
44, 45, 46, 47, 49, 50	CPUT/C[2:0]	O, DIF	Differential CPU clock output. Intel Type-SR buffer.
48	VDD_CPU	PWR	3.3V power supply for CPU outputs
51	CPU_STP#	I, PU	3.3V LVTTTL input. This pin is used to gate the CPU outputs. CPU outputs are turned off two cycles after assertion of this pin
52	RESET_IN#	I, PU	3.3V LVTTTL Input (Negative Edge Triggered) When this pin is asserted LOW, all PLLs will transition to a safe default frequency. This may be the POR defaults or a safe value stored in SMBUS registers.
53	REF2/FSC	I/O, SE	14.318 MHz REF clock output/CPU Frequency Select Intel Type-5 buffer.
54	REF1/FSB	I/O, SE	14.318 MHz REF clock output/CPU Frequency Select Intel Type-5 buffer.
55	REF0/FSA	I/O, SE,	14.318 MHz REF clock output/CPU Frequency Select Intel Type-5 buffer.
56	VSS_REF	PWR	GND for REF, XTAL

**Table 1. Frequency Select Table (FS\_A FS\_B FS\_C)**

FS_C	FS_B	FS_A	CPU	SRC	ATIG	REF0	USB	
1	0	1	100 MHz	100 MHz	100 MHz	14.318 MHz	48 MHz	
0	0	1	133 MHz	100 MHz	100 MHz	14.318 MHz	48 MHz	
0	1	1	166 MHz	100 MHz	100 MHz	14.318 MHz	48 MHz	
0	1	0	200 MHz	100 MHz	100 MHz	14.318 MHz	48 MHz	
0	0	0	266 MHz	100 MHz	100 MHz	14.318 MHz	48 MHz	
1	0	0	333 MHz	100 MHz	100 MHz	14.318 MHz	48 MHz	
1	1	0	400 MHz	100 MHz	100 MHz	14.318 MHz	48 MHz	
1	1	1	RESERVED					

### Frequency Select Pins (FS\_A, FS\_B, FS\_C)

Host clock frequency selection is achieved by applying the appropriate logic levels to FS\_A, FS\_B, and FS\_C inputs prior to VTT\_PWRGD# assertion (as seen by the clock synthesizer). Upon VTT\_PWRGD# being sampled LOW by the clock chip (indicating processor VTT voltage is stable), the clock chip samples the FS\_A, FS\_B, and FS\_C values. For all logic levels of FS\_A, FS\_B, and FS\_C VTT\_PWRGD# employs a one-shot functionality in that once a valid LOW on VTT\_PWRGD# has been sampled, all further VTT\_PWRGD#, FS\_A, FS\_B, and FS\_C transitions will be ignored. There is one CPU frequency select table based on the CK410 specification.

### Serial Data Interface

To enhance the flexibility and function of the clock synthesizer, a two-signal serial interface is provided. Through the Serial Data Interface, various device functions, such as individual clock output buffers, can be individually enabled or disabled. The registers associated with the Serial Data Interface

initialize to their default setting upon power-up, and therefore use of this interface is optional. Clock device register changes are normally made upon system initialization, if any are required. The interface cannot be used during system operation for power management functions.

### Data Protocol

The clock driver serial protocol accepts byte write, byte read, block write, and block read operations from the controller. For block write/read operation, the bytes must be accessed in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after any complete byte has been transferred. For byte write and byte read operations, the system controller can access individually indexed bytes. The offset of the indexed byte is encoded in the command code, as described in *Table 2*.

The block write and block read protocol is outlined in *Table 3* while *Table 4* outlines the corresponding byte write and byte read protocol. The slave receiver address is 11010010 (D2h).

**Table 2. Command Code Definition**

Bit	Description
7	0 = Block read or block write operation, 1 = Byte read or byte write operation
(6:5)	Chip select address, set to '00' to access device
(4:0)	Byte offset for byte read or byte write operation. For block read or block write operations, these bits should be '00000'

**Table 3. Block Read and Block Write Protocol**

Block Write Protocol		Block Read Protocol	
Bit	Description	Bit	Description
1	Start	1	Start
8:2	Slave address – 7 bits	8:2	Slave address – 7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
18:11	Command Code – 8 bits	18:11	Command Code – 8 bits
19	Acknowledge from slave	19	Acknowledge from slave
27:20	Byte Count – 8 bits	20	Repeat start
28	Acknowledge from slave	27:21	Slave address – 7 bits
36:29	Data byte 1 – 8 bits	28	Read = 1
37	Acknowledge from slave	29	Acknowledge from slave
45:38	Data byte 2 – 8 bits	37:30	Byte Count from slave – 8 bits

**Table 3. Block Read and Block Write Protocol (continued)**

Block Write Protocol		Block Read Protocol	
Bit	Description	Bit	Description
46	Acknowledge from slave	38	Acknowledge
....	Data Byte /Slave Acknowledges	46:39	Data byte 1 from slave – 8 bits
....	Data Byte N – 8 bits	47	Acknowledge
....	Acknowledge from slave	55:48	Data byte 2 from slave – 8 bits
....	Stop	56	Acknowledge
		....	Data bytes from slave / Acknowledge
		....	Data Byte N from slave – 8 bits
		....	NOT Acknowledge

**Table 4. Byte Read and Byte Write Protocol**

Byte Write Protocol		Byte Read Protocol	
Bit	Description	Bit	Description
1	Start	1	Start
8:2	Slave address – 7 bits	8:2	Slave address – 7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
18:11	Command Code – 8 bits	18:11	Command Code – 8 bits
19	Acknowledge from slave	19	Acknowledge from slave
27:20	Data byte – 8 bits	20	Repeated start
28	Acknowledge from slave	27:21	Slave address – 7 bits
29	Stop	28	Read
		29	Acknowledge from slave
		37:30	Data from slave – 8 bits
		38	NOT Acknowledge
		39	Stop

## Control Registers

### Byte 0: Output Enable Register 0

Bit	@Pup	Name	Description
7	1	Reserved	Reserved
6	1	Reserved	Reserved
5	1	Reserved	Reserved
4	1	SRC[T/C]4	SRC[T/C]4 Output Enable 0 = Disable (Hi-Z), 1 = Enable
3	1	SRC[T/C]3	SRC[T/C]3 Output Enable 0 = Disable (Hi-Z), 1 = Enable
2	1	SRC[T/C]2	SRC[T/C]2 Output Enable 0 = Disable (Hi-Z), 1 = Enable
1	1	SRC[T/C]1	SRC[T/C]1 Output Enable 0 = Disable (Hi-Z), 1 = Enable
0	1	SRC [T/C]0	SRC[T/C]0 Output Enable 0 = Disable (Hi-Z), 1 = Enable

**Byte 1: Output Enable Register 1**

Bit	@Pup	Name	Description
7	1	Reserved	Reserved
6	1	Reserved	Reserved
5	1	ATIG[T/C]3	ATIG[T/C]3 Output Enable 0 = Disable (Hi-Z), 1 = Enable
4	1	ATIG[T/C]2	ATIG[T/C]2 Output Enable 0 = Disable (Hi-Z), 1 = Enable
3	1	ATIG[T/C]1	ATIG[T/C]1 Output Enable 0 = Disable (Hi-Z), 1 = Enable
2	1	ATIG[T/C]0	ATIG[T/C]0 Output Enable 0 = Disable (Hi-Z), 1 = Enable
1	1	CPU[T/C]2	CPU[T/C]2 Output Enable 0 = Disable (Hi-Z), 1 = Enable
0	1	CPU[T/C]1	CPU[T/C]1 Output Enable 0 = Disable (Hi-Z), 1 = Enable

**Byte 2: Output Enable Register 2**

Bit	@Pup	Name	Description
7	1	CPU[T/C]0	CPU[T/C]0 Output Enable 0 = Disable (Hi-Z), 1 = Enable
6	1	USB_48_1	USB_48_1 Output Enable 0 = Disable (Hi-Z), 1 = Enable
5	1	USB_48_0	USB_48_0 Output Enable 0 = Disable (Hi-Z), 1 = Enable
4	1	REF_2	REF_2 Output Enable 0 = Disable (Hi-Z), 1 = Enable
3	1	REF_1	REF_1 Output Enable 0 = Disable (Hi-Z), 1 = Enable
2	1	REF_0	REF_0 Output Enable 0 = Disable (Hi-Z), 1 = Enable
1	1	Reserved	Reserved
0	0	CPU Spread Enable	CPU_PLL (PLL1) Spread Spectrum Enable 0= Spread Off, 1 = Spread On

**Byte 3: SW\_FREQ Selection Register**

Bit	@Pup	Name	Description																
7	HW	FSC	Read Only bit which reflects the value of pin 62 @ VTPWRGD# assertion																
6	HW	FSB	Read Only bit which reflects the value of pin 61 @ VTPWRGD# assertion																
5	HW	FSA	Read Only bit which reflects the value of pin 60 @ VTPWRGD# assertion																
4	1	ATIG_OC_SEL1	<table border="1"> <thead> <tr> <th>SEL1</th> <th>SEL0</th> <th>ATIG Output</th> <th>N</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>111.33–167 MHz</td> <td>167–250</td> </tr> <tr> <td>1</td> <td>0</td> <td>100–125 MHz</td> <td>200–250</td> </tr> <tr> <td>X</td> <td>1</td> <td>166–256 MHz</td> <td>167–256</td> </tr> </tbody> </table>	SEL1	SEL0	ATIG Output	N	0	0	111.33–167 MHz	167–250	1	0	100–125 MHz	200–250	X	1	166–256 MHz	167–256
SEL1	SEL0	ATIG Output		N															
0	0	111.33–167 MHz		167–250															
1	0	100–125 MHz		200–250															
X	1	166–256 MHz	167–256																
3	0	ATIG_OC_SEL0																	
2	0	FSEL_C	SW Frequency Selection Bits																
1	0	FSEL_B																	
0	0	FSEL_A																	

**Byte 4: Spread Spectrum Control Register**

Bit	@Pup	Name	Description
7	0	CPU_SS1	CPU (PLL1) Spread Spectrum Selection
6	0	CPU_SS0	00: -0.5% (peak to peak) 01: ±0.25% (peak to peak) 10: -1.0% (peak to peak) 11: ±0.5% (peak to peak)
5	0	ATIG_SS0	ATIG (PLL2) Spread Spectrum Selection 00: -0.5% (peak to peak) 01: -1.0% (peak to peak)
4	0	ATIG_SS_OFF	ATIG_PLL (PLL2) Spread Spectrum Enable 0 = Spread Off, 1 = Spread On
3	0	SRC_SS_OFF	SRC_PLL (PLL3) Spread Spectrum Enable 0 = Spread Off, 1 = Spread On
2	0	USB48	USB48 Output Drive Strength 0 = 1x, 1 = 2x
1	0	Reserved	Reserved
0	0	REF	REF Output Drive Strength 0 = 1X, 1 = 2x

**Byte 5: System Configuration Register**

Bit	@Pup	Name	Description
7	0	Reserved	Reserved
6	0	CPU2	Allow control of CPU2 with assertion of CPU_STP# 0 = Free running, 1 = Stopped with CPU_STP# assertion
5	0	CPU1	Allow control of CPU1 with assertion of CPU_STP# 0 = Free running, 1 = Stopped with CPU_STP# assertion
4	0	CPU0	Allow control of CPU0 with assertion of CPU_STP# 0 = Free running, 1 = Stopped with CPU_STP# assertion
3	0	Reserved	Reserved
2	0	Reserved	Reserved
1	1	Reserved	Reserved
0	0	CLKREQA#	CLKREQA# Controls SRC0 0 = Not controlled, 1 = Controlled

**Byte 6: Revision and Device ID**

Bit	@Pup	Name	Description
7	0		Revision Code Bit 3
6	0		Revision Code Bit 2
5	0		Revision Code Bit 1
4	0		Revision Code Bit 0
3	0		Device ID Bit 3
2	0		Device ID Bit 2
1	0		Device ID Bit 1
0	1		Device ID Bit 0

**Byte 7: Vendor ID**

Bit	@Pup	Name	Description
7	0	Reserved	Reserved
6	0	Reserved	Reserved
5	0	Reserved	Reserved
4	0	Reserved	Reserved

**Byte 7: Vendor ID (continued)**

Bit	@Pup	Name	Description
3	1		Vendor ID Bit 3
2	0		Vendor ID Bit 2
1	0		Vendor ID Bit 1
0	0		Vendor ID Bit 0

**Byte 8: SRC PLL (PLL3) Overclocking Register**

Bit	@Pup	Name	Description
7	0	SRC_N[7]	N counter Control bit [7:0]
6	0	SRC_N[6]	N counter Control bit [7:0]
5	0	SRC_N[5]	N counter Control bit [7:0]
4	0	SRC_N[4]	N counter Control bit [7:0]
3	0	SRC_N[3]	N counter Control bit [7:0]
2	0	SRC_N[2]	N counter Control bit [7:0]
1	0	SRC_N[1]	N counter Control bit [7:0]
0	0	SRC_N[0]	N counter Control bit [7:0]

**Byte 9: Clock Request Mapping Register**

Bit	@Pup	Name	Description
7	0	CLKREQC#	CLKREQC# Controls ATIG3 0 = Not controlled, 1 = Controlled
6	0	CLKREQC#	CLKREQC# Controls ATIG2 0 = Not controlled, 1 = Controlled
5	0	CLKREQC#	CLKREQC# Controls ATIG1 0 = Not controlled, 1 = Controlled
4	1	CLKREQC#	CLKREQC# Controls ATIG0 0 = Not controlled, 1 = Controlled
3	0	Reserved	Reserved
2	0	Reserved	Reserved
1	0	Reserved	Reserved
0	0	Reserved	Reserved

**Byte 10: Dynamic Frequency Register4**

Bit	@Pup	Name	Description
7	0	Reserved	Reserved
6	1	Reserved	Reserved
5	0	Reserved	Reserved
4	1	Reserved	Reserved
3	1	Reserved	Reserved
2	0	Reserved	Reserved
1	0	SMSW_SEL_Bypass	Smooth switch on/off 0: on 1: off
0	0	SMSW_SEL	Smooth Switch Select 0: Select CPU_PLL (PLL1) 1: Select ATIG_PLL (PLL2)

**Byte 11: WDT System Register**

Bit	@Pup	Name	Description
7	0	Recovery_Frequency	This bit allows selection of the frequency setting that the clock will be restored to once the system is rebooted 0: Use HW settings 1: Recovery N[8:0]
6	0	Timer_SEL	Timer_SEL selects the WD reset function at SRESET pin when WD time out. 0 = Reset and Reload Recovery_Frequency 1 = Only Reset
5	1	Time_Scale	Time_Scale allows selection of WD time scale 0 = 294 ms 1 = 2.34 s
4	0	WD_Alarm	WD_Alarm is set to "1" when the watchdog times out. It is reset to "0" when the system clears the WD_TIMER time stamp.
3	0	WD_TIMER2	Watchdog timer time stamp selection 000: Reserved (test mode) 001: 1 * Time_Scale 010: 2 * Time_Scale 011: 3 * Time_Scale 100: 4 * Time_Scale 101: 5 * Time_Scale 110: 6 * Time_Scale 111: 7 * Time_Scale
2	0	WD_TIMER1	
1	0	WD_TIMER0	
0	0	WD_EN	

**Byte 12: CPU DAF Register1**

Bit	@Pup	Name	Description
7	0	CPU_DAF_N[7]	If Prog_CPU_EN is set, the values programmed in CPU_DAF_N[8:0] and CPU_DAF_M[6:0] will be used to determine the CPU output frequency. The setting of the FS_Override bit determines the frequency ratio for CPU and other output clocks. When it is cleared, the same frequency ratio stated in the Latched FS[D:A] register will be used. When it is set, the frequency ratio stated in the FSEL[3:0] register will be used.
6	0	CPU_DAF_N[6]	
5	0	CPU_DAF_N[5]	
4	0	CPU_DAF_N[4]	
3	0	CPU_DAF_N[3]	
2	0	CPU_DAF_N[2]	
1	0	CPU_DAF_N[1]	
0	0	CPU_DAF_N[0]	

**Byte 13: CPU DAF Register2**

Bit	@Pup	Name	Description
7	0	CPU_DAF_N[8]	If Prog_CPU_EN is set, the values programmed in CPU_DAF_N[8:0] and CPU_DAF_M[6:0] will be used to determine the CPU output frequency. The setting of the FS_Override bit determines the frequency ratio for CPU and other output clocks. When it is cleared, the same frequency ratio stated in the Latched FS[D:A] register will be used. When it is set, the frequency ratio stated in the FSEL[3:0] register will be used.
6	0	CPU_DAF_M[6]	
5	0	CPU_DAF_M[5]	
4	0	CPU_DAF_M[4]	
3	0	CPU_DAF_M[3]	
2	0	CPU_DAF_M[2]	
1	0	CPU_DAF_M[1]	
0	0	CPU_DAF_M[0]	



**Byte 14: ATIG DAF Register1**

Bit	@Pup	Name	Description
7	0	ATIG_DAF_N[7]	If Prog_ATIG_EN is set, the values programmed in ATIG_DAF_N[8:0] will be used to determine the ATIG output frequency.
6	0	ATIG_DAF_N[6]	
5	0	ATIG_DAF_N[5]	
4	0	ATIG_DAF_N[4]	
3	0	ATIG_DAF_N[3]	
2	0	ATIG_DAF_N[2]	
1	0	ATIG_DAF_N[1]	
0	0	ATIG_DAF_N[0]	

**Byte 15: WDT Recovery Register**

Bit	@Pup	Name	Description
7	0	RECOVERY_N[7]	Used when RESET_IN# is asserted or the Watch Dog timer times out. This will be the safe value or last known good frequency of the CPU. It is set by the user before engaging in any overclocking exercise. M values revert to those set by the FS[C:A] pins
6	0	RECOVERY_N[6]	
5	0	RECOVERY_N[5]	
4	0	RECOVERY_N[4]	
3	0	RECOVERY_N[3]	
2	0	RECOVERY_N[2]	
1	0	RECOVERY_N[1]	
0	0	RECOVERY_N[0]	

**Byte 16: Overclocking Support Register**

Bit	@Pup	Name	Description
7	0	ATIG_N8	ATIG DAF bit N8
6	0	FS[C:A]	FS_override 0 = Select operating frequency by FS[C:A] input pins 1 = Select operating frequency by FSEL[C:A] register values
5	0	DF_EN	Dynamic Frequency enable for CPU frequencies 0 = Disable, 1 = Enable
4	0	Prog_SRC_EN	Enables the setting of SRC_PLL (PLL3) N values via byte 8 0 = Disable, 1 = Enable
3	0	Prog_ATIG_EN	Enables the setting of ATIG_PLL (PLL2) N values via byte 17 0 = Disable, 1 = Enable
2	0	Prog_CPU_EN	Enables the setting of CPU_PLL (PLL1) M and N values via byte 15 and 16 0 = Disable, 1 = Enable
1	0	Watchdog Autorecovery	Watchdog Autorecovery Mode 0 = Disable (manual), 1 = Enable (Auto)
0	0	Recovery_N8	CPU Safe recovery bit 8 for RESET_IN and Watchdog timer timeout.

**Table 5. Crystal Recommendations**

Frequency (Fund)	Cut	Loading	Load Cap	Drive (max.)	Shunt Cap (max.)	Motional (max.)	Tolerance (max.)	Stability (max.)	Aging (max.)
14.31818 MHz	AT	Parallel	20 pF	0.1 mW	5 pF	0.016 pF	35 ppm	30 ppm	5 ppm

**Crystal Recommendations**

The CY28RS600-2 requires a Parallel Resonance Crystal. Substituting a series resonance crystal will cause the CY28RS600-2 to operate at the wrong frequency and violate the ppm specification. For most applications there is a

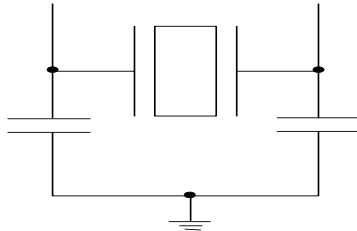
300-ppm frequency shift between series and parallel crystals due to incorrect loading.

**Crystal Loading**

Crystal loading plays a critical role in achieving low ppm performance. To realize low ppm performance, the total capacitance

the crystal will see must be considered to calculate the appropriate capacitive loading (CL).

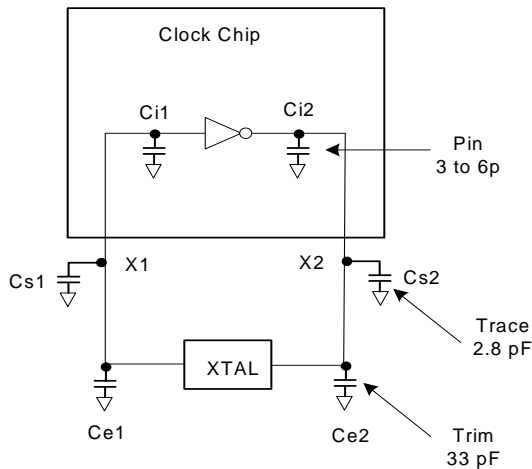
Figure 1 shows a typical crystal configuration using the two trim capacitors. An important clarification for the following discussion is that the trim capacitors are in series with the crystal not parallel. It's a common misconception that load capacitors are in parallel with the crystal and should be approximately equal to the load capacitance of the crystal. This is not true.



**Figure 1. Crystal Capacitive Clarification**

### Calculating Load Capacitors

In addition to the standard external trim capacitors, trace capacitance and pin capacitance must also be considered to correctly calculate crystal loading. As mentioned previously, the capacitance on each side of the crystal is in series with the crystal. This means the total capacitance on each side of the crystal must be twice the specified crystal load capacitance (CL). While the capacitance on each side of the crystal is in series with the crystal, trim capacitors (Ce1,Ce2) should be calculated to provide equal capacitive loading on both sides.



**Figure 2. Crystal Loading Example**

Use the following formulas to calculate the trim capacitor values for Ce1 and Ce2.

#### Load Capacitance (each side)

$$Ce = 2 * CL - (Cs + Ci)$$

#### Total Capacitance (as seen by the crystal)

$$CLe = \frac{1}{\left( \frac{1}{Ce1 + Cs1 + Ci1} + \frac{1}{Ce2 + Cs2 + Ci2} \right)}$$

- CL.....Crystal load capacitance
- CLe..... Actual loading seen by crystal using standard value trim capacitors
- Ce..... External trim capacitors
- Cs..... Stray capacitance (terraced)
- Ci ..... Internal capacitance (lead frame, bond wires etc.)

### CLK\_REQ[A:C]# Description

The CLKREQ#[A:C] signals are active LOW inputs used for clean stopping and starting selected SRC outputs. The CLKREQ# signal is a de-bounced signal in that its state must remain unchanged during two consecutive rising edges of DIFC to be recognized as a valid assertion or deassertion. (The assertion and deassertion of this signal is absolutely asynchronous.)

### CLK\_REQ[A:C]# Assertion

The impact of asserting the CLKREQ#[A:C] pins is that all DIF outputs that are set in the control registers to stoppable via assertion of CLKREQ#[A:C] are to be stopped after their next transition. The final state of all stopped DIF signals is Tristate, both SRCT clock and SRCC clock outputs will be driven Tristate.

### CLK\_REQ[A:C]# Deassertion

All differential outputs that were stopped are to resume normal operation in a glitch free manner. The maximum latency from the deassertion to active outputs is between 2 and 6 SRC clock periods (2 clocks are shown) with all SRC outputs resuming simultaneously.

### PD (Power-down) Clarification

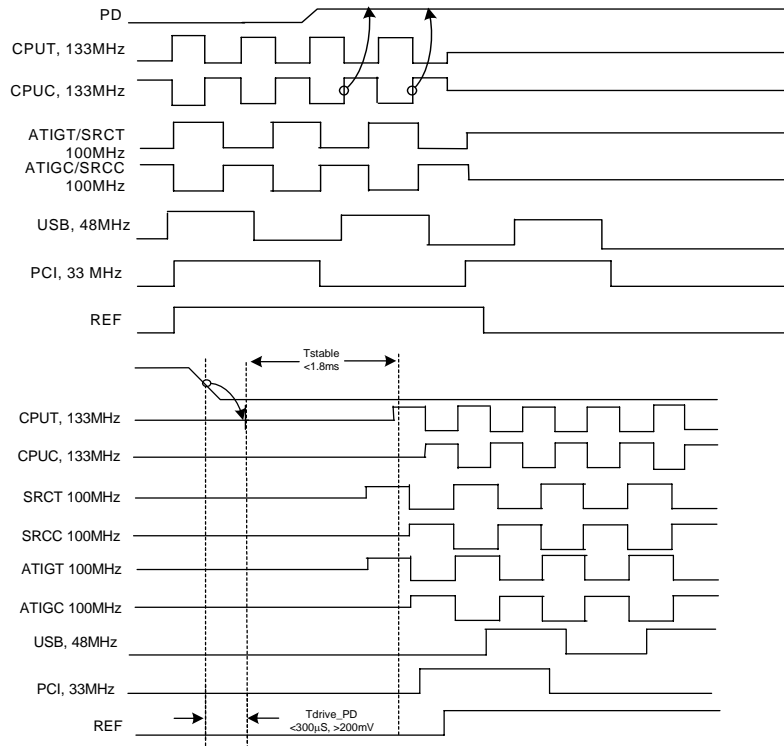
The VTT\_PWRGD# /PD pin is a dual-function pin. During initial power-up, the pin functions as VTT\_PWRGD#. Once VTT\_PWRGD# has been sampled LOW by the clock chip, the pin assumes PD functionality. The PD pin is an asynchronous active HIGH input used to shut off all clocks cleanly prior to shutting off power to the device. This signal is synchronized internal to the device prior to powering down the clock synthesizer. PD is also an asynchronous input for powering up the system. When PD is asserted HIGH, all clocks need to be driven to a LOW value and held prior to turning off the VCOs and the crystal oscillator.

### PD (Power-down) Assertion

When PD is sampled HIGH by two consecutive rising edges of CPUC, all single-ended outputs will be held LOW on their next HIGH-to-LOW transition and differential clocks must be held in tristate on the next diff clock# HIGH-to-LOW transition within four clock periods. Figure 3 and this description are applicable for all valid CPU frequencies. In the event that PD mode is desired as the initial power-on state, PD must be asserted HIGH in less than 10 μs after asserting Vtt\_PwrGd#.

### PD Deassertion

The power-up latency is less than 1.8 ms. This is the time from the deassertion of the PD pin or the ramping of the power supply until the time that stable clocks are output from the clock chip. All differential outputs stopped in a three-state condition resulting from power down will be driven high in less than 300 μs of PD deassertion to a voltage greater than



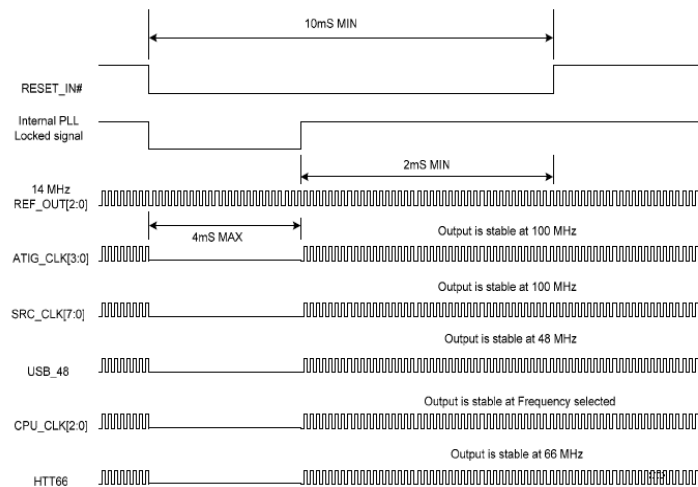
**Figure 3. PWRDWN Assertion/Deassertion Waveform**

200 mV. After the clock chip's internal PLL is powered up and locked, all outputs will be enabled within a few clock cycles of each other. *Figure 3* is an example showing the relationship of clocks coming up.

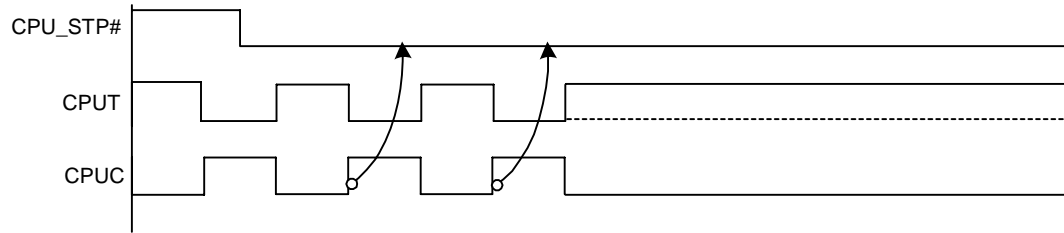
**RESET\_IN# Assertion**

The RESET\_IN# is a negative edge triggered signal. When asserted, all PLLs will revert back to a safe default frequency.

The clock output will be allowed to turn off for a maximum of 4 ms. After this time the PLLs will output a locked clock at a preselected safe frequency. The safe frequency is either based upon the power on reset default values or upon the value stored in the safe frequency register. The safe frequency register is accessible via SMBUS (Bytes 18 & 19). The clock outputs must be stable at the correct safe frequency at least 2 ms before the deassertion of RESET\_IN#.



**Figure 4. RESET\_IN# Assertion/Deassertion Waveform**



**Figure 5. CPU\_ST0P# Assertion Waveform**

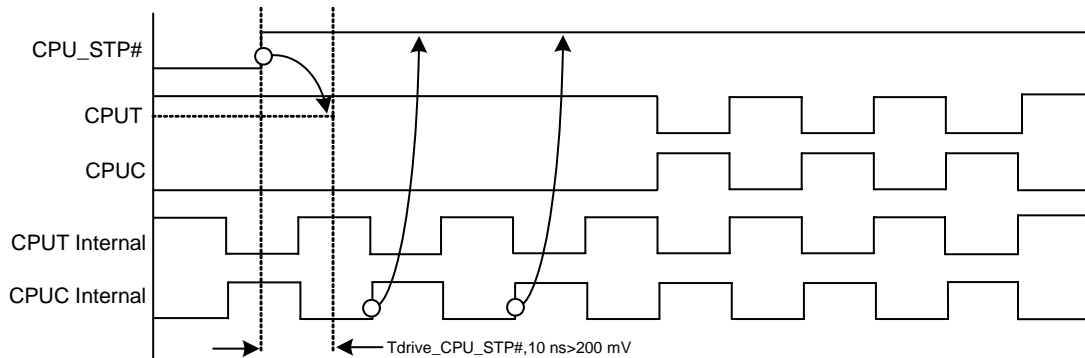
**CPU\_ST0P# Assertion**

The CPU\_ST0P# signal is an active LOW input used for synchronous stopping and starting the CPU output clocks while the rest of the clock generator continues to function. When the CPU\_ST0P# pin is asserted, all CPU outputs that are set with the SMBus configuration to be stoppable via assertion of CPU\_ST0P# will be stopped within two and six CPU clock periods after being sampled by two rising edges of the internal CPUC clock. The final states of the stopped CPU signals are CPUT = HIGH and CPUC = LOW. There is no

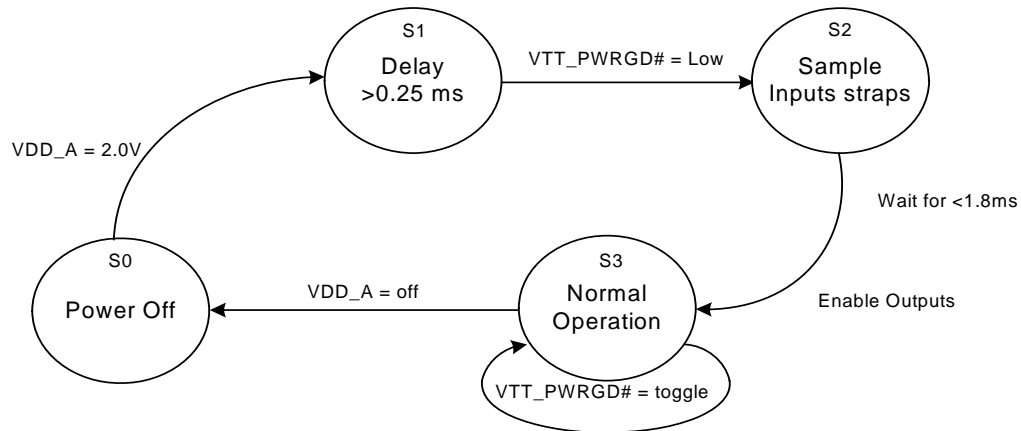
change to the output drive current values during the stopped state.

**CPU\_ST0P# Deassertion**

The deassertion of the CPU\_ST0P# signal will cause all CPU outputs that were stopped to resume normal operation in a synchronous manner, synchronous manner meaning that no short or stretched clock pulses will be produce when the clock resumes. The maximum latency from the deassertion to active outputs is 2 to 6 CPU clock cycles.



**Figure 6. CPU\_ST0P# Deassertion Waveform**



**Figure 7. Clock Generator Power-up/Run State Diagram**

**Absolute Maximum Conditions**

Parameter	Description	Condition	Min.	Max.	Unit
V <sub>DD</sub>	Core Supply Voltage		-0.5	4.6	V
V <sub>DDA</sub>	Analog Supply Voltage		-0.5	4.6	V
V <sub>IN</sub>	Input Voltage	Relative to V <sub>SS</sub>	-0.5	V <sub>DD</sub> + 0.5	VDC
T <sub>S</sub>	Temperature, Storage	Non-functional	-65	+150	°C
T <sub>A</sub>	Temperature, Operating Ambient	Functional	0	70	°C
T <sub>J</sub>	Temperature, Junction	Functional	-	150	°C
ESD <sub>HBM</sub>	ESD Protection (Human Body Model)	MIL-STD-883, Method 3015	2000	-	V
∅ <sub>JC</sub>	Dissipation, Junction to Case	Mil-Spec 883E Method 1012.1	-	20	°C/W
∅ <sub>JA</sub>	Dissipation, Junction to Ambient	JEDEC (JESD 51)	-	60	°C/W
UL-94	Flammability Rating	At 1/8 in.	V-0		
MSL	Moisture Sensitivity Level		1		

**Multiple Supplies:** The Voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

**DC Electrical Specifications**

Parameter	Description	Condition	Min.	Max.	Unit
VDD_REF, VDD_CPU, VDD_PCI, VDD_SRC, VDD_48	3.3V Operating Voltage	3.3V ± 5%	3.135	3.465	V
V <sub>ILSMBUS</sub>	Input Low Voltage	SDATA, SCLK	-	1.0	V
V <sub>IHSMBUS</sub>	Input High Voltage	SDATA, SCLK	2.2	-	V
V <sub>IL</sub>	Input Low Voltage	VDD	V <sub>SS</sub> - 0.3	0.8	V
V <sub>IH</sub>	Input High Voltage		2.0	V <sub>DD</sub> + 0.3	V
I <sub>IL</sub>	Input Leakage Current	Except Pull-ups or Pull-downs 0 < V <sub>IN</sub> < V <sub>DD</sub>	-5	5	mA
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 1 mA	-	0.4	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = 1 mA	2.4	-	V
I <sub>OZ</sub>	High-Impedance Output Current		-10	10	μA
C <sub>IN</sub>	Input Pin Capacitance		3	5	pF
C <sub>OUT</sub>	Output Pin Capacitance		3	5	pF
L <sub>IN</sub>	Pin Inductance		-	7	nH
V <sub>XIH</sub>	Xin High Voltage		0.7 * V <sub>DD</sub>	V <sub>DD</sub>	V
V <sub>XIL</sub>	Xin Low Voltage		0	0.3 * V <sub>DD</sub>	V
IDD	Dynamic Supply Current	At max load and frequency	-	250	mA
IPD <sub>T</sub>	Power Down Supply Current	PD asserted, Outputs Hi-Z	-	12	mA

**AC Electrical Specifications**

Parameter	Description	Condition	Min.	Max.	Unit
<b>Crystal</b>					
T <sub>DC</sub>	XIN Duty Cycle	The device will operate reliably with input duty cycles up to 30/70 but the REF clock duty cycle will not be within specification	47.5	52.5	%
T <sub>PERIOD</sub>	XIN Period	When XIN is driven from an external clock source	69.841	71.0	ns
T <sub>R</sub> / T <sub>F</sub>	XIN Rise and Fall Times	Measured between 0.3V <sub>DD</sub> and 0.7V <sub>DD</sub>	-	10.0	ns
T <sub>CCJ</sub>	XIN Cycle to Cycle Jitter	As an average over 1-μs duration	-	500	ps

**AC Electrical Specifications** (continued)

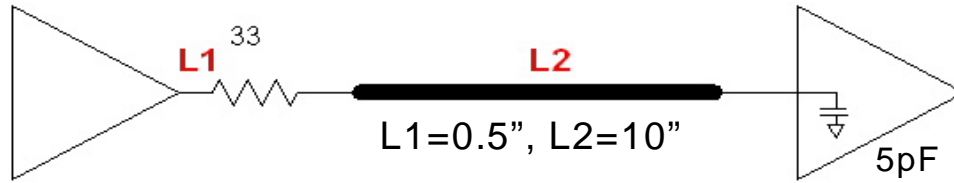
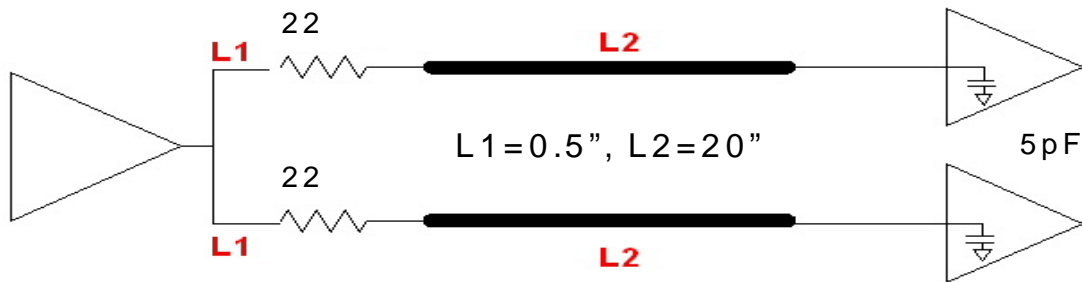
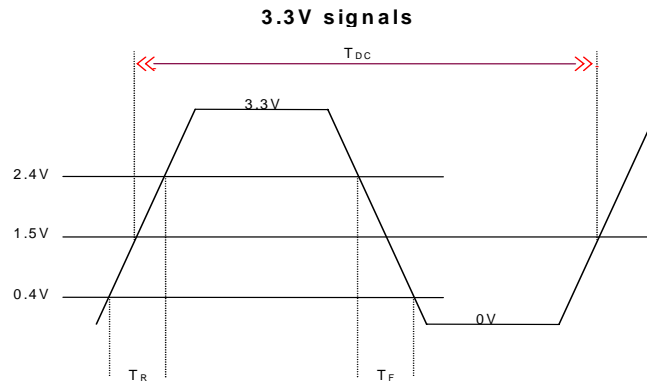
Parameter	Description	Condition	Min.	Max.	Unit
L <sub>ACC</sub>	Long-term Accuracy	Over 150 ms	–	300	ppm
<b>CPU at 0.7V</b>					
T <sub>DC</sub>	CPUT and CPUC Duty Cycle	Measured at crossing point V <sub>OX</sub>	45	55	%
T <sub>PERIOD</sub>	100-MHz CPUT and CPUC Period	Measured at crossing point V <sub>OX</sub>	9.997001	10.00300	ns
T <sub>PERIOD</sub>	133-MHz CPUT and CPUC Period	Measured at crossing point V <sub>OX</sub>	7.497751	7.502251	ns
T <sub>PERIOD</sub>	166-MHz CPUT and CPUC Period	Measured at crossing point V <sub>OX</sub>	5.9982	6.0018	ns
T <sub>PERIOD</sub>	200-MHz CPUT and CPUC Period	Measured at crossing point V <sub>OX</sub>	4.998500	5.001500	ns
T <sub>PERIOD</sub>	266-MHz CPUT and CPUC Period	Measured at crossing point V <sub>OX</sub>	3.748875	3.751125	ns
T <sub>PERIOD</sub>	333-MHz CPUT and CPUC Period	Measured at crossing point V <sub>OX</sub>	2.9991	3.0009	ns
T <sub>PERIOD</sub>	400-MHz CPUT and CPUC Period	Measured at crossing point V <sub>OX</sub>	2.4993	2.5008	ns
L <sub>ACC</sub>	CPUT/C Long Term Accuracy	Measured at crossing point V <sub>OX</sub>	–300	300	ppm
T <sub>CCJ</sub>	CPUT/C Cycle to Cycle Jitter	Measured at crossing point V <sub>OX</sub>	–	85	ps
T <sub>R</sub> / T <sub>F</sub>	CPUT and CPUC Rise and Fall Times	Measured from V <sub>OL</sub> = 0.175 to V <sub>OH</sub> = 0.525V	175	700	ps
T <sub>RFM</sub>	Rise/Fall Matching	Determined as a fraction of $2*(T_R - T_F)/(T_R + T_F)$	–	20	%
ΔT <sub>R</sub>	Rise Time Variation		–	125	ps
ΔT <sub>F</sub>	Fall Time Variation		–	125	ps
TSKEW	Any CPU to CPU Clock Skew	Measured at crossing point V <sub>OX</sub>	–	100	ps
V <sub>HIGH</sub>	Voltage High	Math averages <i>Figure 11</i>	660	850	mv
V <sub>LOW</sub>	Voltage Low	Math averages <i>Figure 11</i>	–150	–	mv
V <sub>OX</sub>	Crossing Point Voltage at 0.7V Swing		250	550	mv
V <sub>OVS</sub>	Maximum Overshoot Voltage		–	V <sub>HIGH</sub> + 0.3	V
V <sub>UDS</sub>	Minimum Undershoot Voltage		–0.3	–	V
V <sub>RB</sub>	Ring Back Voltage	See <i>Figure 11</i> . Measure SE	–	0.2	V
<b>SRC</b>					
T <sub>DC</sub>	SRCT and SRCC Duty Cycle	Measured at crossing point V <sub>OX</sub>	45	55	%
T <sub>PERIOD</sub>	100-MHz SRCT and SRCC Period	Measured at crossing point V <sub>OX</sub>	9.997001	10.00300	ns
T <sub>PERIODSS</sub>	100-MHz SRCT and SRCC Period, SSC	Measured at crossing point V <sub>OX</sub>	9.997001	10.05327	ns
T <sub>PERIODAbs</sub>	100-MHz SRCT and SRCC Absolute Period	Measured at crossing point V <sub>OX</sub>	10.12800	9.872001	ns
T <sub>PERIODSSAbs</sub>	100-MHz SRCT and SRCC Absolute Period, SSC	Measured at crossing point V <sub>OX</sub>	9.872001	10.17827	ns
T <sub>SKEW</sub>	Any SRCT/C to SRCT/C Clock Skew	Measured at crossing point V <sub>OX</sub>	–	250	ps
T <sub>CCJ</sub>	SRCT/C Cycle to Cycle Jitter	Measured at crossing point V <sub>OX</sub>	–	125	ps
L <sub>ACC</sub>	SRCT/C Long Term Accuracy	Measured at crossing point V <sub>OX</sub>	–300	300	ppm
T <sub>R</sub> / T <sub>F</sub>	SRCT and SRCC Rise and Fall Times	Measured from V <sub>OL</sub> = 0.175 to V <sub>OH</sub> = 0.525V	175	700	ps
T <sub>RFM</sub>	Rise/Fall Matching	Determined as a fraction of $2*(T_R - T_F)/(T_R + T_F)$	–	20	%
ΔT <sub>R</sub>	Rise Time Variation		–	125	ps
ΔT <sub>F</sub>	Fall Time Variation		–	125	ps
V <sub>HIGH</sub>	Voltage High	Math averages <i>Figure 11</i>	660	850	mv
V <sub>LOW</sub>	Voltage Low	Math averages <i>Figure 11</i>	–150	–	mv
V <sub>OX</sub>	Crossing Point Voltage at 0.7V Swing		250	550	mV
V <sub>OVS</sub>	Maximum Overshoot Voltage		–	V <sub>HIGH</sub> + 0.3	V
V <sub>UDS</sub>	Minimum Undershoot Voltage		–0.3	–	V

**AC Electrical Specifications** (continued)

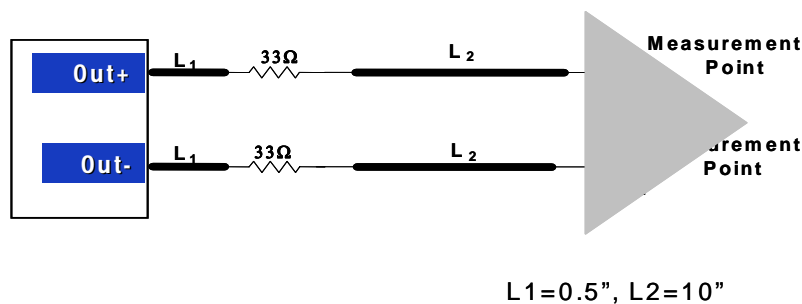
Parameter	Description	Condition	Min.	Max.	Unit
V <sub>RB</sub>	Ring Back Voltage	See Figure 11. Measure SE	–	0.2	V
<b>ATIG</b>					
T <sub>DC</sub>	ATIGT and ATIGC Duty Cycle	Measured at crossing point V <sub>OX</sub>	45	55	%
T <sub>PERIOD</sub>	100-MHz ATIGT and ATIGC Period	Measured at crossing point V <sub>OX</sub>	9.997001	10.00300	ns
T <sub>PERIODSS</sub>	100-MHz ATIGT and ATIGC Period, SSC	Measured at crossing point V <sub>OX</sub>	9.997001	10.05327	ns
T <sub>PERIODAbs</sub>	100-MHz ATIGT and ATIGC Absolute Period	Measured at crossing point V <sub>OX</sub>	10.12800	9.872001	ns
T <sub>PERIODSSAbs</sub>	100-MHz ATIGT and ATIGC Absolute Period, SSC	Measured at crossing point V <sub>OX</sub>	9.872001	10.17827	ns
T <sub>SKEW</sub>	Any ATIGT/C to ATIGT/C Clock Skew	Measured at crossing point V <sub>OX</sub>	–	250	ps
T <sub>CCJ</sub>	ATIGT/C Cycle to Cycle Jitter	Measured at crossing point V <sub>OX</sub>	–	125	ps
L <sub>ACC</sub>	ATIGT/C Long Term Accuracy	Measured at crossing point V <sub>OX</sub>	–300	300	ppm
T <sub>R</sub> / T <sub>F</sub>	ATIGT and ATIGC Rise and Fall Times	Measured from V <sub>OL</sub> = 0.175 to V <sub>OH</sub> = 0.525V	175	700	ps
T <sub>RFM</sub>	Rise/Fall Matching	Determined as a fraction of $2*(T_R - T_F)/(T_R + T_F)$	–	20	%
ΔT <sub>R</sub>	Rise Time Variation		–	125	ps
ΔT <sub>F</sub>	Fall Time Variation		–	125	ps
V <sub>HIGH</sub>	Voltage High	Math averages Figure 11	660	850	mv
V <sub>LOW</sub>	Voltage Low	Math averages Figure 11	–150	–	mv
V <sub>OX</sub>	Crossing Point Voltage at 0.7V Swing		250	550	mV
V <sub>OVS</sub>	Maximum Overshoot Voltage		–	V <sub>HIGH</sub> + 0.3	V
V <sub>UDS</sub>	Minimum Undershoot Voltage		–0.3	–	V
V <sub>RB</sub>	Ring Back Voltage	See Figure 11. Measure SE	–	0.2	V
<b>USB</b>					
T <sub>DC</sub>	Duty Cycle	Measurement at 1.5V	45	55	%
T <sub>PERIOD</sub>	Period	Measurement at 1.5V	20.83125	20.83542	ns
T <sub>PERIODAbs</sub>	Absolute Period	Measurement at 1.5V	20.48125	21.18542	ns
T <sub>HIGH</sub>	USB high time	Measurement at 2.4V	8.094	10.036	nS
T <sub>LOW</sub>	USB low time	Measurement at 0.4V	7.694	9.836	nS
T <sub>R</sub> / T <sub>F</sub>	Rise and Fall Times	Measured between 0.8V and 2.0V	1.0	2.0	ns
T <sub>CCJ</sub>	Cycle to Cycle Jitter	Measurement at 1.5V	–	300	ps
L <sub>ACC</sub>	USB Long Term Accuracy	Measurement at 1.5V	–100	100	ppm
T <sub>LTJ</sub>	Long Term Jitter	Measurement at 1.5V@1 μs	-	1000	ps
<b>REF</b>					
T <sub>DC</sub>	REF Duty Cycle	Measurement at 1.5V	45	55	%
T <sub>PERIOD</sub>	REF Period	Measurement at 1.5V	69.8203	69.8622	ns
T <sub>PERIODAbs</sub>	REF Absolute Period	Measurement at 1.5V	68.82033	70.86224	ns
T <sub>R</sub> / T <sub>F</sub>	REF Rise and Fall Times	Measured between 0.8V and 2.0V	1.0	4.0	V/ns
T <sub>CCJ</sub>	REF Cycle to Cycle Jitter	Measurement at 1.5V	–	500	ps
T <sub>LTJ</sub>	Long Term Jitter	Measurement at 1.5V@10 μs	-	500	ps
<b>ENABLE/DISABLE and SET-UP</b>					
T <sub>STABLE</sub>	Clock Stabilization from Power-up		–	1.8	ms
T <sub>SS</sub>	Stopclock Set-up Time		10.0	–	ns
T <sub>SH</sub>	Stopclock Hold Time		0	–	ns

**Test and Measurement Set-up**
**For PCI, USB Single-ended Signals and Reference**

The following diagram shows the test load configurations for the single-ended PCI, USB, and REF output signals.


**Figure 8. Single-ended PCI/USB Load Configuration**

**Figure 9. Single-ended REF Load Configuration**

**Figure 10. Single-ended Output Signals (for AC Parameters Measurement)**
**For all differential output signals**

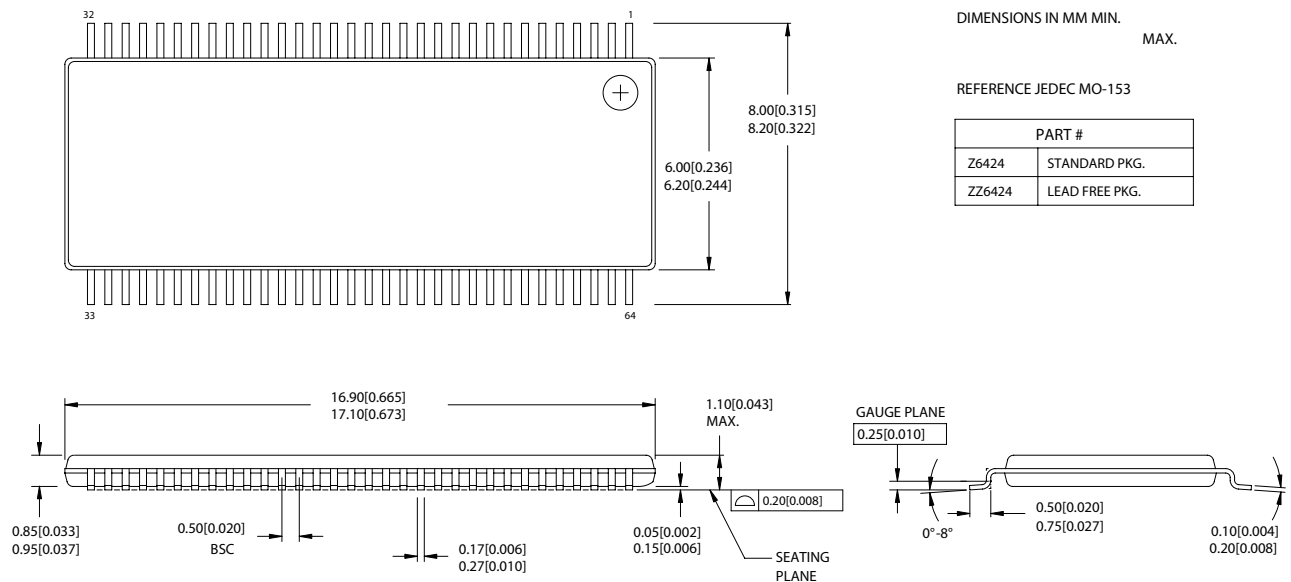
The following diagram shows the test load configuration for all differential outputs.


**Figure 11. 0.7V Load Configuration**



**Ordering Information**

Part Number	Package Type	Product Flow
<b>Lead-free</b>		
CY28RS600ZXC-2	64-pin TSSOP	Commercial, 0° to 70°C
CY28RS600ZXC-2T	64-pin TSSOP – Tape and Reel	Commercial, 0° to 70°C

**Package Drawing and Dimensions**
**64-Lead Thin Shrunken Small Outline Package (6 mm x 17 mm) Z64**


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