PRELIMINARY **CY28549**

Clock Generator for Intel® CK410M

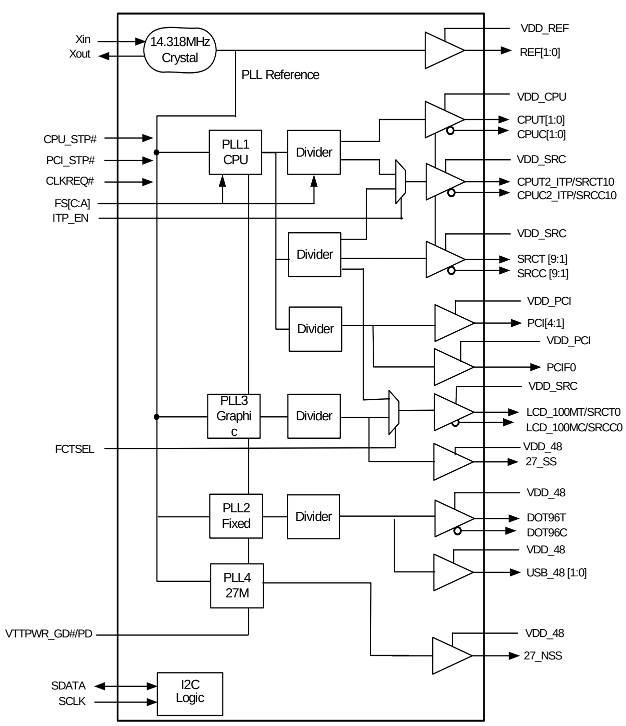
Features

- Compliant to Intel® CK410M
- Selectable CPU frequencies
- Low power differential CPU clock pairs
- 100-MHz low power differential SRC clocks
- 96-MHz low power differential dot clock
- 27-MHz Spread and Non-spread video clock
- 48-MHz USB clock
- SRC clocks independently stoppable through CLKREQ#[1:9]
- 96/100-MHz low power spreadable differential video clock
- 33-MHz PCI clocks
- Buffered Reference Clock 14.318 MHz
- Low-voltage frequency select inputs
- I^2C support with readback capabilities
- Ideal Lexmark Spread Spectrum profile for maximum electromagnetic interference (EMI) reduction
- 3.3V power supply
- 72-pin QFN package

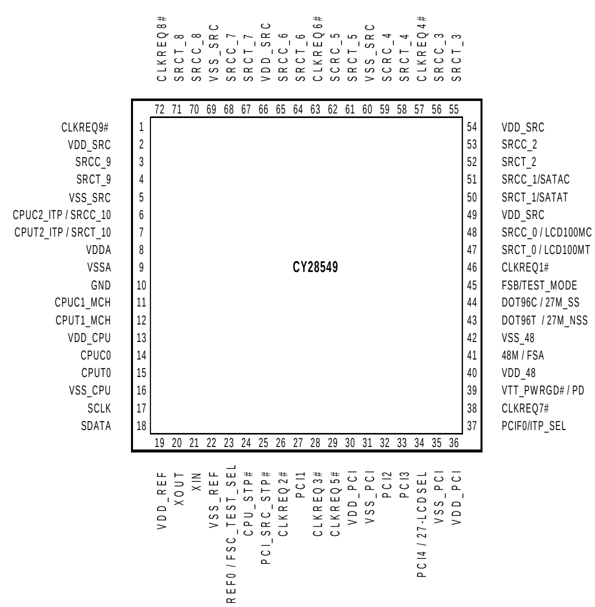
Table 1. Output Confguration Table

CPU	SRC	PCI	REF	DOT96	USB_48M	LCD	27M
x2/x3	x9/11	x5	x 2	x 1	x 1	x1	x2

Block Diagram



Pin Configuration



Pin Description

Pin No.	Name	Type	Description
1	CLKREQ9#	I	3.3V LVTTL input for enabling assigned SRC clock (active LOW).
2	VDD_SRC	PWR	3.3V power supply for outputs.
3	SRCC_9	O, DIF	Complementary 100-MHz Differential serial reference clocks.
4	SRCT_9	O, DIF	True 100-MHz Differential serial reference clocks.
5	VSS_SRC	GND	Ground for outputs.
6	CPUC2_ITP/SRCC10	O, DIF	Selectable Complementary differential CPU or SRC clock output. ITP_SEL = 0 @ VTTPWRGD#/PD assertion = SRC10 ITP_SEL = 1 @ VTTPWRGD#/PD assertion = CPU2
7	CPUT2_ITP/SRCT10,	O, DIF	Selectable True differential CPU or SRC clock output. ITP_SEL = 0 @ VTTPWRGD#/PD assertion = SRC10 ITP_SEL = 1 @ VTTPWRGD#/PD assertion = CPU2
8	VDDA	PWR	3.3V power supply for PLL.
9	VSSA	GND	Ground for PLL.
10	GND	GND	Ground for outputs.
11	CPUC1_MCH,	O, DIF	Complementary Differential CPU clock output to MCH
12	CPUT1_MCH,	O, DIF	True Differential CPU clock output to MCH
13	VDD_CPU	PWR	3.3V power supply for outputs.
14	CPUC0	O, DIF	Complementary Differential CPU clock output
15	CPUT0	O, DIF	True Differential CPU clock output
16	VSS_CPU	GND	Ground for outputs.
17	SCLK	I	SMBus-compatible SCLOCK.
18	SDATA	I/O, OD	SMBus-compatible SDATA.
19	VDD_REF	PWR	3.3V power supply for outputs.
20	XOUT	O, SE	14.318-MHz crystal output.
21	XIN	I	14.318-MHz crystal input.
22	VSS_REF	GND	Ground for outputs.
23	REF0/FSC_TESTSEL	I/O	Fixed 14.318 clock output/3.3V-tolerant input for CPU frequency selection/Selects test mode if pulled to V_{IMFS_C} when VTTPWRGD#/PD is asserted LOW. *Refer to DC Electrical Specifications table for* V_{ILFS_C},V_{IMFS_C},V_{IHFS_C} *specifications.*
24	CPU_STP#	I	3.3V LVTTL input for CPU_STP# active LOW
25	PCI_SRC_STP#	I	3.3V LVTTL input for PCI_STP# active LOW
26	CLKREQ2#	I	3.3V LVTTL input for enabling assigned SRC clock (active LOW).
27	PCI1	O, SE	33MHz clock output
28	CLKREQ3#	I	3.3V LVTTL input for enabling assigned SRC clock (active LOW).
29	CLKREQ5#	I	3.3V LVTTL input for enabling assigned SRC clock (active LOW).
30	VDD_PCI	PWR	3.3V power supply for outputs.
31	VSS_PCI	GND	Ground for outputs.
32	PCI2	O, SE	33-MHz clock output
33	PCI3	O, SE	33-MHz clock output

Pin Description (continued)

<table>
<tr><th>Pin No.</th><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>34</td><td>PCI4/FCTSEL1</td><td>I/O, SE,</td><td>33-MHz clock output/3.3V LVTTL input for selecting pins 47,48 (SRC[T/C]0, 100M[T/C]) and pins 43,44 (DOT96[T/C] and 27M Spread and Non-spread) (sampled on VTTPWRGD#/PD assertion).
<table>
<tr><th>FCTSEL1</th><th>Pin 43</th><th>Pin 44</th><th>Pin 47</th><th>Pin 48</th></tr>
<tr><td>0</td><td>DOT96T</td><td>DOT96C</td><td>96/100M_T</td><td>96/100M_C</td></tr>
<tr><td>1</td><td>27M_NSS</td><td>27M_SS</td><td>SRCT0</td><td>SRCC0</td></tr>
</table></td></tr>
<tr><td>35</td><td>VSS_PCI</td><td>GND</td><td>Ground for outputs.</td></tr>
<tr><td>36</td><td>VDD_PCI</td><td>PWR</td><td>3.3V power supply for outputs.</td></tr>
<tr><td>37</td><td>ITP_SEL/PCIF0</td><td>I/O, SE</td><td>3.3V LVTTL input to enable SRC10 or CPU2_ITP/33-MHz clock output. (sampled on VTTPWRGD#/PD assertion).
1 = CPU2_ITP, 0 = SRC10</td></tr>
<tr><td>38</td><td>CLKREQ7#</td><td>I</td><td>3.3V LVTTL input for enabling assigned SRC clock (active LOW).</td></tr>
<tr><td>39</td><td>VTT_PWRGD#/PD</td><td>I</td><td>3.3V LVTTL input. This pin is a level sensitive strobe. it latches data on the FSA, FSB, FSC, FCTSEL1 and ITP_SEL pins. After assertion, it becomes a real time input for controlling power down.</td></tr>
<tr><td>40</td><td>VDD_48</td><td>PWR</td><td>3.3V power supply for outputs.</td></tr>
<tr><td>41</td><td>48M/FSA</td><td>I/O</td><td>Fixed 48-MHz clock output/3.3V-tolerant input for CPU frequency selection
Refer to DC Electrical Specifications table for Vil_FS and Vih_FS specifications.</td></tr>
<tr><td>42</td><td>VSS_48</td><td>GND</td><td>Ground for outputs.</td></tr>
<tr><td>43</td><td>DOT96T/ 27M_NSS</td><td>O, DIF</td><td>True Fixed 96-MHz clock output or 27 Mhz Spread and Non-spread output Selected via FCTSEL1 at VTTPWRGD#/PD assertion.</td></tr>
<tr><td>44</td><td>DOT96C/ 27M_SS</td><td>O, DIF</td><td>Complementary Fixed 96-MHz clock output or 27 Mhz Spread and Non-spread output Selected via FCTSEL1 at VTTPWRGD#/PD assertion.</td></tr>
<tr><td>45</td><td>FSB/TEST_MODE</td><td>I</td><td>3.3V-tolerant input for CPU frequency selection. Selects Ref/N or Tri-state when in test mode
0 = Tri-state, 1 = Ref/N
Refer to DC Electrical Specifications table for Vil_FS and Vih_FS specifications.</td></tr>
<tr><td>46</td><td>CLKREQ6#</td><td>I</td><td>3.3V LVTTL input for enabling assigned SRC clock (active LOW).</td></tr>
<tr><td>47</td><td>SRCT_0/
LCD100MT</td><td>O,DIF</td><td>True 100-MHz differential serial reference clock output/Differential 96/100-MHz SS clock for flat-panel display
Selected via FCTSEL1 at VTTPWRGD#/PD assertion.</td></tr>
<tr><td>48</td><td>SRCC0/
LCD100MC</td><td>O,DIF</td><td>Complementary 100-MHz differential serial reference clock output/Differential 96/100-MHz SS clock for flat-panel display
Selected via FCTSEL1 at VTTPWRGD#/PD assertion.</td></tr>
<tr><td>49</td><td>VDD_SRC</td><td>PWR</td><td>3.3V power supply for outputs.</td></tr>
<tr><td>50</td><td>SRCT_1/SATAT,</td><td>O, DIF</td><td>True 100-MHz Differential serial reference clocks.</td></tr>
<tr><td>51</td><td>SRCC_1/SATAC</td><td>O, DIF</td><td>Complementary 100-MHz Differential serial reference clocks.</td></tr>
<tr><td>52</td><td>SRCT_2</td><td>O, DIF</td><td>True 100-MHz Differential serial reference clocks.</td></tr>
<tr><td>53</td><td>SRCC_2</td><td>O, DIF</td><td>Complementary 100-MHz Differential serial reference clocks.</td></tr>
<tr><td>54</td><td>VDD_SRC</td><td>PWR</td><td>3.3V power supply for outputs.</td></tr>
<tr><td>55</td><td>SRCT_3</td><td>O, DIF</td><td>True 100-MHz Differential serial reference clocks.</td></tr>
<tr><td>56</td><td>SRCC_3</td><td>O, DIF</td><td>Complementary 100-MHz Differential serial reference clocks.</td></tr>
<tr><td>57</td><td>CLKREQ4#</td><td>I</td><td>3.3V LVTTL input for enabling assigned SRC clock (active LOW).</td></tr>
<tr><td>58</td><td>SRCT_4</td><td>O, DIF</td><td>True 100-MHz Differential serial reference clocks.</td></tr>
<tr><td>59</td><td>SRCC_4</td><td>O, DIF</td><td>Complementary 100-MHz Differential serial reference clocks.</td></tr>
<tr><td>60</td><td>VSS_SRC</td><td>GND</td><td>Ground for outputs.</td></tr>
<tr><td>61</td><td>SRCT_5</td><td>O, DIF</td><td>True 100-MHz Differential serial reference clocks.</td></tr>
</table>

Pin Description (continued)

Pin No.	Name	Type	Description
62	SRCC_5	O, DIF	Complementary 100-MHz Differential serial reference clocks.
63	CLKREQ6#	I	3.3V LVTTL input for enabling assigned SRC clock (active LOW).
64	SRCT_6	O, DIF	True 100-MHz Differential serial reference clocks.
65	SRCC_6	O, DIF	Complementary 100-MHz Differential serial reference clocks.
66	VDD_SRC	PWR	3.3V power supply for outputs.
67	SRCT_7	O, DIF	True 100-MHz Differential serial reference clocks.
68	SRCC_7	O, DIF	Complementary 100-MHz Differential serial reference clocks.
69	VSS_SRC	GND	Ground for outputs.
70	SRCC_8	O, DIF	Complementary 100-MHz Differential serial reference clocks.
71	SRCT_8	O, DIF	True 100-MHz Differential serial reference clocks.
72	CLKREQ8#	I	3.3V LVTTL input for enabling assigned SRC clock (active LOW).

Frequency Select Pins (FSA, FSB, and FSC)

Host clock frequency selection is achieved by applying the appropriate logic levels to FSA, FSB, FSC inputs prior to VTT_PWRGD# assertion (as seen by the clock synthesizer). Upon VTT_PWRGD# being sampled LOW by the clock chip (indicating processor VTT voltage is stable), the clock chip samples the FSA, FSB, and FSC input values. For all logic levels of FSA, FSB, and FSC, VTT_PWRGD# employs a one-shot functionality in that once a valid LOW on VTT_PWRGD# has been sampled, all further VTT_PWRGD#, FSA, FSB, and FSC transitions will be ignored, except in test mode.

Serial Data Interface

To enhance the flexibility and function of the clock synthesizer, a two-signal serial interface is provided. Through the Serial Data Interface, various device functions, such as individual clock output buffers, can be individually enabled or disabled. The registers associated with the Serial Data Interface initialize to their default setting upon power-up, and therefore use of this interface is optional. Clock device register changes are normally made upon system initialization, if any are required. The interface cannot be used during system operation for power management functions.

Data Protocol

The clock driver serial protocol accepts byte write, byte read, block write, and block read operations from the controller. For block write/read operation, the bytes must be accessed in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after any complete byte has been transferred. For byte write and byte read operations, the system controller can access individually indexed bytes. The offset of the indexed byte is encoded in the command code, as described in *Table 3*.

The block write and block read protocol is outlined in *Table 4* while *Table 5* outlines the corresponding byte write and byte read protocol. The slave receiver address is 11010010 (D2h)

Table 2. Frequency Select Table FSA, FSB, and FSC

FSC	FSB	FSA	CPU	SRC	PCIF/PCI	27MHz	REF	DOT96	USB
1	0	1	100 MHz	100 MHz	33 MHz	27 MHz	14.318 MHz	96 MHz	48 MHz
0	0	1	133 MHz	100 MHz	33 MHz	27 MHz	14.318 MHz	96 MHz	48 MHz
0	1	1	166 MHz	100 MHz	33 MHz	27 MHz	14.318 MHz	96 MHz	48 MHz
0	1	0	200 MHz	100 MHz	33 MHz	27 MHz	14.318 MHz	96 MHz	48 MHz

Table 3. Command Code Definition

Bit	Description
7	0 = Block read or block write operation, 1 = Byte read or byte write operation
(6:0)	Byte offset for byte read or byte write operation. For block read or block write operations, these bits should be '0000000'

Table 4. Block Read and Block Write Protocol

Block Write Protocol		Block Read Protocol	
Bit	Description	Bit	Description
1	Start	1	Start
8:2	Slave address–7 bits	8:2	Slave address–7 bits
9	Write	9	Write

Table 4. Block Read and Block Write Protocol (continued)

Block Write Protocol		Block Read Protocol	
Bit	Description	Bit	Description
10	Acknowledge from slave	10	Acknowledge from slave
18:11	Command Code–8 bits	18:11	Command Code–8 bits
19	Acknowledge from slave	19	Acknowledge from slave
27:20	Byte Count–8 bits (Skip this step if I^{2}C_EN bit set)	20	Repeat start
28	Acknowledge from slave	27:21	Slave address–7 bits
36:29	Data byte 1–8 bits	28	Read = 1
37	Acknowledge from slave	29	Acknowledge from slave
45:38	Data byte 2–8 bits	37:30	Byte Count from slave–8 bits
46	Acknowledge from slave	38	Acknowledge
....	Data Byte/Slave Acknowledges	46:39	Data byte 1 from slave–8 bits
....	Data Byte N–8 bits	47	Acknowledge
....	Acknowledge from slave	55:48	Data byte 2 from slave–8 bits
....	Stop	56	Acknowledge
		....	Data bytes from slave/Acknowledge
		....	Data Byte N from slave–8 bits
		....	NOT Acknowledge
		....	Stop

Table 5. Byte Read and Byte Write Protocol

Byte Write Protocol		Byte Read Protocol	
Bit	Description	Bit	Description
1	Start	1	Start
8:2	Slave address–7 bits	8:2	Slave address–7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
18:11	Command Code–8 bits	18:11	Command Code–8 bits
19	Acknowledge from slave	19	Acknowledge from slave
27:20	Data byte–8 bits	20	Repeated start
28	Acknowledge from slave	27:21	Slave address–7 bits
29	Stop	28	Read
		29	Acknowledge from slave
		37:30	Data from slave–8 bits
		38	NOT Acknowledge
		39	Stop

Control Registers

Byte 0 Control Register 0

Bit	@Pup	Name	Description
7	0	RESEREVD	RESERVED
6	0	RESEREVD	RESERVED
5	0	RESEREVD	RESERVED
4	0	RESEREVD	RESERVED

Control Registers

Byte 0 Control Register 0

Bit	@Pup	Name	Description
3	0	RESEREVD	RESERVED
2	0	RESEREVD	RESERVED
1	0	RESEREVD	RESERVED
0	1	RESEREVD	RESERVED

Byte 1 Control Register 1

Bit	@Pup	Name	Description
7	1	SRC[T/C]7	SRC[T/C]7 Output Enable 0 = Disabled, 1 = Enabled
6	1	SRC[T/C]6	SRC[T/C]6 Output Enable 0 = Disabled, 1 = Enabled
5	1	SRC[T/C]5	SRC[T/C]5 Output Enable 0 = Disabled, 1 = Enabled
4	1	SRC[T/C]4	SRC[T/C]4 Output Enable 0 = Disabled, 1 = Enabled
3	1	SRC[T/C]3	SRC[T/C]3 Output Enable 0 = Disabled, 1 = Enabled
2	1	SRC[T/C]2	SRC[T/C]2 Output Enable 0 = Disabled, 1 = Enabled
1	1	SRC[T/C]1	SRC[T/C]1 Output Enable 0 = Disabled, 1 = Enabled
0	1	SRC[T/C]0 /LCD_96_100M[T/C]	SRC[T/C]0/LCD_96_100M[T/C] Output Enable 0 = Disabled, 1 = Enabled

Byte 2 Control Register 2

Bit	@Pup	Name	Description
7	1	PCIF0	PCIF0 Output Enable 0 = Disabled, 1 = Enabled
6	1	27M NSS/DOT_96[T/C]	27M Non-spread and DOT_96 MHz Output Enable 0 = Disable, 1 = Enabled
5	1	48M	48-MHz Output Enable 0 = Disabled, 1 = Enabled
4	1	REF0	REF0 Output Enable 0 = Disabled, 1 = Enabled
3	1	RESERVED	RESERVED
2	1	CPU[T/C]1	CPU[T/C]1 Output Enable 0 = Disabled, 1 = Enabled
1	1	CPU[T/C]0	CPU[T/C]0 Output Enable 0 = Disabled, 1 = Enabled
0	1	CPU, SRC, PCI, PCIF Spread Enable	PLL1 (CPU PLL) Spread Spectrum Enable 0 = Spread off, 1 = Spread on

Byte 3 Control Register 3

Bit	@Pup	Name	Description
7	1	PCI4	PCI4 Output Enable 0 = Disabled, 1 = Enabled
6	1	PCI3	PCI3 Output Enable 0 = Disabled, 1 = Enabled
5	1	PCI2	PCI2 Output Enable 0 = Disabled, 1 = Enabled

Byte 3 Control Register 3

Bit	@Pup	Name	Description
4	1	PCI1	PCI1 Output Enable 0 = Disabled, 1 = Enabled
3	1	RESERVED	RESERVED
2	1	RESERVED	RESERVED
1	1	CPU[T/C]2/SRC[T/C]10	CPU[T/C]2/SRC[T/C]10 Output Enable 0 = Disabled, 1 = Enabled
0	1	RESERVED	RESERVED

Byte 4 Control Register 4

Bit	@Pup	Name	Description
7	0	SRC7	Allow control of SRC[T/C]7 with assertion of PCI_STP# or SW PCI_STP# 0 = Free running, 1 = Stopped with PCI_STP#
6	0	SRC6	Allow control of SRC[T/C]6 with assertion of PCI_STP# or SW PCI_STP# 0 = Free running, 1 = Stopped with PCI_STP#
5	0	SRC5	Allow control of SRC[T/C]5 with assertion of PCI_STP# or SW PCI_STP# 0 = Free running, 1 = Stopped with PCI_STP#
4	0	SRC4	Allow control of SRC[T/C]4 with assertion of PCI_STP# or SW PCI_STP# 0 = Free running, 1 = Stopped with PCI_STP#
3	0	SRC3	Allow control of SRC[T/C]3 with assertion of PCI_STP# or SW PCI_STP# 0 = Free running, 1 = Stopped with PCI_STP#
2	0	SRC2	Allow control of SRC[T/C]2 with assertion of PCI_STP# or SW PCI_STP# 0 = Free running, 1 = Stopped with PCI_STP#
1	0	SRC1	Allow control of SRC[T/C]1 with assertion of PCI_STP# or SW PCI_STP# 0 = Free running, 1 = Stopped with PCI_STP#
0	0	SRC0	Allow control of SRC[T/C]0 with assertion of PCI_STP# or SW PCI_STP# 0 = Free running, 1 = Stopped with PCI_STP#

Byte 5 Control Register 5

Bit	@Pup	Name	Description
7	0	LCD_96_100M[T/C]	LCD_96_100M[T/C] PWRDWN Drive Mode 0 = Driven in PWRDWN, 1 = Tri-state
6	0	DOT96[T/C]	DOT PWRDWN Drive Mode 0 = Driven in PWRDWN, 1 = Tri-state
5	0	RESERVED	RESERVED, Set = 0
4	0	RESERVED	RESERVED, Set = 0
3	0	PCIF0	Allow control of PCIF0 with assertion of SW and HW PCI_STP# 0 = Free running, 1 = Stopped with PCI_STP#
2	1	CPU[T/C]2	Allow control of CPU[T/C]2 with assertion of CPU_STP# 0 = Free running, 1 = Stopped with CPU_STP#
1	1	CPU[T/C]1	Allow control of CPU[T/C]1 with assertion of CPU_STP# 0 = Free running, 1 = Stopped with CPU_STP#
0	1	CPU[T/C]0	Allow control of CPU[T/C]0 with assertion of CPU_STP# 0 = Free running, 1 = Stopped with CPU_STP#

Byte 6 Control Register 6

Bit	@Pup	Name	Description
7	0	SRC[T/C]	SRC[T/C] Stop Drive Mode 0 = Driven when PCI_STP# asserted 1 = Tri-state when PCI_STP# asserted
6	0	CPU[T/C]2	CPU[T/C]2 Stop Drive Mode 0 = Driven when CPU_STP# asserted 1 = Tri-state when CPU_STP# asserted

Byte 6 Control Register 6

5	0	CPU[T/C]1	CPU[T/C]1 Stop Drive Mode 0 = Driven when CPU_STP# asserted 1 = Tri-state when CPU_STP# asserted
4	0	CPU[T/C]0	CPU[T/C]0 Stop Drive Mode 0 = Driven when CPU_STP# asserted 1 = Tri-state when CPU_STP# asserted
3	0	SRC[T/C][9:1]	SRC[T/C][9:1] PWRDWN Drive Mode 0 = Driven when PD asserted 1 = Tri-state when PD asserted
2	0	CPU[T/C]2	CPU[T/C]2 PWRDWN Drive Mode 0 = Driven when PD asserted 1 = Tri-state when PD asserted
1	0	CPU[T/C]1	CPU[T/C]1 PWRDWN Drive Mode 0 = Driven when PD asserted 1 = Tri-state when PD asserted
0	0	CPU[T/C]0	CPU[T/C]0 PWRDWN Drive Mode 0 = Driven when PD asserted 1 = Tri-state when PD asserted

Byte 7 Control Register 7

Bit	@Pup	Name	Description
7	0	TEST_SEL	REF/N or Tri-state Select 0 = Tri-state, 1 = REF/N Clock
6	0	TEST_MODE	Test Clock Mode Entry Control 0 = Normal operation, 1 = REF/N or Tri-state mode,
5	1	RESEREVD	RESERVED
4	1	REF0	REF0 Output Drive Strength 0 = Low, 1 = High
3	1	PCI, PCIF and SRC clock outputs except those set to free running	SW PCI_STP Function 0 = SW PCI_STP assert, 1= SW PCI_STP deassert When this bit is set to 0, all STOPPABLE PCI, PCIF and SRC outputs will be stopped in a synchronous manner with no short pulses. When this bit is set to 1, all STOPPED PCI, PCIF and SRC outputs will resume in a synchronous manner with no short pulses.
2	HW	FSC	FSC Reflects the value of the FSC pin sampled on power up 0 = FSC was low during VTT_PWRGD# assertion
1	HW	FSB	FSB Reflects the value of the FSB pin sampled on power up 0 = FSB was low during VTT_PWRGD# assertion
0	HW	FSA	FSA Reflects the value of the FSA pin sampled on power up 0 = FSA was low during VTT_PWRGD# assertion

Byte 8 Vendor ID

Bit	@Pup	Name	Description
7	0	Revision Code Bit 3	Revision Code Bit 3
6	1	Revision Code Bit 2	Revision Code Bit 2
5	0	Revision Code Bit 1	Revision Code Bit 1
4	1	Revision Code Bit 0	Revision Code Bit 0
3	1	Vendor ID Bit 3	Vendor ID Bit 3
2	0	Vendor ID Bit 2	Vendor ID Bit 2
1	0	Vendor ID Bit 1	Vendor ID Bit 1
0	0	Vendor ID Bit 0	Vendor ID Bit 0

Byte 9 Control Register 9

Bit	@Pup	Name	Description

Byte 9 Control Register 9

7	0	RESERVED	RESERVED, Set = 0
6	0	RESERVED	RESERVED, Set = 0
5	0	RESERVED	RESERVED
4	0	RESERVED	RESERVED
3	0	RESERVED	RESERVED
2	1	48M	48-MHz Output Drive Strength 0 = Low, 1 = High
1	1	RESERVED	RESERVED
0	1	PCIF0	PCIF0 Output Drive Strength 0 = Low, 1 = High

Byte 10 Control Register 10

Bit	@Pup	Name	Description
7	0	RESERVED	RESERVED
6	0	RESERVED	RESERVED
5	0	S1	27M_SS/LCD 96_100M SS Spread Spectrum Selection table: S[1:0] SS% ‘00’ = –0.5%(Default value) ‘01’ = –1.0% ‘10’ = –1.5% ‘11’ = –2.0%
4	0	S0	
3	1	RESERVED	RESERVED
2	1	27M_SS	27M Spread Output Enable 0 = Disabled, 1 = Enabled
1	1	27M_SS/LCD_100M Spread Enable	27M_SS/LCD_100M Spread spectrum enable. 0 = Disabled, 1 = Enabled
0	0	RESERVED	RESERVED

Byte 11 Control Register 11

Bit	@Pup	Name	Description
7	0	RESERVED	RESERVED
6	0	RESERVED	RESERVED
5	1	SRC[T/C]9	SRC[T/C]9 Output Enable 0 = Disable (Hi-Z), 1 = Enable
4	1	SRC[T/C]8	SRC[T/C]8 Output Enable 0 = Disable (Hi-Z), 1 = Enable
3	1	RESERVED	RESERVED
2	0	SRC[T/C]10	Allow control of SRC[T/C]10 with assertion of SW PCI_STP# 0 = Free running, 1 = Stopped with PCI_STP#
1	0	SRC[T/C]9	Allow control of SRC[T/C]9 with assertion of SW PCI_STP# 0 = Free running, 1 = Stopped with PCI_STP#
0	0	SRC[T/C]8	Allow control of SRC[T/C]8 with assertion of SW PCI_STP# 0 = Free running, 1 = Stopped with PCI_STP#

Byte 12 Control Register 12

Bit	@Pup	Name	Description
7	0	RESERVED	RESERVED, Set = 0
6	HW	RESERVED	RESERVED
5	HW	RESERVED	RESERVED
4	HW	RESERVED	RESERVED

Byte 12 Control Register 12

Bit	@Pup	Name	Description
3	1	27M_SS/27M_NSS	27-MHz (spread and non-spread) Output Drive Strength 0 = Low, 1 = High
2	0	RESERVED	RESERVED
1	1	RESERVED	RESERVED, Set = 1
0	HW	RESERVED	RESERVED

Byte 13 Control Register 13

Bit	@Pup	Name	Description
7	0	CLKREQ#9	CLKREQ#9 Input Enable 0 = Disabled, 1 = Enabled
6	0	CLKREQ#8	CLKREQ#8 Input Enable 0 = Disabled, 1 = Enabled
5	0	CLKREQ#7	CLKREQ#7 Input Enable 0 = Disabled, 1 = Enabled
4	0	CLKREQ#6	CLKREQ#6 Input Enable 0 = Disabled, 1 = Enabled
3	0	CLKREQ#5	CLKREQ#5 Input Enable 0 = Disabled, 1 = Enabled
2	0	CLKREQ#4	CLKREQ#4 Input Enable 0 = Disabled, 1 = Enabled
1	0	CLKREQ#3	CLKREQ#3 Input Enable 0 = Disabled, 1 = Enabled
0	0	CLKREQ#2	CLKREQ#2 Input Enable 0 = Disabled, 1 = Enabled

Byte 14 Control Register 14

Bit	@Pup	Name	Description
7	0	CLKREQ#1	CLKREQ#1 Input Enable 0 = Disabled, 1 = Enabled
6	1	LCD 96_100M Clock Speed	LCD 96_100M Clock Speed 0 = 96 MHz 1 = 100 MHz
5	1	RESERVED	RESERVED, Set = 1
4	1	RESERVED	RESERVED, Set = 1
3	1	PCI4	PCI4 (Spread and Non-spread) Output Drive Strength 0 = Low, 1 = High
2	1	PCI3	PCI3 (Spread and Non-spread) Output Drive Strength 0 = Low, 1 = High
1	1	PCI2	PCI2 (Spread and Non-spread) Output Drive Strength 0 = Low, 1 = High
0	1	PCI1	PCI1 (Spread and Non-spread) Output Drive Strength 0 = Low, 1 = High

Byte 15 Control Register 15

Bit	@Pup	Name	Description
7	HW	RESEREVD	RESERVED
6	1	RESERVED	RESERVED
5	1	RESERVED	RESERVED
4	1	RESERVED	RESERVED
3	1	RESERVED	RESERVED

Byte 15 Control Register 15

Bit	@Pup	Name	Description
2	1	IO_VOUT2	IO_VOUT[2,1,0] 000 = 0.63V 001 = 0.71V 010 = 0.77V 011 = 0.82V (Default) 100 = 0.86V 101 = 0.90V 110 = 0.93V 111 = Reserved
1	0	IO_VOUT1	
0	1	IO_VOUT0	

Table 6. Crystal Recommendations

Frequency (Fund)	Cut	Loading	Load Cap	Drive (max.)	Shunt Cap (max.)	Motional (max.)	Tolerance (max.)	Stability (max.)	Aging (max.)
14.31818 MHz	AT	Parallel	20 pF	0.1 mW	5 pF	0.016 pF	35 ppm	30 ppm	5 ppm

The CY28549 requires a Parallel Resonance Crystal. Substituting a series resonance crystal will cause the CY28549 to operate at the wrong frequency and violate the ppm specification. For most applications there is a 300-ppm frequency shift between series and parallel crystals due to incorrect loading.

Crystal Loading

Crystal loading plays a critical role in achieving low ppm performance. To realize low ppm performance, the total capacitance the crystal will see must be considered to calculate the appropriate capacitive loading (CL).

Figure 1 shows a typical crystal configuration using the two trim capacitors. An important clarification for the following discussion is that the trim capacitors are in series with the crystal not parallel. It's a common misconception that load capacitors are in parallel with the crystal and should be approximately equal to the load capacitance of the crystal. This is not true.

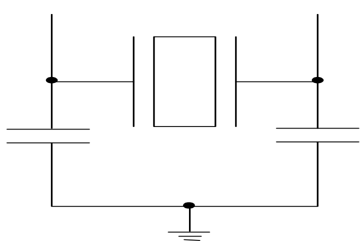


Figure 1. Crystal Capacitive Clarification

Calculating Load Capacitors

In addition to the standard external trim capacitors, trace capacitance and pin capacitance must also be considered to correctly calculate crystal loading. As mentioned previously, the capacitance on each side of the crystal is in series with the crystal. This means the total capacitance on each side of the crystal must be twice the specified crystal load capacitance (CL). While the capacitance on each side of the crystal is in series with the crystal, trim capacitors (Ce1,Ce2) should be calculated to provide equal capacitive loading on both sides.

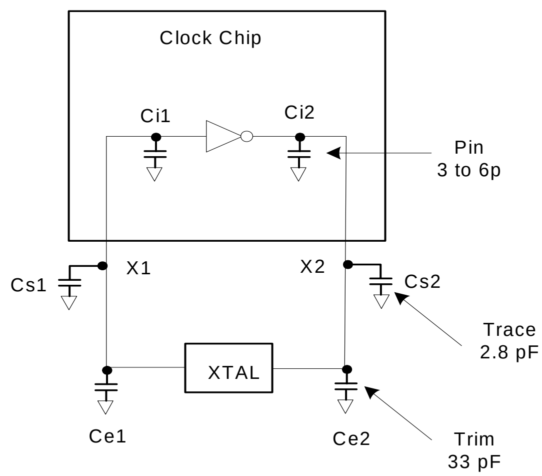


Figure 2. Crystal Loading Example

Use the following formulas to calculate the trim capacitor values for Ce1 and Ce2.

Load Capacitance (each side)

$$\boldsymbol{Ce} = 2 * CL - (Cs + Ci)$$

Total Capacitance (as seen by the crystal)

$$\boldsymbol{CLe} = \frac{1}{\left(\frac{1}{Ce1 + Cs1 + Ci1} + \frac{1}{Ce2 + Cs2 + Ci2}\right)}$$

CL ....Crystal load capacitance

CLe ....Actual loading seen by crystal using standard value trim capacitors

Ce ....External trim capacitors

Cs ....Stray capacitance (terraced)

Ci .... Internal capacitance (lead frame, bond wires etc.)

CLK_REQ# Description

The CLKREQ# signals are active LOW inputs used for clean enabling and disabling selected SRC outputs. The outputs

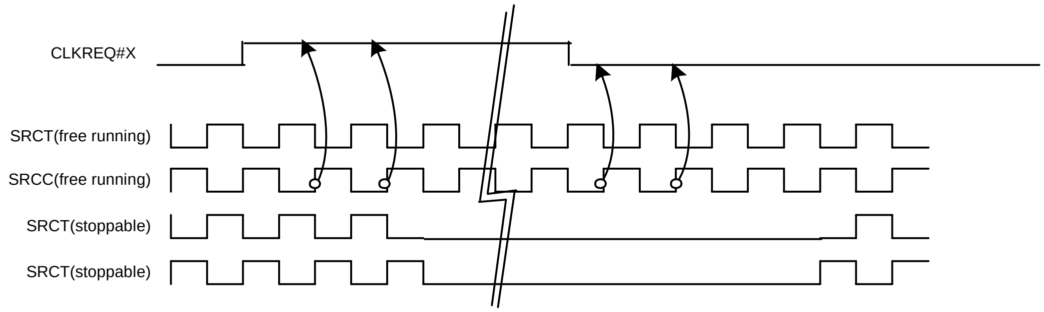


Figure 3. CLK_REQ#[1:9] Deassertion/Assertion Waveform

controlled by CLKREQ# are determined by the settings in register byte 8. The CLKREQ# signal is a de-bounced signal in that it's state must remain unchanged during two consecutive rising edges of SRCC to be recognized as a valid assertion or deassertion. (The assertion and deassertion of this signal is absolutely asynchronous.)

CLK_REQ[1:9]# Assertion (CLKREQ# -> LOW)

All differential outputs that were stopped are to resume normal operation in a glitch-free manner. The maximum latency from the assertion to active outputs is between 2 and 6 SRC clock periods (2 clocks are shown) with all SRC outputs resuming simultaneously. All stopped SRC outputs must be driven HIGH within 10 ns of CLKREQ# deassertion to a voltage greater than 200 mV.

CLK_REQ[1:9]# Deassertion (CLKREQ# -> HIGH)

The impact of deasserting the CLKREQ# pins is that all SRC outputs that are set in the control registers to stoppable via deassertion of CLKREQ# are to be stopped after their next transition. The final state of all stopped SRC clocks is Low/Low.

PD (Power-down) Clarification

The VTT_PWRGD#/PD pin is a dual-function pin. During initial power-up, the pin functions as VTT_PWRGD#. Once VTT_PWRGD# has been sampled LOW by the clock chip, the pin assumes PD functionality. The PD pin is an asynchronous active HIGH input used to shut off all clocks cleanly prior to shutting off power to the device. This signal is synchronized internal to the device prior to powering down the clock synthesizer. PD is also an asynchronous input for powering up the system. When PD is asserted HIGH, all clocks need to be driven to a LOW value and held prior to turning off the VCOs and the crystal oscillator.

PD (Power-down) Assertion

When PD is sampled HIGH by two consecutive rising edges of CPUC, all single-ended outputs will be held LOW on their next HIGH-to-LOW transition and differential clocks must be held HIGH or tri-stated (depending on the state of the control register drive mode bit) on the next diff clock# HIGH-to-LOW transition within 4 clock periods. When the SMBus PD drive mode bit corresponding to the differential (CPU, SRC, and DOT) clock output of interest is programmed to '0', the clock outputs are held with "Diff clock" pin driven HIGH, and "Diff clock#" tri-state. If the control register PD drive mode bit corresponding to the output of interest is programmed to "1", then both the "Diff clock" and the "Diff clock#" are tri-state. Note that *Figure 4* shows CPUT = 133 MHz and PD drive mode = '1' for all differential outputs. This diagram and description is applicable to valid CPU frequencies 100, 133, 166, and 200 MHz. In the event that PD mode is desired as the initial power-on state, PD must be asserted HIGH in less than 10 µs after asserting Vtt_PwrGd#. It should be noted that 96_100_SSC will follow the DOT waveform when selected for 96 MHz and the SRC waveform when in 100-MHz mode.

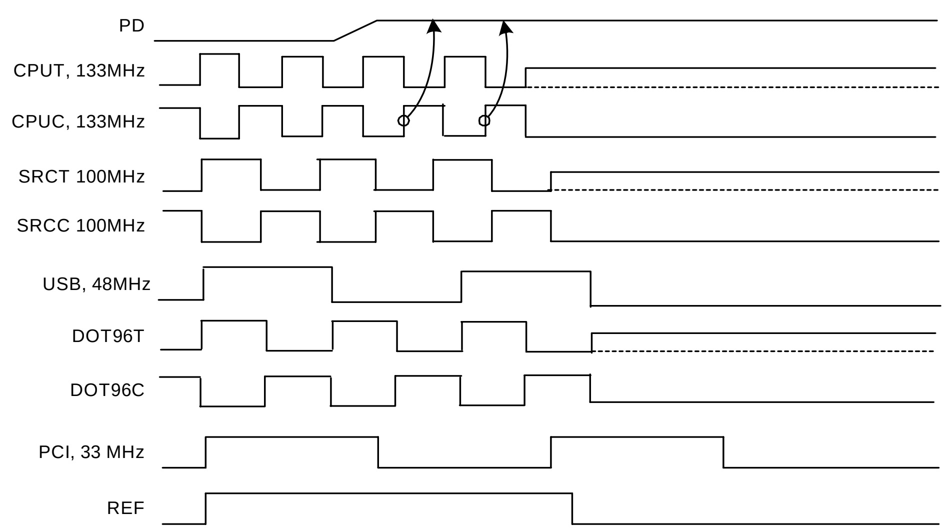


Figure 4. Power-down Assertion Timing Waveform

PD Deassertion

The power-up latency is less than 1.8 ms. This is the time from the deassertion of the PD pin or the ramping of the power supply until the time that stable clocks are output from the clock chip. All differential outputs stopped in a three-state condition resulting from power down will be driven high in less than 300 µs of PD deassertion to a voltage greater than 200 mV. After the clock chip's internal PLL is powered up and locked, all outputs will be enabled within a few clock cycles of each other. *Figure 5* is an example showing the relationship of clocks coming up. It should be noted that 96_100_SSC will follow the DOT waveform when selected for 96 MHz and the SRC waveform when in 100-MHz mode.

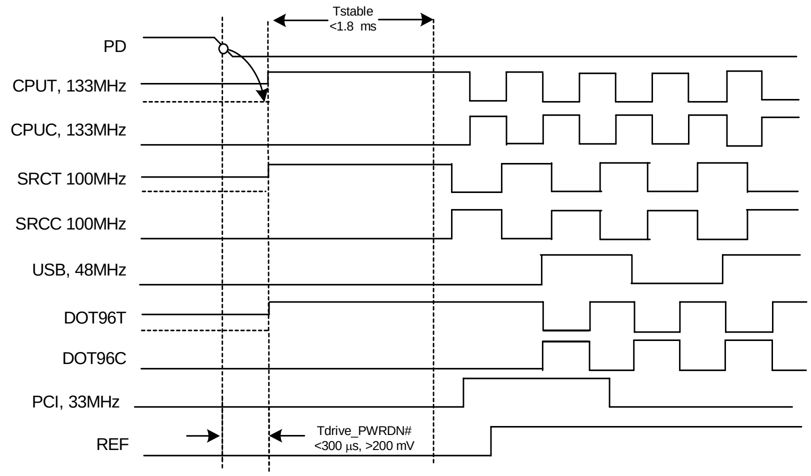


Figure 5. Power-down Deassertion Timing Waveform

CPU_STP# Assertion

The CPU_STP# signal is an active LOW input used for synchronous stopping and starting the CPU output clocks while the rest of the clock generator continues to function. When the CPU_STP# pin is asserted, all CPU outputs that are set with the SMBus configuration to be stoppable via assertion of CPU_STP# will be stopped within two–six CPU clock periods after being sampled by two rising edges of the internal CPUC clock. The final state of all stopped CPU clocks is High/Low when driven, Low/Low when tri-stated.

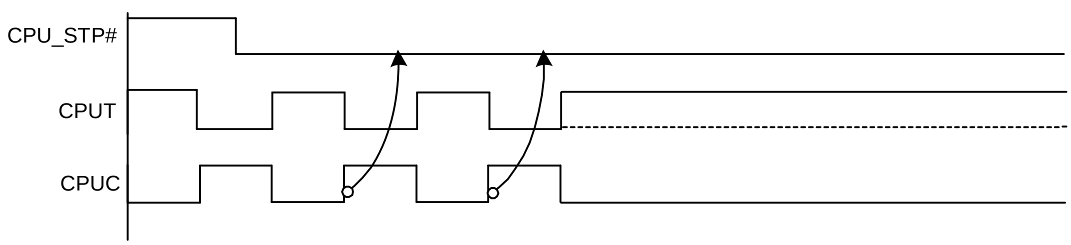


Figure 6. CPU_STP# Assertion Waveform

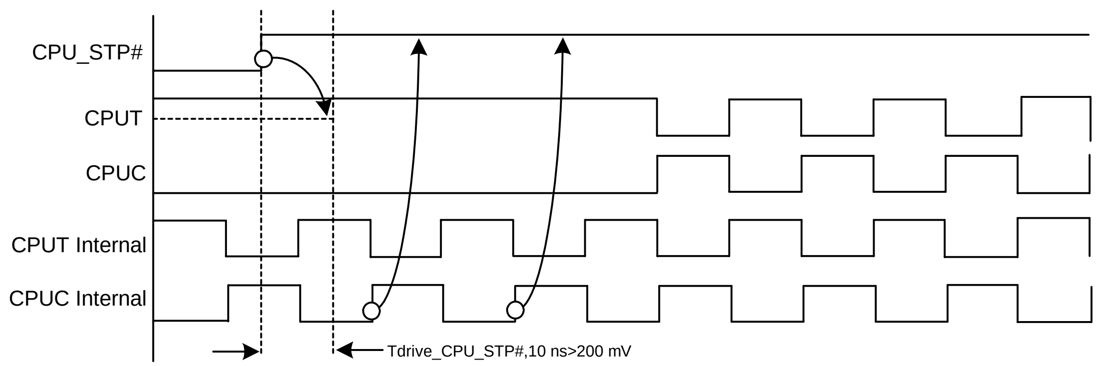


Figure 7. CPU_STP# Deassertion Waveform

PCI_STP# Assertion

The PCI_STP# signal is an active LOW input used for synchronous stopping and starting the PCI outputs and SRC outputs if they are set to be stoppable in SMbus while the rest of the clock generator continues to function. The set-up time for capturing PCI_STP# going LOW is 10 ns (t_{SU}). (See *Figure 9*.) The PCIF clocks will not be affected by this pin if their corresponding control bit in the SMBus register is set to allow them to be free running. All stopped PCI outputs are driven Low, SRC outputs are High/Low if set to driven and Low/Low if set to tri-state.

PCI_STP# Deassertion

The deassertion of the PCI_STP# signal will cause all PCI and stoppable PCIF clocks to resume running in a synchronous manner within two PCI clock periods after PCI_STP# transitions to a HIGH level

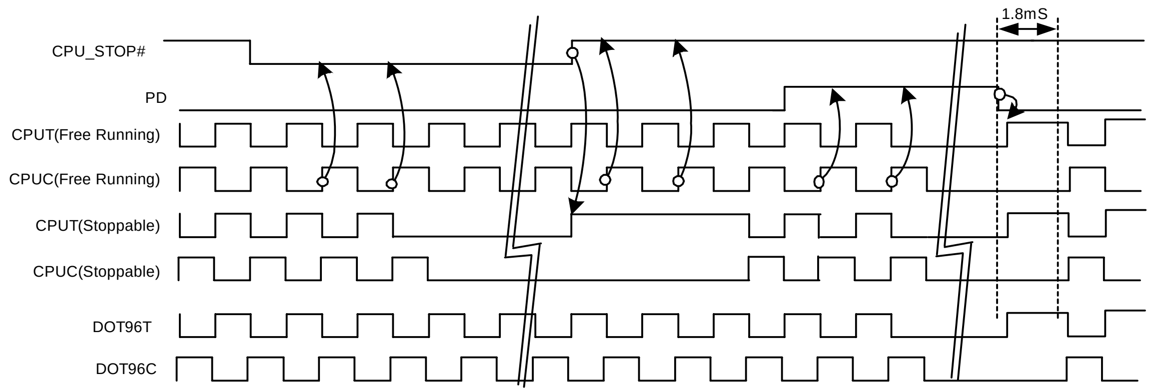


Figure 8. CPU_STP# = Tri-state, CPU_PD = Tri-state, DOT_PD = Tri-state

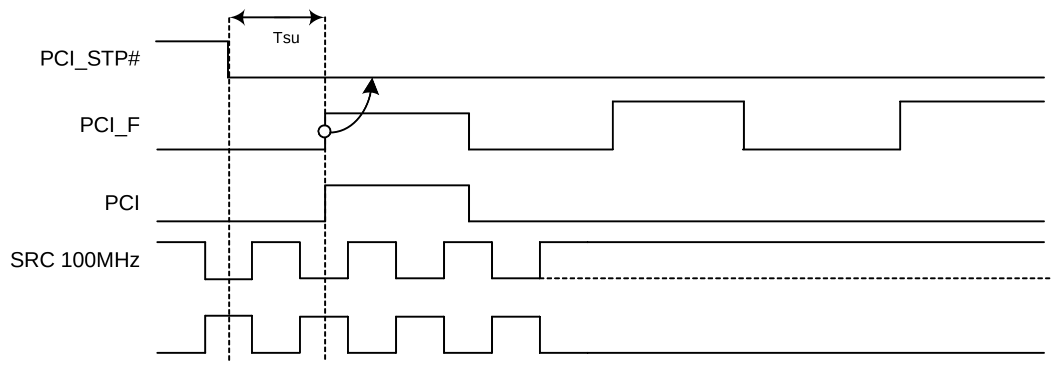


Figure 9. PCI_STP# Assertion Waveform

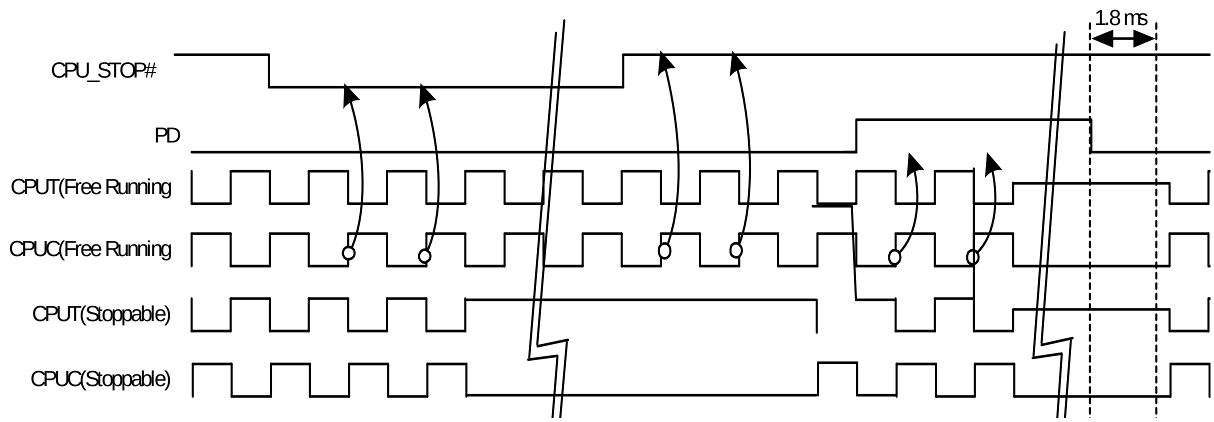


Figure 10. CPU_STP# = Driven, CPU_PD = Driven, DOT_PD = Driven

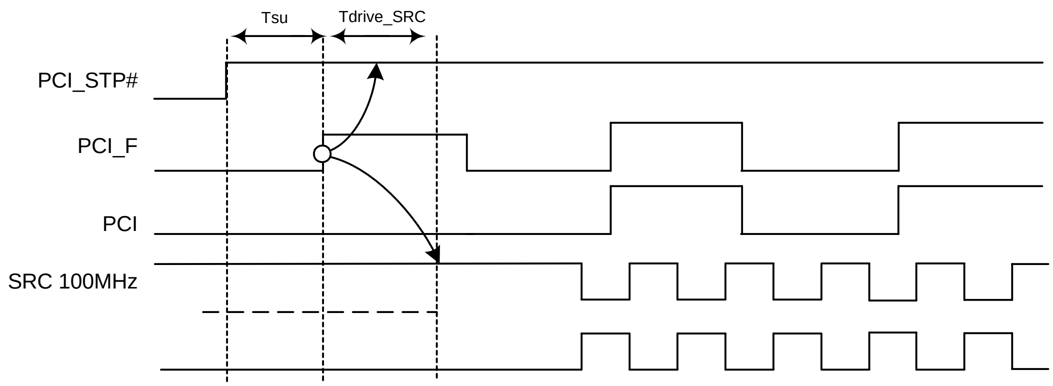


Figure 11. PCI_STP# Deassertion Waveform

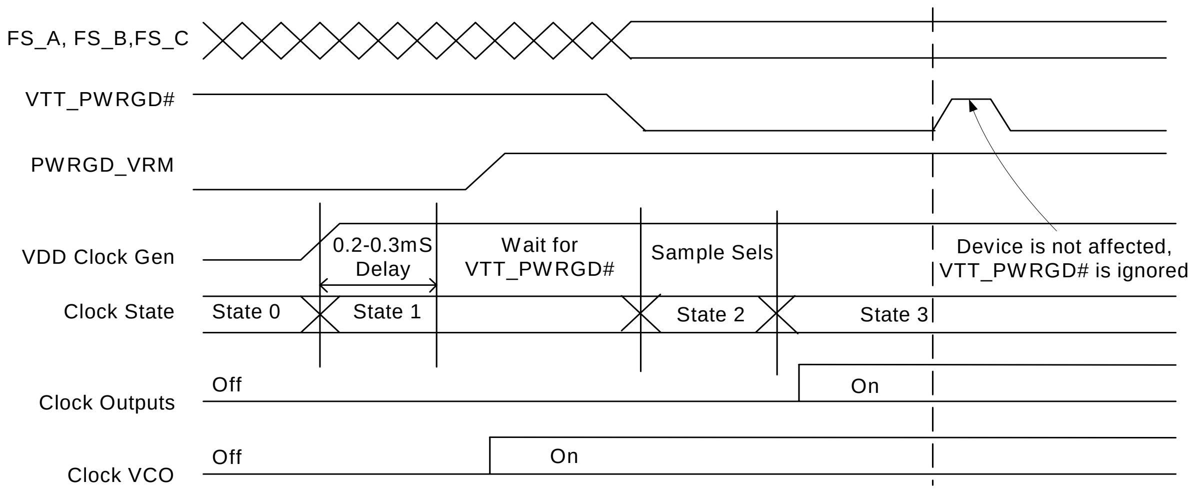


Figure 12. VTTPWRGD# Timing DIagram

Absolute Maximum Conditions

Parameter	Description	Condition	Min.	Max.	Unit
V_{DD}	Core Supply Voltage		–0.5	4.6	V
V_{DD_A}	Analog Supply Voltage		–0.5	4.6	V
V_{IN}	Input Voltage	Relative to V_{SS}	–0.5	V_{DD} + 0.5	VDC
T_S	Temperature, Storage	Non-functional	–65	150	°C
T_A	Temperature, Operating Ambient	Functional	0	85	°C
T_J	Temperature, Junction	Functional	–	150	°C
$Ø_{JC}$	Dissipation, Junction to Case	Mil-STD-883E Method 1012.1	–	20	°C/W
$Ø_{JA}$	Dissipation, Junction to Ambient	JEDEC (JESD 51)	–	60	°C/W
ESD_{HBM}	ESD Protection (Human Body Model)	MIL-STD-883, Method 3015	2000	–	V
UL-94	Flammability Rating	At 1/8 in.	V–0		
MSL	Moisture Sensitivity Level		1		

Multiple Supplies: The Voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

DC Electrical Specifications

Parameter	Description	Condition	Min.	Max.	Unit
All VDDs	3.3V Operating Voltage	3.3 ± 5%	3.135	3.465	V
V_{ILI2C}	Input Low Voltage	SDATA, SCLK	–	1.0	V
V_{IHI2C}	Input High Voltage	SDATA, SCLK	2.2	–	V
V_{IL_FS}	FS_[A,B] Input Low Voltage		V_{SS} – 0.3	0.35	V
V_{IH_FS}	FS_[A,B] Input High Voltage		0.7	V_{DD} + 0.5	V
V_{ILFS_C}	FS_C Input Low Voltage		V_{SS} – 0.3	0.35	V
V_{IMFS_C}	FS_C Input Middle Voltage		0.7	1.7	V
V_{IHFS_C}	FS_C Input High Voltage		2.0	V_{DD} + 0.5	V
V_{IL}	3.3V Input Low Voltage		V_{SS} – 0.3	0.8	V
V_{IH}	3.3V Input High Voltage		2.0	V_{DD} + 0.3	V
I_{IL}	Input Low Leakage Current	Except internal pull-up resistors, 0 < V_{IN} < V_{DD}	–5	5	μA
I_{IH}	Input High Leakage Current	Except internal pull-down resistors, 0 < V_{IN} < V_{DD}	–	5	μA
V_{OL}	3.3V Output Low Voltage	I_{OL} = 1 mA	–	0.4	V
V_{OH}	3.3V Output High Voltage	I_{OH} = –1 mA	2.4	–	V
I_{OZ}	High-impedance Output Current		–10	10	μA
C_{IN}	Input Pin Capacitance		3	5	pF
C_{OUT}	Output Pin Capacitance		3	6	pF
L_{IN}	Pin Inductance		–	7	nH
V_{XIH}	Xin High Voltage		$0.7V_{DD}$	V_{DD}	V
V_{XIL}	Xin Low Voltage		0	$0.3V_{DD}$	V
$I_{DD3.3V}$	Dynamic Supply Current	In low drive mode per *Figure 13* and *Figure 15* @133 MHz	–	250	mA
$I_{PD3.3V}$	Power-down Supply Current	PD asserted, Outputs Driven	–	30	mA
$I_{PD3.3V}$	Power-down Supply Current	PD asserted, Outputs Tri-state	–	5	mA

AC Electrical Specifications

Parameter	Description	Condition	Min.	Max.	Unit
Crystal					
T_{DC}	XIN Duty Cycle	The device will operate reliably with input duty cycles up to 30/70 but the REF clock duty cycle will not be within specification	47.5	52.5	%
T_{PERIOD}	XIN Period	When XIN is driven from an external clock source	69.841	71.0	ns
T_R/T_F	XIN Rise and Fall Times	Measured between $0.3V_{DD}$ and $0.7V_{DD}$	–	10.0	ns
T_{CCJ}	XIN Cycle to Cycle Jitter	As an average over 1-μs duration	–	500	ps
L_{ACC}	Long-term Accuracy	Measured at crossing point V_{OX}	–	300	ppm
CPU at 0.8V					
T_{DC}	CPUT and CPUC Duty Cycle	Measured at crossing point V_{OX}	45	55	%
T_{PERIOD}	100-MHz CPUT and CPUC Period	Measured at crossing point V_{OX}	9.997001	10.00300	ns
T_{PERIOD}	133-MHz CPUT and CPUC Period	Measured at crossing point V_{OX}	7.497751	7.502251	ns
T_{PERIOD}	166-MHz CPUT and CPUC Period	Measured at crossing point V_{OX}	5.998201	6.001801	ns
T_{PERIOD}	200-MHz CPUT and CPUC Period	Measured at crossing point V_{OX}	4.998500	5.001500	ns
$T_{PERIODSS}$	100-MHz CPUT and CPUC Period, SSC	Measured at crossing point V_{OX}	9.997001	10.05327	ns
$T_{PERIODSS}$	133-MHz CPUT and CPUC Period, SSC	Measured at crossing point V_{OX}	7.497751	7.539950	ns
$T_{PERIODSS}$	166-MHz CPUT and CPUC Period, SSC	Measured at crossing point V_{OX}	5.998201	6.031960	ns
$T_{PERIODSS}$	200-MHz CPUT and CPUC Period, SSC	Measured at crossing point V_{OX}	4.998500	5.026634	ns
$T_{PERIODAbs}$	100-MHz CPUT and CPUC Absolute period	Measured at crossing point V_{OX}	9.912001	10.08800	ns
$T_{PERIODAbs}$	133-MHz CPUT and CPUC Absolute period	Measured at crossing point V_{OX}	7.412751	7.587251	ns
$T_{PERIODAbs}$	166-MHz CPUT and CPUC Absolute period	Measured at crossing point V_{OX}	5.913201	6.086801	ns
$T_{PERIODAbs}$	200-MHz CPUT and CPUC Absolute period	Measured at crossing point V_{OX}	4.913500	5.086500	ns
$T_{PERIODSSAbs}$	100-MHz CPUT and CPUC Absolute period, SSC	Measured at crossing point V_{OX}	9.912001	10.13827	ns
$T_{PERIODSSAbs}$	133-MHz CPUT and CPUC Absolute period, SSC	Measured at crossing point V_{OX}	7.412751	7.624950	ns
$T_{PERIODSSAbs}$	166-MHz CPUT and CPUC Absolute period, SSC	Measured at crossing point V_{OX}	5.913201	6.116960	ns
$T_{PERIODSSAbs}$	200-MHz CPUT and CPUC Absolute period, SSC	Measured at crossing point V_{OX}	4.913500	5.111634	ns
T_{CCJ}	CPUT/C Cycle to Cycle Jitter	Measured at crossing point V_{OX}	–	85[1]	ps
T_{CCJ2}	CPU2_ITP Cycle to Cycle Jitter	Measured at crossing point V_{OX}	–	125[1]	ps
L_{ACC}	Long-term Accuracy	Measured at crossing point V_{OX}	–	300	ppm
T_{SKEW}	CPU1 to CPU0 Clock Skew	Measured at crossing point V_{OX}	–	100	ps
T_{SKEW2}	CPU2_ITP to CPU0 Clock Skew	Measured at crossing point V_{OX}	–	150	ps
T_R/T_F	CPUT and CPUC Rise and Fall Time	Measured from V_{OL} = 0.175 to V_{OH} = 0.525V	175	700	ps
T_{RFM}	Rise/Fall Matching	Determined as a fraction of $2*(T_R – T_F)/(T_R + T_F)$	–	20	%

AC Electrical Specifications (continued)

Parameter	Description	Condition	Min.	Max.	Unit
ΔT_R	Rise Time Variation		–	125	ps
ΔT_F	Fall Time Variation		–	125	ps

Note:
1. Measured with one REF on.

Parameter	Description	Condition	Min.	Max.	Unit
V_{HIGH}	Voltage High	Math averages *Figure 15*	660	850	mV
V_{LOW}	Voltage Low	Math averages *Figure 15*	–150	–	mV
V_{OX}	Crossing Point Voltage at 0.7V Swing		250	550	mV
V_{OVS}	Maximum Overshoot Voltage		–	V_{HIGH} + 0.3	V
V_{UDS}	Minimum Undershoot Voltage		–0.3	–	V
V_{RB}	Ring Back Voltage	See *Figure 15*. Measure SE	–	0.2	V
SRC at 0.8V					
T_{DC}	SRCT and SRCC Duty Cycle	Measured at crossing point V_{OX}	45	55	%
T_{PERIOD}	100-MHz SRCT and SRCC Period	Measured at crossing point V_{OX}	9.997001	10.00300	ns
$T_{PERIODSS}$	100-MHz SRCT and SRCC Period, SSC	Measured at crossing point V_{OX}	9.997001	10.05327	ns
$T_{PERIODAbs}$	100-MHz SRCT and SRCC Absolute Period	Measured at crossing point V_{OX}	9.872001	10.12800	ns
$T_{PERI-ODSSAbs}$	100-MHz SRCT and SRCC Absolute Period, SSC	Measured at crossing point V_{OX}	9.872001	10.17827	ns
T_{SKEW}	Any SRCT/C to SRCT/C Clock Skew	Measured at crossing point V_{OX}	–	250	ps
T_{CCJ}	SRCT/C Cycle to Cycle Jitter	Measured at crossing point V_{OX}	–	125[1]	ps
L_{ACC}	SRCT/C Long Term Accuracy	Measured at crossing point V_{OX}	–	300	ppm
T_R/T_F	SRCT and SRCC Rise and Fall Time	Measured from V_{OL} = 0.175 to V_{OH} = 0.525V	175	800	ps
T_{RFM}	Rise/Fall Matching	Determined as a fraction of $2*(T_R – T_F)/(T_R + T_F)$	–	20	%
ΔT_R	Rise TimeVariation		–	125	ps
ΔT_F	Fall Time Variation		–	125	ps
Tdrive	SRC output enable after PCI_STP# de-assertion			15	ns
V_{HIGH}	Voltage High	Math averages *Figure 15*	660	850	mV
V_{LOW}	Voltage Low	Math averages *Figure 15*	–150	–	mV
V_{OX}	Crossing Point Voltage at 0.7V Swing		180	550	mV
V_{OVS}	Maximum Overshoot Voltage		–	V_{HIGH} + 0.3	V
V_{UDS}	Minimum Undershoot Voltage		–0.3	–	V
V_{RB}	Ring Back Voltage	See *Figure 15.* Measure SE	–	0.2	V
LCD 96_100M_SSC at 0.8V					
T_{DC}	SSCT and SSCC Duty Cycle	Measured at crossing point V_{OX}	45	55	%
T_{PERIOD}	100-MHz SSCT and SSCC Period	Measured at crossing point V_{OX}	9.997001	10.00300	ns
$T_{PERIODSS}$	100-MHz SSCT and SSCC Period, SSC	Measured at crossing point V_{OX}	9.997001	10.05327	ns
$T_{PERIODAbs}$	100-MHz SSCT and SSCC Absolute Period	Measured at crossing point V_{OX}	9.872001	10.12800	ns
$T_{PERI-ODSSAbs}$	100-MHz SRCT and SRCC Absolute Period, SSC	Measured at crossing point V_{OX}	9.872001	10.17827	ns
T_{PERIOD}	96-MHz SSCT and SSCC Period	Measured at crossing point V_{OX}	10.41354	10.41979	ns

AC Electrical Specifications (continued)

Parameter	Description	Condition	Min.	Max.	Unit
$T_{PERIODSS}$	96-MHz SSCT and SSCC Period, SSC	Measured at crossing point V_{OX}	10.41354	10.47215	ns
$T_{PERIODAbs}$	96-MHz SSCT and SSCC Absolute Period	Measured at crossing point V_{OX}	10.16354	10.66979	ns
$T_{PERIODSSAbs}$	96-MHz SRCT and SRCC Absolute Period, SSC	Measured at crossing point V_{OX}	10.16354	10.72266	ns
T_{CCJ}	SSCT/C Cycle to Cycle Jitter	Measured at crossing point V_{OX}	–	125	ps
L_{ACC}	SSCT/C Long Term Accuracy	Measured at crossing point V_{OX}	–	300	ppm
T_R/T_F	SSCT and SSCC Rise and Fall Time	Measured from V_{OL} = 0.175 to V_{OH} = 0.525V	175	700	ps
T_{RFM}	Rise/Fall Matching	Determined as a fraction of $2*(T_R – T_F)/(T_R + T_F)$	–	20	%
ΔT_R	Rise TimeVariation		–	125	ps
ΔT_F	Fall Time Variation		–	125	ps
V_{HIGH}	Voltage High	Math averages *Figure 15*	660	850	mV
V_{LOW}	Voltage Low	Math averages *Figure 15*	–150	–	mV
V_{OX}	Crossing Point Voltage at 0.7V Swing		250	550	mV
V_{OVS}	Maximum Overshoot Voltage		–	V_{HIGH} + 0.3	V
V_{UDS}	Minimum Undershoot Voltage		–0.3	–	V
V_{RB}	Ring Back Voltage	See *Figure 15.* Measure SE	–	0.2	V
PCI/PCIF at 3.3V					
T_{DC}	PCI Duty Cycle	Measurement at 1.5V	45	55	%
T_{PERIOD}	Spread Disabled PCIF/PCI Period	Measurement at 1.5V	29.99100	30.00900	ns
$T_{PERIODSS}$	Spread Enabled PCIF/PCI Period, SSC	Measurement at 1.5V	29.9910	30.15980	ns
$T_{PERIODAbs}$	Spread Disabled PCIF/PCI Period	Measurement at 1.5V	29.49100	30.50900	ns
$T_{PERIODSSAbs}$	Spread Enabled PCIF/PCI Period, SSC	Measurement at 1.5V	29.49100	30.65980	ns
T_{HIGH}	PCIF and PCI high time	Measurement at 2.4V	12.0	–	ns
T_{LOW}	PCIF and PCI low time	Measurement at 0.4V	12.0	–	ns
T_R/T_F	PCIF/PCI rising and falling Edge Rate	Measured between 0.8V and 2.0V	1.0	4.0	V/ns
T_{SKEW}	Any PCI clock to Any PCI clock Skew	Measurement at 1.5V	–	1000	ps
T_{delay}	Intentional PCI-PCI delay	Measurement at 1.5V		200	pS
Tdrive	PCI output enable after PCI_STP# de-assertion			15	ns
T_{CCJ}	PCIF and PCI Cycle to Cycle Jitter	Measurement at 1.5V	–	500	ps
L_{ACC}	PCIF/PCI Long Term Accuracy	Measured at crossing point V_{OX}	–	300	ppm
DOT96 at 0.8V					
T_{DC}	DOT96T and DOT96C Duty Cycle	Measured at crossing point V_{OX}	45	55	%
T_{PERIOD}	DOT96T and DOT96C Period	Measured at crossing point V_{OX}	10.41354	10.41979	ns
$T_{PERIODAbs}$	DOT96T and DOT96C Absolute Period	Measured at crossing point V_{OX}	10.16354	10.66979	ns
T_{CCJ}	DOT96T/C Cycle to Cycle Jitter	Measured at crossing point V_{OX}	–	250	ps
L_{ACC}	DOT96T/C Long Term Accuracy	Measured at crossing point V_{OX}	–	300	ppm
T_R/T_F	DOT96T and DOT96C Rise and Fall Time	Measured from V_{OL} = 0.175 to V_{OH} = 0.525V	175	900	ps

AC Electrical Specifications (continued)

Parameter	Description	Condition	Min.	Max.	Unit
T_{RFM}	Rise/Fall Matching	Determined as a fraction of $2*(T_R – T_F)/(T_R + T_F)$	–	20	%
ΔT_R	Rise Time Variation		–	125	ps
ΔT_F	Fall Time Variation		–	125	ps
V_{HIGH}	Voltage High	Math averages *Figure 15*	660	850	mV
V_{LOW}	Voltage Low	Math averages *Figure 15*	–150	–	mV
V_{OX}	Crossing Point Voltage at 0.7V Swing		250	550	mV
V_{OVS}	Maximum Overshoot Voltage		–	V_{HIGH} + 0.3	V
V_{UDS}	Minimum Undershoot Voltage		–0.3	–	V
V_{RB}	Ring Back Voltage	See *Figure 15.* Measure SE	–	0.2	V
48_M at 3.3V					
T_{DC}	Duty Cycle	Measurement at 1.5V	45	55	%
T_{PERIOD}	Period	Measurement at 1.5V	20.83125	20.83542	ns
$T_{PERIODAbs}$	Absolute Period	Measurement at 1.5V	20.48125	21.18542	ns
T_{HIGH}	48_M High time	Measurement at 2.4V	8.094	11.100	ns
T_{LOW}	48_M Low time	Measurement at 0.4V	7.694	11.100	ns
T_R/T_F	Rising and Falling Edge Rate	Measured between 0.8V and 2.0V	1.0	2.0	V/ns
T_{CCJ}	Cycle to Cycle Jitter	Measurement at 1.5V	–	350	ps
L_{ACC}	48M Long Term Accuracy	Measured at crossing point V_{OX}	–	100	ppm
27_M at 3.3V					
T_{DC}	Duty Cycle	Measurement at 1.5V	45	55	%
T_{PERIOD}	Spread Disabled 27M Period	Measurement at 1.5V	27.000	27.0547	ns
	Spread Enabled 27M Period	Measurement at 1.5V	27.000	27.0547	
T_{HIGH}	27_M High time	Measurement at 2.0V	10.5	–	ns
T_{LOW}	27_M Low time	Measurement at 0.8V	10.5	–	ns
T_R/T_F	Rising and Falling Edge Rate	Measured between 0.8V and 2.0V	1.0	4.0	V/ns
T_{CCJ}	Cycle to Cycle Jitter	Measurement at 1.5V	–	500	ps
L_{ACC}	27_M Long Term Accuracy	Measured at crossing point V_{OX}	–	50	ppm
REF at 3.3V					
T_{DC}	REF Duty Cycle	Measurement at 1.5V	45	55	%
T_{PERIOD}	REF Period	Measurement at 1.5V	69.8203	69.8622	ns
$T_{PERIODAbs}$	REF Absolute Period	Measurement at 1.5V	68.82033	70.86224	ns
T_R/T_F	REF Rising and Falling Edge Rate	Measured between 0.8V and 2.0V	1.0	4.0	V/ns
T_{SKEW}	REF Clock to REF Clock	Measurement at 1.5V	–	500	ps
T_{CCJ}	REF Cycle to Cycle Jitter	Measurement at 1.5V	–	1000	ps
L_{ACC}	Long Term Accuracy	Measurement at 1.5V	–	300	ppm
ENABLE/DISABLE and SET-UP					
T_{STABLE}	Clock Stabilization from Power-up		–	1.8	ms
T_{SS}	Stopclock Set-up Time		10.0	–	ns
T_{SH}	Stopclock Hold Time		0	–	ns

Test and Measurement Set-up

For Single-ended Signals and Reference

The following diagram shows test load configurations for the single-ended PCI, USB, and REF output signals.

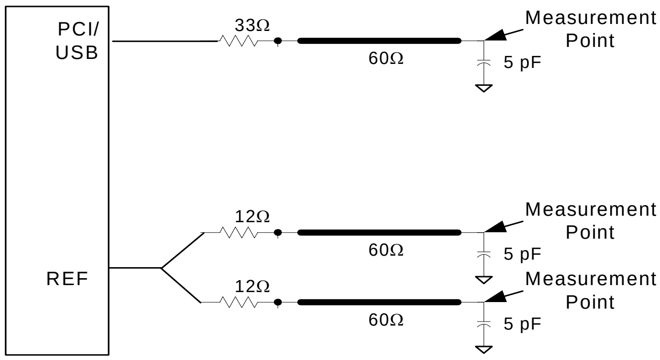


Figure 13.Single-ended Load Configuration Low Drive Option

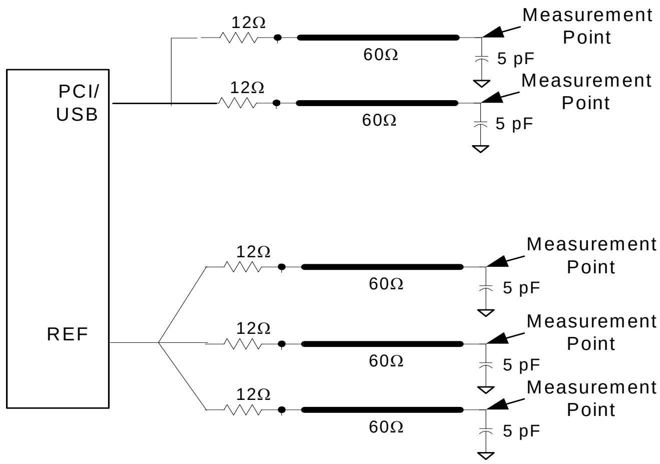


Figure 14. Single-ended Load Configuration High Drive Option

The following diagram shows the test load configuration for the differential CPU and SRC outputs.

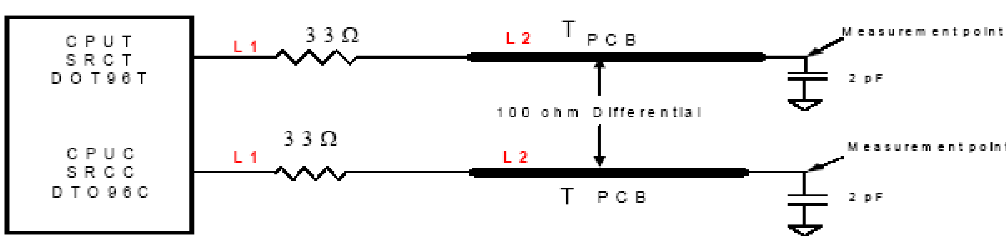


Figure 15. 0.8V Differential Load Configuration

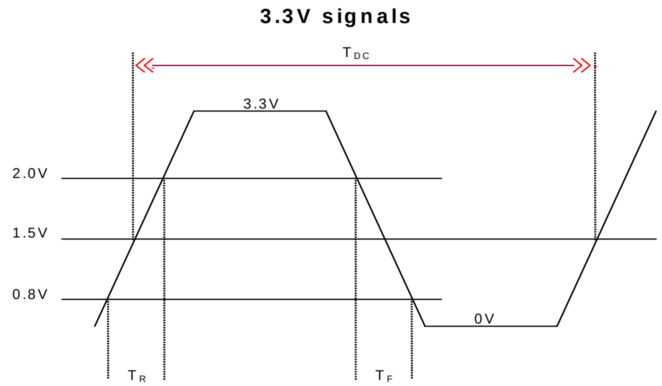


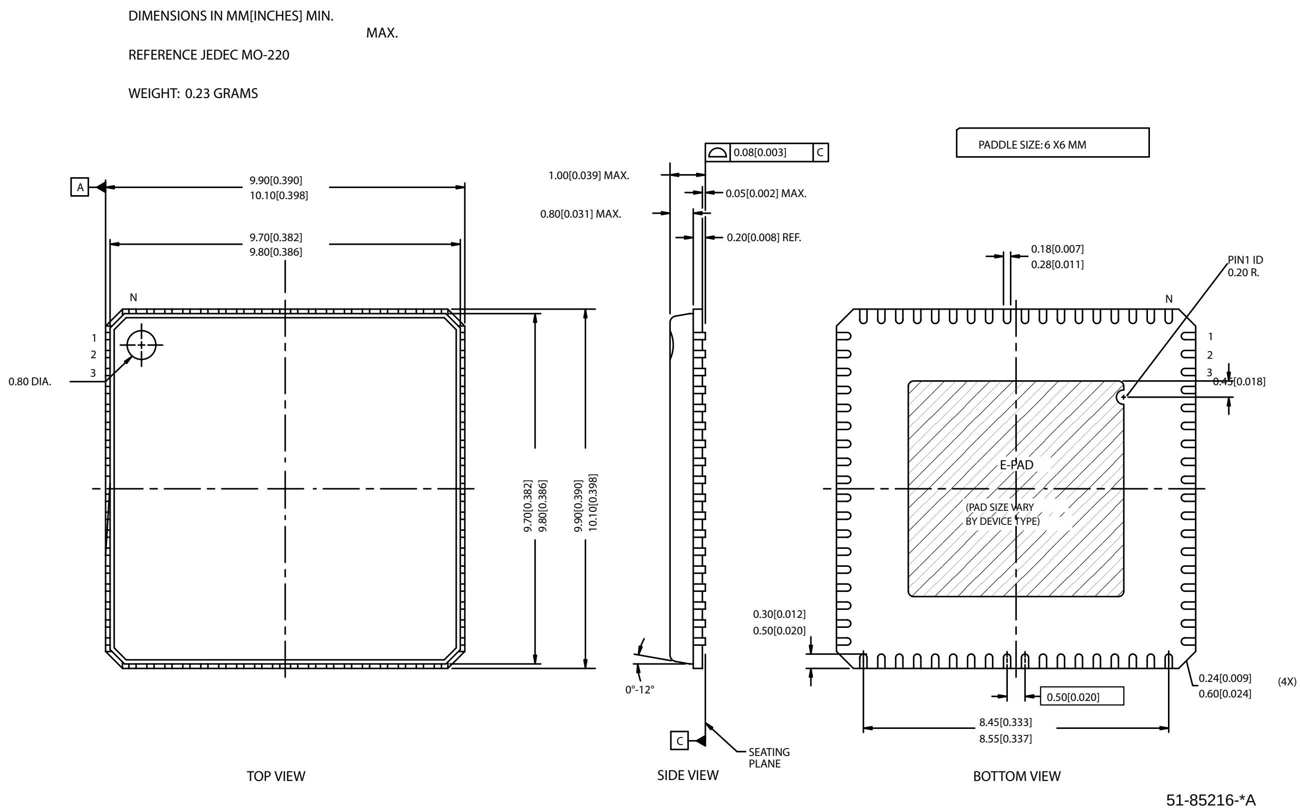
Figure 16. Single-ended Output Signals (for AC Parameters Measurement)

Ordering Information

Part Number	Package Type	Product Flow
Lead-free		
CY28549LFXC	72-pin QFN	Commercial, 0° to 85°C
CY28549LFXCT	72-pin QFN–Tape and Reel	Commercial, 0° to 85°C

Package Diagram

72-Lead QFN 10 x 10 mm (Punch Version) LF72A



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Document History Page

Document Title: CY28549 Clock Generator for Intel® CK410M Document Number: xxx-xxxxx				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**				New data sheet