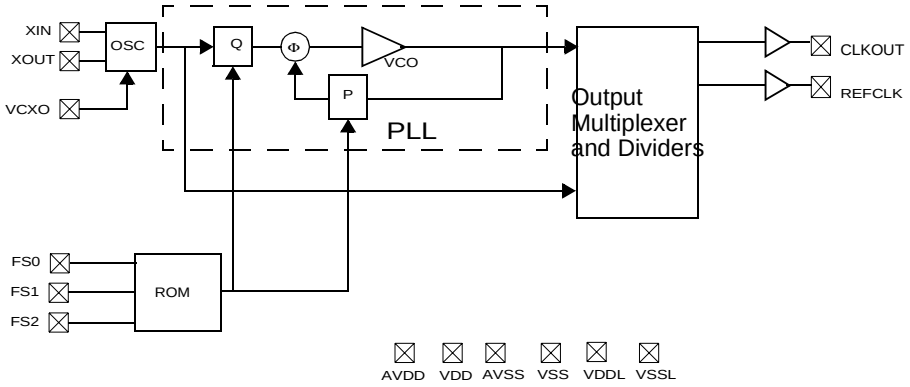
# MediaClock™
# Digital TV Clock Generator with VCXO

| Features | Benefits |
|---|---|
| • **Low jitter, high-accuracy outputs** | Meets critical timing requirements in complex system designs |
| • **VCXO with analog adjust** | Large ±150-ppm range, better linearity |
| • **3.3V operation** | Enables application compatibility |

## Frequency Table

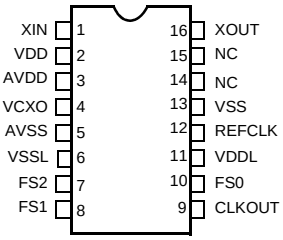
| Part Number | Outputs | Input Frequency Range | Output Frequency Range |
|---|---|---|---|
| CY24133-1 | 2 | 27-MHz pullable Crystal per Cypress Specification | 3.072-, 4.096-, 6.144-, 11.2896-, 12.288-MHz-selectable output frequencies and 27-MHz reference output |

## Logic Block Diagram




## Pin Configuration

**CY24133-1**
**16-pin TSSOP**



## Pin Description

| Name | Pin Number | Description |
|---|---|---|
| XIN | 1 | **Reference Crystal Input** |
| $V_{DD}$ | 2 | **Voltage Supply** |
| $A_{VDD}$ | 3 | **Analog Voltage Supply** |
| VCXO | 4 | **Input Analog Control Voltage for VCXO** |
| $AV_{SS}$ | 5 | **Analog Ground** |
| $V_{SSL}$ | 6 | **Output Clock Ground** |
| FS2 | 7 | **Frequency Select 2** |
| FS1 | 8 | **Frequency Select 1** |
| CLKOUT | 9 | **Configurable Clock Output 1 at VDDL level** |
| FS0 | 10 | **Frequency Select 0** |
| VDDL | 11 | **Clock Output Voltage Supply** |
| REFCLK | 12 | **Reference Clock Output at VDDL level** |
| VSS | 13 | **Ground** |
| NC | 14 | **No Connect** |
| NC | 15 | **No Connect** |
| XOUT[1] | 16 | **Reference Crystal Output** |

## Frequency Select Table—CY24133-1

| FS2 | FS1 | FSO | CLKOUT | REFCLK |
|---|---|---|---|---|
| 0 | 0 | 0 | 3.072 | 27 |
| 0 | 0 | 1 | 4.096 | 27 |
| 0 | 1 | 0 | 6.144 | 27 |
| 0 | 1 | 1 | 11.2896 | 27 |
| 1 | 0 | 0 | 12.288 | 27 |
| 1 | 0 | 1 | off | off |
| 1 | 1 | 0 | off | off |
| 1 | 1 | 1 | off | off |

## Pullable Crystal Specifications

| Parameter | Name | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $CR_{load}$ | Crystal Load Capacitance | | 14 | | pF |
| C0/C1 | | | | 250 | |
| ESR | Equivalent Series Resistance | | 35 | 50 | Ω |
| $T_o$ | Operating Temperature | 0 | | 70 | °C |
| Crystal Accuracy | Crystal Accuracy | | | ±20 | ppm |
| $TT_s$ | Stability over temperature and aging | | | ±50 | ppm |

## Absolute Maximum Conditions

| Parameter | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage | –0.5 | 7.0 | V |
| $V_{DDL}$ | I/O Supply Voltage | –0.5 | 7.0 | V |
| $T_S$ | Storage Temperature[2] | –65 | 125 | °C |
| $T_J$ | Junction Temperature | | 125 | °C |

**Notes:**
1. Float $X_{OUT}$ if $X_{IN}$ is externally driven.
2. Rated for 10 years.

## Absolute Maximum Conditions (continued)

| Parameter | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| | Digital Inputs | $AV_{SS}$ – 0.3 | $AV_{DD}$ + 0.3 | V |
| | Analog Input referred to $AV_{DD}$ | $AV_{SS}$ – 0.3 | $AV_{DD}$ + 0.3 | V |
| | Electrostatic Discharge | 2 | | kV |

## Recommended Operating Conditions

| Parameter | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $AV_{DD}/V_{DD}/V_{DDL}$ | Operating Voltage | 3.135 | 3.3 | 3.456 | V |
| $T_A$ | Ambient Temperature | 0 | | 70 | °C |
| $C_{LOAD}$ | Max. Load Capacitance $V_{DD}/V_{DDL}$=3.3V | | | 15 | pF |
| $f_{REF}$ | Reference Frequency | | 27 | | MHz |

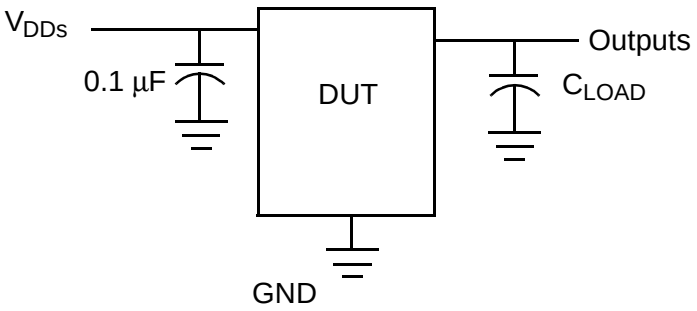
## DC Electrical Specifications

| Parameter[3] | Name | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{OH}$ | Output High Current | $V_{OH} = V_{DD} – 0.5$, $V_{DD}/V_{DDL}$ = 3.3V | 12 | 24 | | mA |
| $I_{OL}$ | Output Low Current | $V_{OL}$ = 0.5, $V_{DD}/V_{DDL}$ = 3.3V | 12 | 24 | | mA |
| $V_{IH}$ | Input High Voltage | CMOS levels | 0.7 | | | VDD |
| $V_{IL}$ | Input Low Voltage | CMOS levels | | | 0.3 | VDD |
| $C_{IN}$ | Input Capacitance | Frequency Select Pins | | | 7 | pF |
| $f_{\Delta XO}$ | VCXO pullability range | | ±150 | | | ppm |
| $V_{VCXO}$ | VCXO input range | | 0 | | $AV_{DD}$ | V |
| $I_{DD}$ | Supply Current | $AV_{DD}/V_{DD}/V_{DDL}$ Current | | 18 | 25 | mA |

## AC Electrical Specifications

| Parameter[3] | Name | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| DC | Output Duty Cycle | Duty Cycle is defined in *Figure 1*, 50% of $V_{DD}$ | 45 | 50 | 55 | % |
| ER | Rising Edge Rate | Output Clock Edge Rate, Measured from 20% to 80% of $V_{DD}$, $C_{LOAD}$ = 15 pF See *Figure 2*. | 0.8 | 1.4 | | V/ns |
| EF | Falling Edge Rate | Output Clock Edge Rate, Measured from 80% to 20% of $V_{DD}$, $C_{LOAD}$ = 15 pF See *Figure 2*. | 0.8 | 1.4 | | V/ns |
| $t_9$ | Clock Jitter | Peak-to-Peak period jitter on CLKOUT | | 350 | | ps |
| $t_{10}$ | PLL Lock Time | Measured from $V_{DD}$ = 3.0V | | | 3 | ms |

## Test and Measurement Set-up




**Note:**
3. Guaranteed by design, not 100% tested.

## Voltage and Timing Definitions

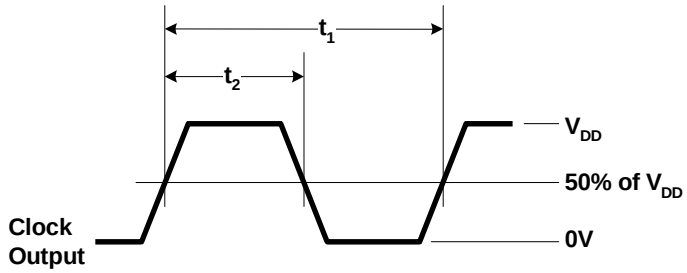



**Figure 1. Duty Cycle Definition**

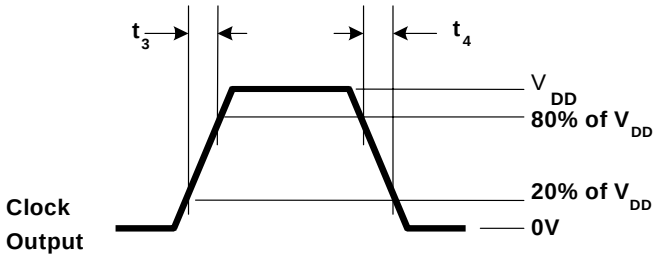


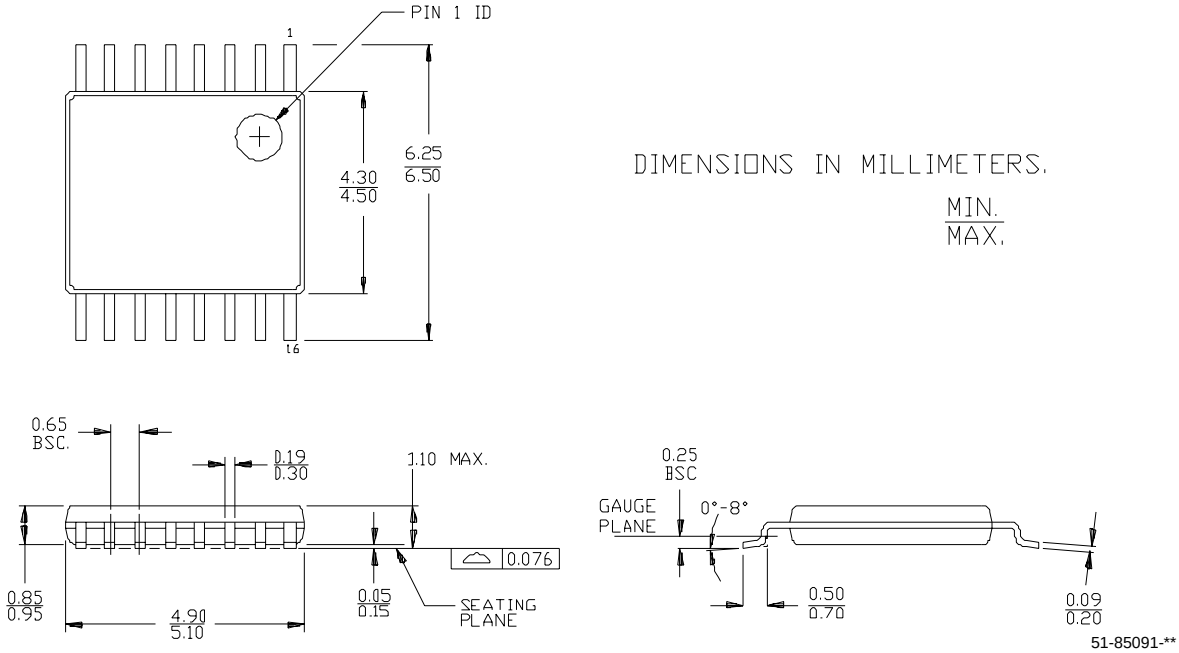

**Figure 2. ER = (0.6 x $V_{DD}$) /t3, EF = (0.6 x $V_{DD}$) /t4**

## Ordering Information

| Ordering Code | Package Name | Package Type | Operating Range | Operating Voltage |
|---|---|---|---|---|
| CY24133ZC-1 | Z16 | 16-pin TSSOP | Commercial | 3.3V |
| CY24133ZC-1T | Z16 | 16-pin TSSOP – Tape and Reel | Commercial | 3.3V |

## Package Drawing and Dimensions

**16-lead Thin Shrunk Small Outline Package (4.40 MM Body) Z16**



## Document History Page

| Document Title: CY24133 MediaClock™ Digital TV Clock Generator with VCXO<br>Document Number: 38-07497 | | | | |
|---|---|---|---|---|
| **REV.** | **ECN NO.** | **Issue Date** | **Orig. of Change** | **Description of Change** |
| ** | 121554 | 02/17/03 | CKN | New Data Sheet |