

March 1999 Revised May 2003

NC7WZ07

TinyLogic® UHS Dual Buffer (Open Drain Outputs)

General Description

The NC7WZ07 is a dual buffer with open drain outputs from Fairchild's Ultra High Speed Series of TinyLogic® in the space saving SC70 6-lead package. The device is fabricated with advanced CMOS technology to achieve ultra high speed with high output drive while maintaining low static power dissipation over a very broad $\rm V_{CC}$ operating range. The device is specified to operate over the 1.65V to 5.5V $\rm V_{CC}$ range. The inputs and outputs are high impedance when $\rm V_{CC}$ is 0V. Inputs tolerate voltages up to 7V independent of $\rm V_{CC}$ operating voltage.

Features

- Space saving SC70 6-lead package
- Ultra small MicroPak™ leadless package
- Ultra High Speed: t_{PZL} 2.3 ns Typ into 50 pF at 5V V_{CC}
- High I_{OL} Output Drive: +24 mA at 3V V_{CC}
- Broad V_{CC} Operating Range: 1.65V to 5.5V
- \blacksquare Matches the performance of LCX when operated at 3.3V V_{CC}
- Power down high impedance inputs/outputs
- Overvoltage tolerant inputs facilitate 5V to 3V translation
- Patented noise/EMI reduction circuitry implemented

Ordering Code:

Order Number	Package Number	Product Code Top Mark	Package Description	Supplied As		
NC7WZ07P6X	MAA06A	Z07	6-Lead SC70, EIAJ SC88, 1.25mm Wide	3k Units on Tape and Reel		
NC7WZ07L6X	MAC06A	D3	6-Lead MicroPak, 1.0mm Wide	5k Units on Tape and Reel		

Logic Symbol

IEEE/IEC



Pin Descriptions

Pin Names	Description
A ₁ , A ₂	Data Inputs
Y_1, Y_2	Output

Function Table

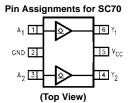
$$\mathbf{Y} = \mathbf{A}$$

Input	Output
Α	Υ
L	L
Н	Z

H = HIGH Logic Level L = LOW Logic Level

 $\label{eq:total_cond} \mbox{TinyLogic} \mbox{\o s} \mbox{ is a registered trademark of Fairchild Semiconductor Corporation.} \\ \mbox{MicroPak}^{\mbox{\tiny M}} \mbox{ is a trademark of Fairchild Semiconductor Corporation.} \\$

Connection Diagrams



Pin One Orientation Diagram



AAA represents Product Code Top Mark - see ordering code

Note: Orientation of Top Mark determines Pin One location. Read the top product code mark left to right, Pin One is the lower left pin (see diagram).

Pad Assignments for MicroPak



(Top Thru View)

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DS500218

Absolute Maximum Ratings(Note 1)

DC Input Diode Current (I_{IK})

@ $V_{IN} < -0.5V$ -50 mA

DC Output Diode Current (I_{OK})

Storage Temperature (T_{STG}) $-65^{\circ}C$ to +150 $^{\circ}C$ Junction Temperature under Bias (T_{J}) 150 $^{\circ}C$

Junction Lead Temperature (T_L)

(Soldering, 10 seconds) 260°C

Power Dissipation (P $_{\rm D}$) @ +85°C 180 mW

Recommended Operating Conditions (Note 2)

 $\begin{array}{ll} \mbox{Supply Voltage Operating ($V_{\rm CC}$)} & 1.65\mbox{V to } 5.5\mbox{V} \\ \mbox{Supply Voltage Data Retention ($V_{\rm CC}$)} & 1.5\mbox{V to } 5.5\mbox{V} \\ \mbox{Input Voltage ($V_{\rm IN}$)} & 0\mbox{V to } 5.5\mbox{V} \\ \end{array}$

Output Voltage (V_{OUT}) 0V to 5.5V Operating Temperature (T_A) $-40^{\circ}C$ to $+85^{\circ}C$

Input Rise and Fall Time (t_r, t_f)

$$\begin{split} &V_{CC} = 1.8 \text{V, } 2.5 \text{V} \pm 0.2 \text{V} & 0 \text{ ns/V to } 20 \text{ ns/V} \\ &V_{CC} = 3.3 \text{V} \pm 0.3 \text{V} & 0 \text{ ns/V to } 10 \text{ ns/V} \\ &V_{CC} = 5.0 \text{V} \pm 0.5 \text{V} & 0 \text{ ns/V to } 5 \text{ ns/V} \end{split}$$

Thermal Resistance (θ_{JA}) 350° C/W

Note 1: Absolute maximum ratings are DC values beyond which the device may be damaged or have its useful life impaired. The datasheet specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside datasheet specifications.

Note 2: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

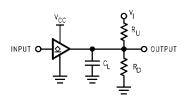
Symbol	Parameter	V _{CC}	$T_A = +25^{\circ}C$;	$T_A = -40^{\circ}C$ to $+85^{\circ}C$		Units	Con	Conditions	
Oyillboi	i arameter	(V)	Min	Тур	Max	Min	Max	Onits		ullions	
V _{IH}	HIGH Level Input Voltage	1.65 to 1.95	0.75 V _{CC}			0.75 V _{CC}		V			
		2.3 to 5.5	0.7 V _{CC}			0.7 V _{CC}		· ·			
V _{IL}	LOW Level Input Voltage	1.65 to 1.95			0.25 V _{CC}		0.25 V _{CC}	V			
		2.3 to 5.5			$0.3 V_{CC}$		$0.3\mathrm{V}_{\mathrm{CC}}$	· •			
I _{LKG}	HIGH Level Output	1.65 to 5.5			±5		±10	μА	$V_{IN} = V_{IH}$		
	Leakage Current	1.00 to 0.0							$V_{OUT} = V_{CC}$ or GND		
V _{OL}	LOW Level Output Voltage	1.65		0.0	0.1		0.0				
		1.8		0.0	0.1		0.1				
		2.3		0.0	0.1		0.1	V	$V_{IN} = V_{IL}$	$I_{OL} = 100 \ \mu A$	
		3.0		0.0	0.1		0.1				
		4.5		0.0	0.1		0.1				
		1.65		0.08	0.24		0.24			$I_{OL} = 4 \text{ mA}$	
		2.3		0.10	0.3		0.3			$I_{OL} = 8 \text{ mA}$	
		3.0		0.16	0.4		0.4	V		$I_{OL} = 16 \text{ mA}$	
		3.0		0.24	0.55		0.55			$I_{OL} = 24 \text{ mA}$	
		4.5		0.25	0.55		0.55			$I_{OL} = 32 \text{ mA}$	
I _{IN}	Input Leakage Current	0 to 5.5			±0.1		±1.0	μΑ	$0 \le V_{IN} \le 5$	5.5V	
I _{OFF}	Power Off Leakage Current	0.0			1		10	μΑ	V _{IN} or V _{OUT} = 5.5V		
I _{CC}	Quiescent Supply Current	1.65 to 5.5			1.0		10	μΑ	V _{IN} = 5.5V, GND		

AC Electrical Characteristics

Symbol	Parameter	V _{CC}		$T_A = +25^{\circ}C$		$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$		Units	Conditions	Figure
Symbol		(V)	Min	Тур	Max	Min	Max	Units	Conditions	Number
t _{PZL}	Propagation Delay	1.65	1.8	6.6	11.5	1.8	12.6			
		1.8	1.8	5.5	9.5	1.8	10.5		$C_L = 50 pF$	_
		2.5 ± 0.2	1.2	3.7	5.8	1.2	6.4	ns	$RU=500\Omega$	Figures 1, 3
		3.3 ± 0.3	0.8	2.9	4.4	0.8	4.8		$RD=500\Omega$., 0
		5.0 ± 0.5	0.5	2.3	3.5	0.5	3.9		$V_I = 2 \times V_{CC}$	
t _{PLZ}	Propagation Delay	1.65	1.8	5.5	11.5	1.8	12.6			
		1.8	1.8	4.3	9.5	1.8	10.5		$C_L = 50 \text{ pF}$	_
		2.5 ± 0.2	1.2	2.8	5.8	1.2	6.4	ns	$RU=500\Omega$	Figures 1, 3
		3.3 ± 0.3	0.8	2.1	4.4	0.8	4.8		$RD=500\Omega$., 0
		5.0 ± 0.5	0.5	1.4	3.5	0.5	3.9		$V_I = 2 \times V_{CC}$	
C _{IN}	Input Capacitance	0		2.5				pF		
C _{OUT}	Output Capacitance	0		4.0				pF		
C _{PD}	Power Dissipation	3.3		3				pF	(Note 3)	Figure 2
	Capacitance	5.0		4				PΕ	(Note 3)	Figure 2

Note 3: C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle. (See Figure 2.) C_{PD} is related to I_{CCD} dynamic operating current by the expression: $I_{CCD} = (C_{PD})(V_{CC})(f_{|N}) + (I_{CC}static).$

AC Loading and Waveforms



 C_L includes load and stray capacitance Input PRR = 1.0 MHz; t_W = 500 ns

FIGURE 1. AC Test Circuit



 $\begin{aligned} & \text{Input} = \text{AC Waveform; } t_{\text{r}} = t_{\text{f}} = 1.8 \text{ ns;} \\ & \text{PRR} = 10 \text{ MHz; } \text{Duty Cycle} = 50\% \end{aligned}$

FIGURE 2. $I_{\rm CCD}$ Test Circuit

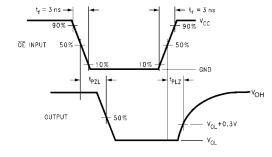


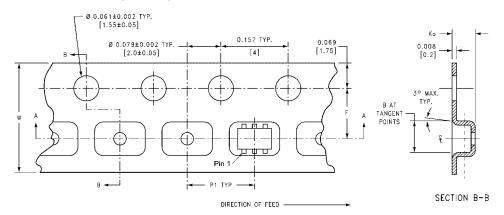
FIGURE 3. AC Waveforms

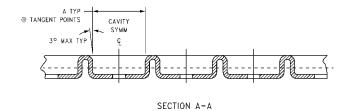
Tape and Reel Specification

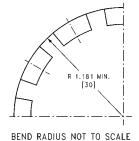
TAPE FORMAT for SC70

TAI ET ORMAT TO 3070										
Package	Tape	Number	Cavity	Cover Tape						
Designator	Section	Cavities	Status	Status						
	Leader (Start End)	125 (typ)	Empty	Sealed						
P6X	Carrier	3000	Filled	Sealed						
	Trailer (Hub End)	75 (typ)	Empty	Sealed						

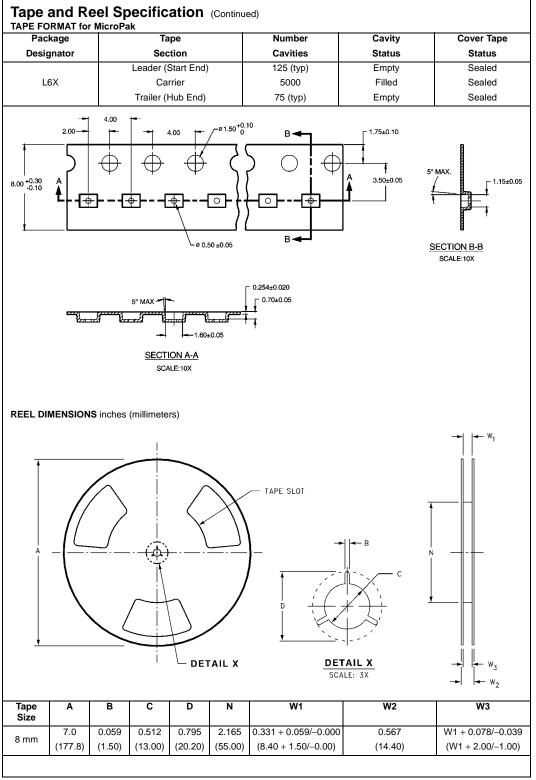
TAPE DIMENSIONS inches (millimeters)







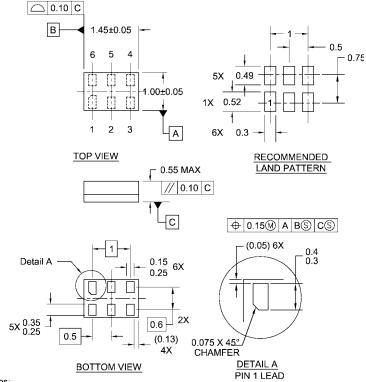
DIM F DIM A DIM B DIM P1 DIM W Tape Size DIM K_o Package 0.093 0.096 0.138 ± 0.004 0.053 ± 0.004 0.157 0.315 ± 0.004 SC70-6 8 mm (3.5 ± 0.10) (1.35 ± 0.10) (4) (8 ± 0.1) (2.35)(2.45)



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Physical Dimensions inches (millimeters) unless otherwise noted 0.65 B 1.25±0.10 2.10±0.10 0.20 +0.10 LAND PATTERN RECOMMENDATION ◆ max 0.1 **②** SEE DETAIL A 0.9±.10 0.95±0.15 max 0.1 R0.14 GAGE PLANE R0.10 0.20 0.45 0.10 -- 0.425 NOMINAL DETAIL A NOTES: A. CONFORMS TO EIAJ REGISTERED OUTLINE DRAWING SC88. MAA06ARevC B. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. C. DIMENSIONS ARE IN MILLIMETERS. 6-Lead SC70, EIAJ SC88, 1.25mm Wide Package Number MAA06A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



- Notes:
- 1. JEDEC PACKAGE REGISTRATION IS ANTICIPATED 2. DIMENSIONS ARE IN MILLIMETERS
- 3. DRAWING CONFORMS TO ASME Y14.5M-1994

MAC06ARevB

6-Lead MicroPak, 1.0mm Wide Package Number MAC06A

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