CY24C01/02/04/08/16

1 Kbit, 2 Kbit, 4 Kbit, 8 Kbit, and 16 Kbit (x8) Two Wire (I2C) Serial EEPROM

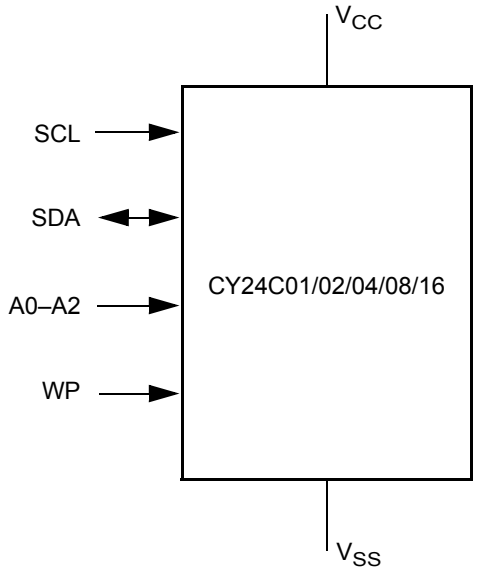
Features

- Continuous voltage operation
  - V_{CC} = 1.65V to 5.5V
- Internally organized as 128 x 8 (1K), 256 x 8 (2K), 512 x 8 (4K), 1024 x 8 (8K), or 2048 x 8 (16K)
- Industry standard two wire serial interface
- Schmitt trigger, filtered inputs for noise suppression
- Bidirectional data transfer protocol
- 1 MHz (2.5V - 5.5V), 400 KHz (1.65V - 5.5V), and 100 KHz (1.65V - 5.5V) compatibility
- Write protect pin for hardware data protection
- 16-byte page write mode
- Partial page writes enabled
- Self timed write cycle (5 ms max)
- High reliability
  - Endurance: 1 million write cycles
  - Data retention: 100 years
- Industrial temperature range
- 8-Pin SOIC and 8-Pin TSSOP packages
- Pb-free and RoHS compliant

Functional Description

The CY24C01/02/04/08/16 range of products provide 1K, 2K, 4K, 8K, and 16K bits of serial Electrically Erasable and Programmable Read Only Memory (EEPROM) organized as 128, 256, 512, 1024, and 2048 words of eight bits each. The device is optimized for use in many industrial applications where low power and low voltage operations are essential. The CY24C01/02/04/08/16 is available in space saving 8-Pin SOIC and 8-Pin TSSOP packages and is accessed through a two-wire serial interface. In addition, the entire family is available in 1.65V (1.65V to 5.5V) version.

Logic Block Diagram



Pinouts

Figure 1. Pin Diagram - 8-Pin SOIC/TSSOP Package

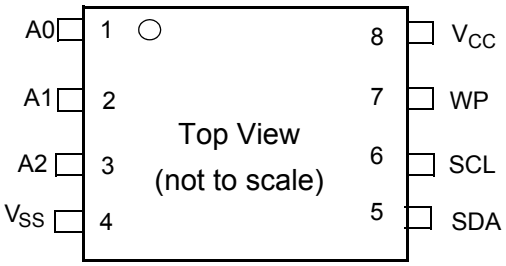


Table 1. Pin Definitions - 8-Pin SOIC/TSSOP Package

Pin Name	8-SOIC/TSSOP Pin Number	I/O Type	Description
A0–A2	1,2,3	Input	**Device Address Pins.** The CY24C01 and CY24C02 uses the A2, A1, and A0 inputs for hard wire addressing and a total of eight 1K and 2K devices may be addressed on a single bus system. The CY24C04 uses the A2 and A1 inputs for hard wire addressing and a total of four 4K devices may be addressed on a single bus system. The A0 pin is a no connect. The CY24C08 uses only the A2 input for hardwire addressing and a total of two 8K devices may be addressed on a single bus system. The A0 and A1 pins are no connects. The CY24C16 does not use the device address pins which limit the number of devices on a single bus to one. The A0, A1, and A2 pins are no connects.
V_{SS}	4	Ground	**Ground.** The ground for the device. It must be connected to the ground of the system.
SDA	5	Input/Output	**Serial Data.** The SDA pin is bidirectional for serial data transfer. This pin is open drain driven and is wired-ORed with any number of other open drain or open collector devices.
SCL	6	Input	**Serial Clock.** The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.
WP	7	Input	**Write Protect.** The CY24C01/02/04/08/16 has a write protect pin that provides hardware data protection. The write protect pin allows normal read and write operations when connected to ground (GND). When the write protect pin is connected to VCC, the write protection feature is enabled and operates as shown in Table 2 on page 3.
V_{CC}	8	Power Supply	**Power Supply.** The power supply inputs to the device.

Memory Organization

CY24C01

Internally organized with eight pages of 16 bytes each, the 1K requires a 7-bit data word address for random word addressing.

CY24C02

Internally organized with 16 pages of 16-bytes each, the 2K requires a 8-bit data word address for random word addressing.

CY24C04

Internally organized with 32 pages of 16 bytes each, the 4K requires a 9-bit data word address for random word addressing.

CY24C08

Internally organized with 64 pages of 16 bytes each, the 8K requires a 10-bit data word address for random word addressing.

CY24C16

Internally organized with 128 pages of 16 bytes each, the 16K requires an 11-bit data word address for random word addressing.

Device Operating Features

Clock and Data Transitions

The SDA pin is normally pulled high with an external device. Data on the SDA pin changes only during SCL low time periods. Data changes during SCL high periods indicate a start or stop condition as defined in the following section.

Start Condition

A high to low transition of SDA with SCL high is a start condition which must precede any other command (see Figure 2).

Stop Condition

A low to high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command places the EEPROM in a standby power mode (see Figure 2).

Acknowledge

All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM acknowledges each word received by sending a zero during the ninth clock cycle.

Standby Mode

The CY24C01/02/04/08/16 features a low power standby mode, which is enabled on power up, after the receipt of the STOP bit and the completion of any internal operations.

Device Internal Reset

To prevent inadvertent write operations during power up, a Power On Reset (POR) circuit is included. During power up (continuous rise of V_{CC}), the device does not respond to any instruction until the V_{CC} reaches the POR threshold voltage (this threshold is lower than the V_{CC} minimum operating voltage defined in DC Electrical Characteristics on page 8). When V_{CC} has passed over the POR threshold, the device is reset and is in standby power mode. During power down (continuous decay of V_{CC}), when V_{CC} drops from the normal operating voltage to below the POR threshold voltage, the device stops responding to any instruction sent to it. Before selecting and issuing instructions to the memory, a valid and stable V_{CC} voltage must be applied. This voltage must remain stable and valid until the end of the transmission of the instruction and, for a write instruction, until the completion of the internal write cycle (t_{WR}).

Memory Reset

After an interruption in protocol, power loss, or system reset, any two-wire part is reset with the following steps:

1. Clock up to nine cycles.
2. Look for SDA high in each cycle while SCL is high.
3. Create a start condition as SDA is high.

Table 2. Write Protect

WP Pin Status	Part of the Memory Protected				
	CY24C01	CY24C02	CY24C04	CY24C08	CY24C16
V_{CC}	Full 1K Array	Full 2K Array	Full 4K Array	Full 8K Array	Full 16K Array
V_{SS}	Normal Read/Write Operations				

Figure 2. Start/Stop Definition

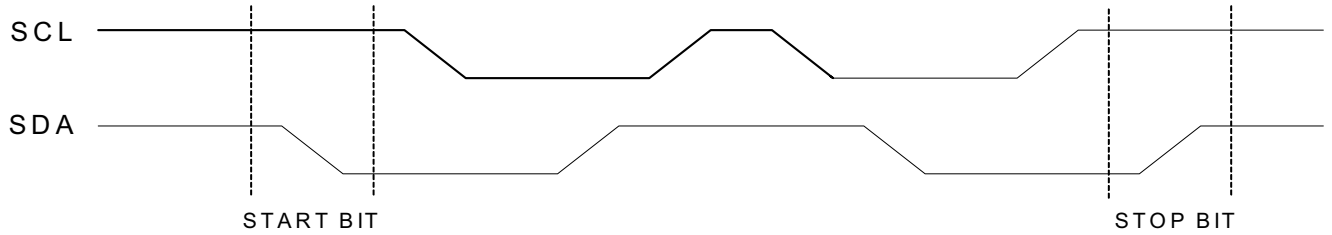
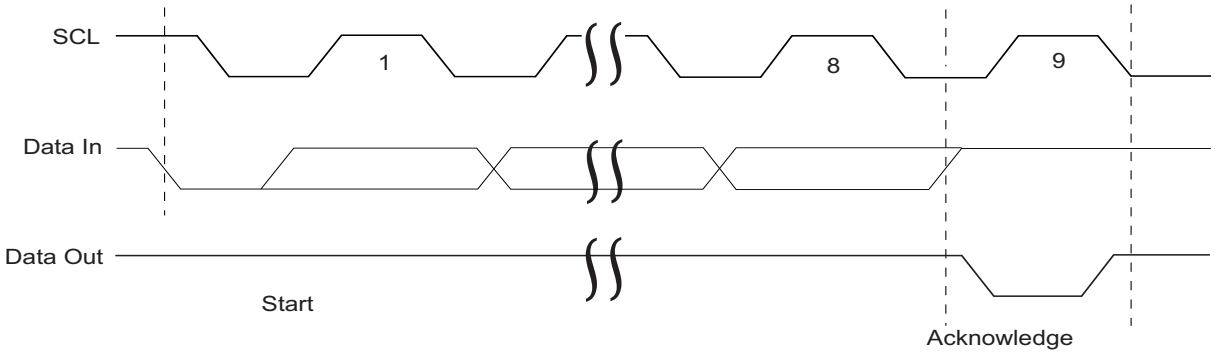


Figure 3. Acknowledge Timing



Device Addressing

The CY24C01/02/04/08/16 EEPROM requires an 8-bit device address word after a start condition, to enable the chip for a read or write operation (refer to Table 3 on page 5).

The device address word consists of a mandatory one, zero sequence for the first four most significant bits as shown in Table 3 on page 5. This is common to all the EEPROM devices.

The next three bits are the A2, A1, and A0 device address bits for CY24C01 and CY24C02. These three bits must compare to their corresponding hard wired input pins.

CY24C04 uses only the A2 and A1 device address bits. The third bit is a memory page address bit. The two device address bits must compare to their corresponding hard wired input pins. The A0 pin is no connect.

CY24C08 only uses the A2 device address bit with the next 2 bits being for memory page addressing. The A2 bit must compare to its corresponding hard wired input pin. The A1 and A0 pins are no connect.

CY24C16 does not use any device address bits and the 3 bits are used for memory page addressing. The page addressing bits on the 4K, 8K, and 16K devices must be considered the most significant bits of the data word address which follows. The A0, A1, and A2 pins are no connect.

The eighth bit of the device address is the read or write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

When the device address is compared, the EEPROM outputs a zero. If a compare is not made, the chip returns to the standby state.

Write Operations

Byte Write

A write operation requires an 8-bit data word address following the device address word and acknowledgment. On receipt of this address, the EEPROM responds with a zero and then clocks in the first 8-bit data word. Following the receipt of the 8-bit data word, the EEPROM outputs a zero. The addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally timed write cycle, t_{WR}, to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM does not respond until the write is complete (see Figure 4 on page 6).

Page Write

The CY24C01/02/04/08/16/CY24C08/CY24C16 devices are capable of 16-byte page writes.

A page write is initiated in the same way as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to 15 more data words. The EEPROM responds with a zero after each data word is received. The microcontroller must terminate the page write sequence with a stop condition (see Figure 5 on page 6).

The lower four bits of the data word address are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the internally generated word address reaches the page boundary, the next byte is placed at the beginning of the same page. If more than 16 data words are transmitted to the EEPROM, the data word address rolls over and the previous data is overwritten.

Acknowledge Polling

When the internally timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling is initiated. This involves sending a start condition followed by the device address word. The read or write bit is representative of the operation desired. After the internal write cycle is complete, the EEPROM responds with a zero, enabling the read or write sequence to continue.

Read Operations

Read operations are initiated in the same way as write operations except that the read or write select bit in the device address word is set to one. There are three read operations: current address read, random address read, and sequential read.

Current Address Read

The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address roll over during read and byte write is from the last byte of the last memory page to the first byte of the first page. The address roll over during write is from the last byte of the current page to the first byte of the same page. After the device address with the read or write select bit set to one is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input zero but generates a stop condition (see Figure 6 on page 6).

Random Read

A random read needs a 'dummy' byte write sequence to load in the data word address. After the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller initiates a current address read by sending a device address with the read or write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a zero but generates a stop condition as shown in Figure 7 on page 6.

Sequential Read

Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledgement. As long as the EEPROM receives an acknowledgement, it continues to increment the data word address and serially clocks out sequential data words. When the address memory limit is reached, the data word address rolls over and the sequential read continues. The sequential read operation is terminated when the microcontroller does not respond with a zero but generates a stop condition (see Figure 8 on page 7).

Table 3. Device Addressing [1,2,3]

Density	Device Type Identifier				Chip Enable Address			
	b7	b6	b5	b4	b3	b2	b1	b0
1K/2K	1	0	1	0	A2	A1	A0	R/$\overline{W}$
4K	1	0	1	0	A2	A1	P0	R/$\overline{W}$
8K	1	0	1	0	A2	P1	P0	R/$\overline{W}$
16K	1	0	1	0	P2	P1	P0	R/$\overline{W}$

Table 4. Operating Modes

Mode	R/$\overline{W}$ Bit	WP	Bytes	Initial Sequence
Current Address Read	1	X	1	Start, Device Select, R/$\overline{W}$ = 1
Random Address Read	0	X	1	Start, Device Select, R/$\overline{W}$ = 0, Address
	1	X		reStart, Device Select, R/$\overline{W}$ = 1
Sequential Read	1	X	≥1	Similar to Current or Random Address Read
Byte Write	0	0	1	Start, Device Select, R/$\overline{W}$ = 0
Page Write	0	0	≤16	Start, Device Select, R/$\overline{W}$ = 0

Notes
1. P2, P1, P0 are used for memory page addressing.
2. A2, A1 and A0 are compared against the respective external pins on the memory device.
3. The MSB b7 is sent first.

Figure 4. Byte Write Timing [4]

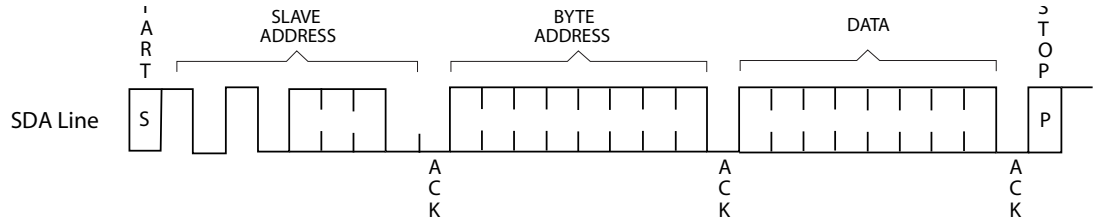


Figure 5. Page Write Timing

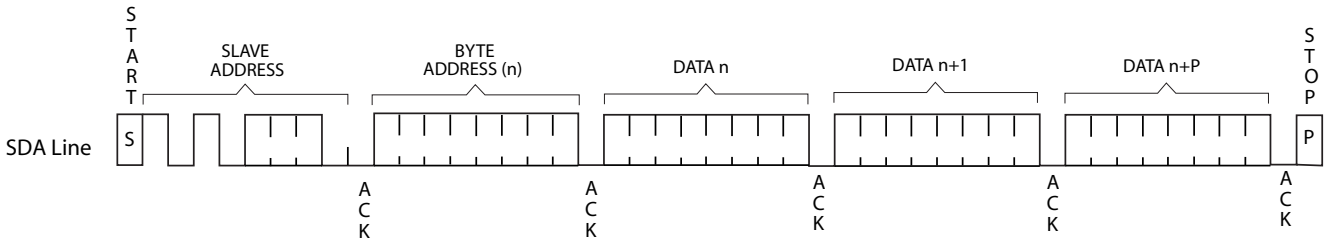


Figure 6. Current Address Read Timing

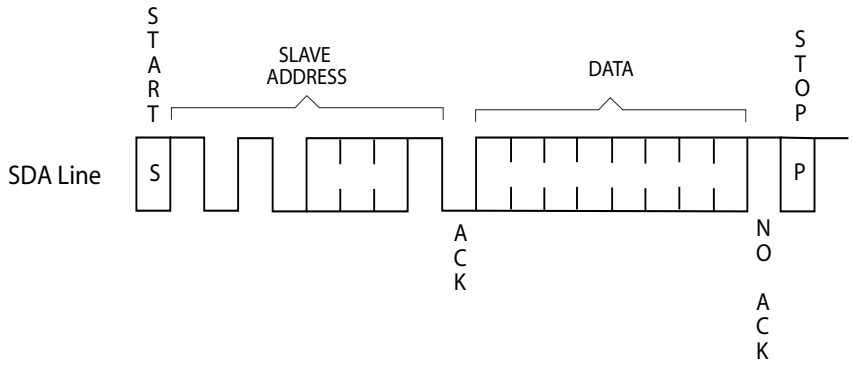
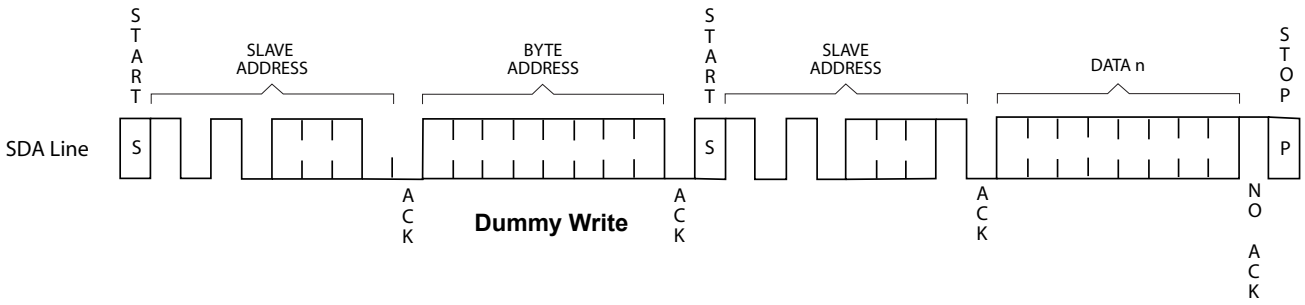
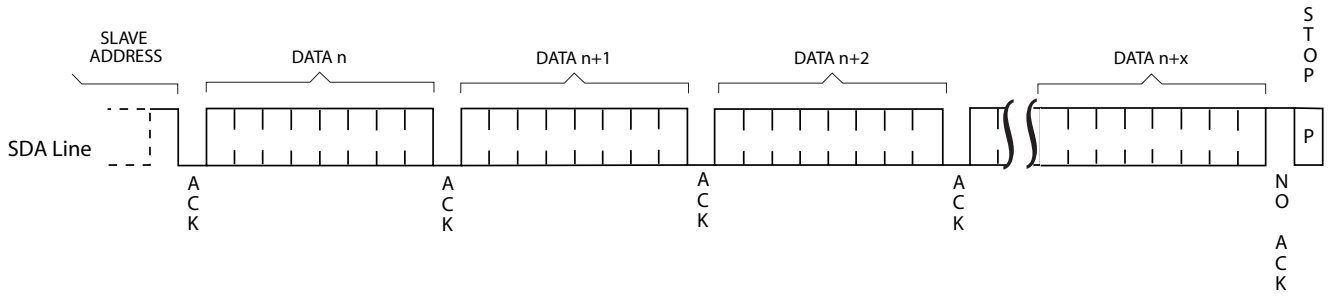


Figure 7. Random Address Read Timing



Note
4. P = 15 for CY24C04/08/16.

Figure 8. Sequential Read Timing



Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –65°C to +150°C

Ambient temperature with power applied ..... –55°C to +125°C

Supply voltage on V_{CC} relative to GND.....–1.0V to +6.0V

DC voltage applied to outputs in high-Z state..... –0.5V to V_{CC} + 1.0V

Input voltage..... –0.5V to V_{CC} + 0.5V

Transient voltage (<20 ns) on any pin to ground potential ..... –1.0V to V_{CC} + 2.0V

Package power dissipation capability (T_A = 25°C) 1.0W

Surface mount lead soldering temperature (3 Seconds)..... +260°C for 10 seconds

Output short circuit current[5] ..... 50 mA

Static discharge voltage..... > 2001V (per MIL-STD-883, Method 3015)

Latch up current ..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Industrial	–40°C to +85°C	1.65V to 5.5V

DC Electrical Characteristics

Over the Operating Range (VCC = 1.65V to 5.5V)

Parameter	Description	Test Conditions	Min	Max	Unit
V_{CC}	Supply Voltage		1.65	5.5	V
I_{SB1}	Standby Current	V_{CC} = 1.65V, V_{IN} = V_{SS} or V_{CC}		1	µA
I_{SB2}	Standby Current	V_{CC} = 2.7V, V_{IN} = V_{SS} or V_{CC}		1.1	µA
I_{SB3}	Standby Current	V_{CC} = 5.5V, V_{IN} = V_{SS} or V_{CC}		1.2	µA
I_{CC1}	Operating Current (READ)	V_{CC} = 5.5V at 1 MHz		2	mA
I_{CC2}	Operating Current (READ)	V_{CC} = 5.5V at 400 KHz		1	mA
I_{CC3}	Operating Current (Write)	V_{CC} = 5.5V		2	mA
I_{LI}	Input Leakage Current	V_{IN} = V_{CC} or V_{SS}.		1	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{CC} or V_{SS}.		1	µA
V_{IL}	Input LOW Voltage	V_{CC} = V_{CC} Min	–0.6 [6]	0.3 V_{CC}	V
V_{IH}	Input HIGH Voltage	V_{CC} = V_{CC} Max	0.7 V_{CC}	V_{CC} + 0.5 [6]	V
V_{OL}	Output LOW Voltage	I_{OL} = 3 mA, V_{CC} = 5.5V		0.4	V
		I_{OL} = 0.15 mA, V_{CC} = 1.8V		0.2	

Note
5. Outputs shorted for only one second. Only one output shorted at a time.
6. This parameter is characterized but not tested.

Capacitance

In the following table, the capacitance parameters are listed. [7]

Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input Capacitance (A0,A1, A2, SCL)	T_A = 25°C, f = 1 MHz, V_{CC} = 1.65V	6	pF
C_{IO}	Input/Output Capacitance (SDA)		8	pF

Thermal Resistance

In the following table, the thermal resistance parameters are listed. [7]

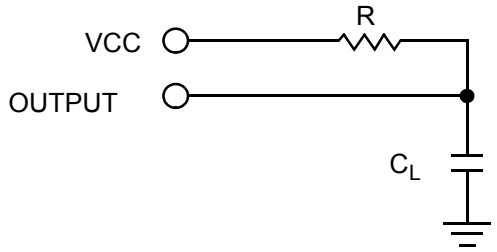
Parameter	Description	Test Conditions	8-SOIC	8-TSSOP	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA / JESD51.	120.83	119.31	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		90.31	82.77	°C/W

Reliability Characteristics

In the following table, the reliability characteristics parameters are listed. [7]

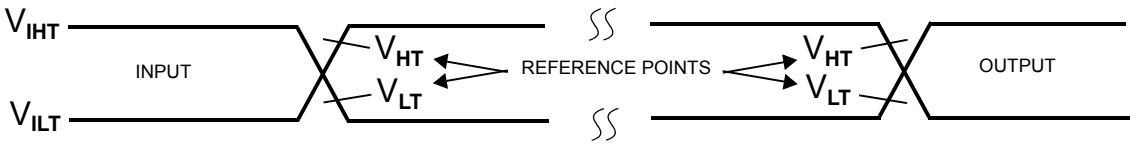
Parameter	Description	Test Method	Min	Unit
N_{END}	Endurance	JEDEC Standard A117	1 Million	Cycles
T_{DR}	Data Rentention	JEDEC Standard A103	100	Years
I_{LTH}	Latch Up	JEDEC Standard 78	100 + I_{CC}	mA

Figure 9. AC Test Loads and Waveforms



Frequency	R (ohm)	C_L (pF)
1 MHz	1.2K	30
100 KHz, 400 KHz	2.7K	100

Figure 10. AC Input and Output Reference Waveforms



AC test inputs are driven at V_{IHT} (0.9 V_{CC}) for a logic '1' and V_{ILT} (0.1 V_{CC}) for a logic '0'. Measurement reference points for inputs and outputs are V_{LT} (V_{CC}/2 - 0.1V) and V_{HT} (V_{CC}/2 + 0.1V). Input rise and fall times (10%–90%) are <100 ns.

Note
7. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

AC Switching Characteristics

Cypress Parameter	Alt Parameter	Description	1 MHz (2.5V - 5.5V)		400 KHz (1.65V - 5.5V)		100 KHz (1.65V - 5.5V)		Unit
			Min	Max	Min	Max	Min	Max	
f_{SCL}	f_{SCL}	Clock Frequency, SCL		1000		400		100	KHz
t_{CL}	t_{LOW}	Clock Pulse Width Low	0.4		0.6		4		µs
t_{CH}	t_{HIGH}	Clock Pulse Width High	0.4		0.6		4		µs
t_{AA}	t_{AA}	Clock Low To Data Out Valid		0.4		0.9		4.5	µs
t_I	t_I	Noise Suppression Time		25		50		50	ns
$t_{S.STA}$	$t_{SU.STA}$	Start Setup Time	0.25		0.6		4		µs
$t_{H.STA}$	$t_{HD.STA}$	Start Hold Time	0.25		0.6		4		µs
t_{SD}	$t_{SU.DAT}$	Data In Setup Time	100		100		200		ns
t_{HD}	$t_{HD.DAT}$	Data In Hold Time	0		0		0		µs
t_{DOH}	t_{DH}	Data Out Hold Time	50		50		100		ns
$t_{S.STO}$	$t_{SU.STO}$	Stop Setup Time	0.25		0.6		4		µs
t_R	t_R	Inputs Rise Time		100		250		1000	ns
t_F	t_F	Inputs Fall Time		100		250		1000	ns
t_{WC}	t_{WR}	Write Cycle Time		5		5		5	ms
t_{BUF} [6]	t_{BUF}	Bus Free Time for New Data Transmission	0.5		1.3		4.7		µs

Figure 11. Bus Timing

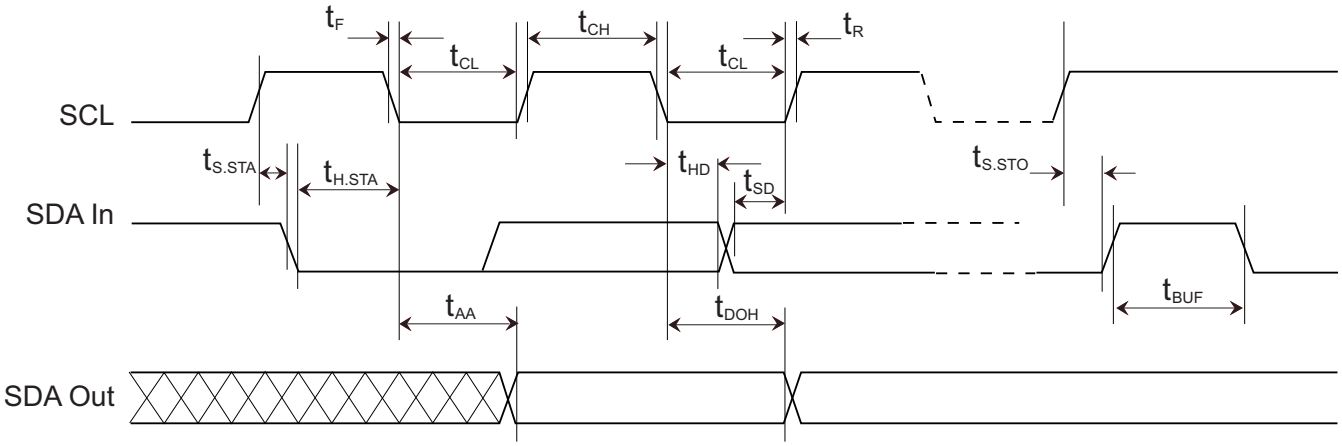
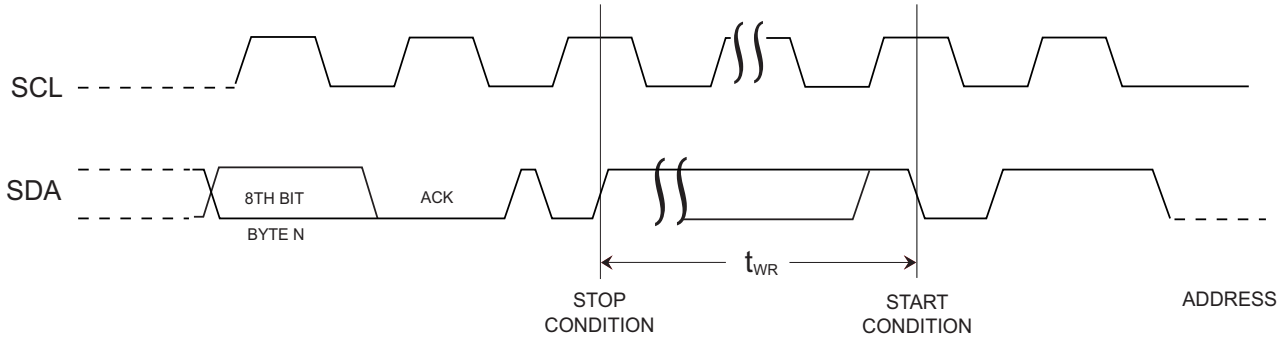
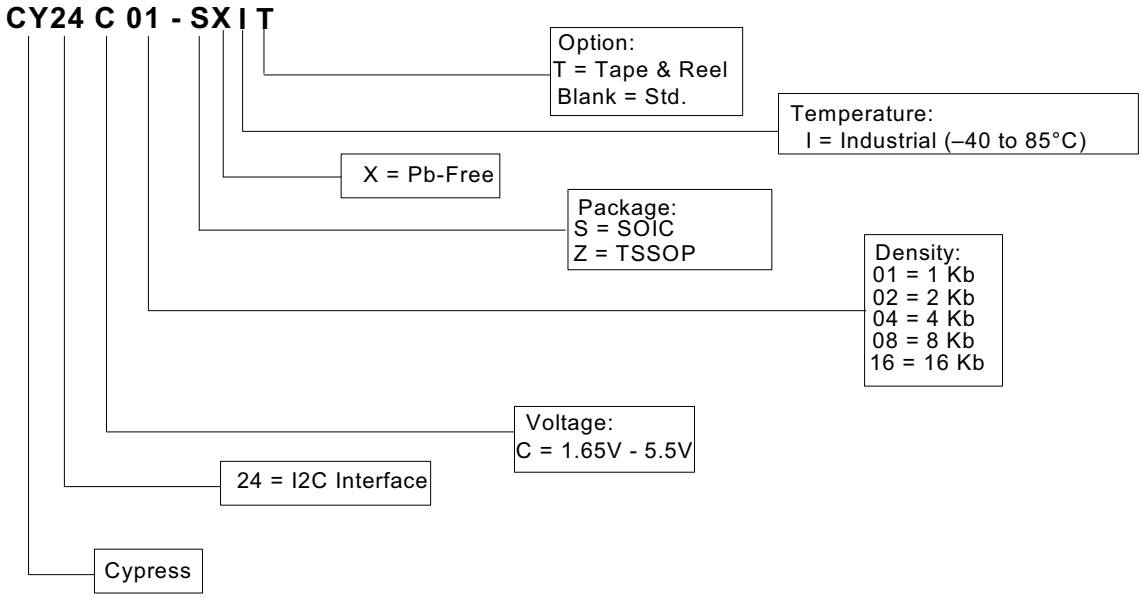


Figure 12. Write Timing



Part Numbering Nomenclature



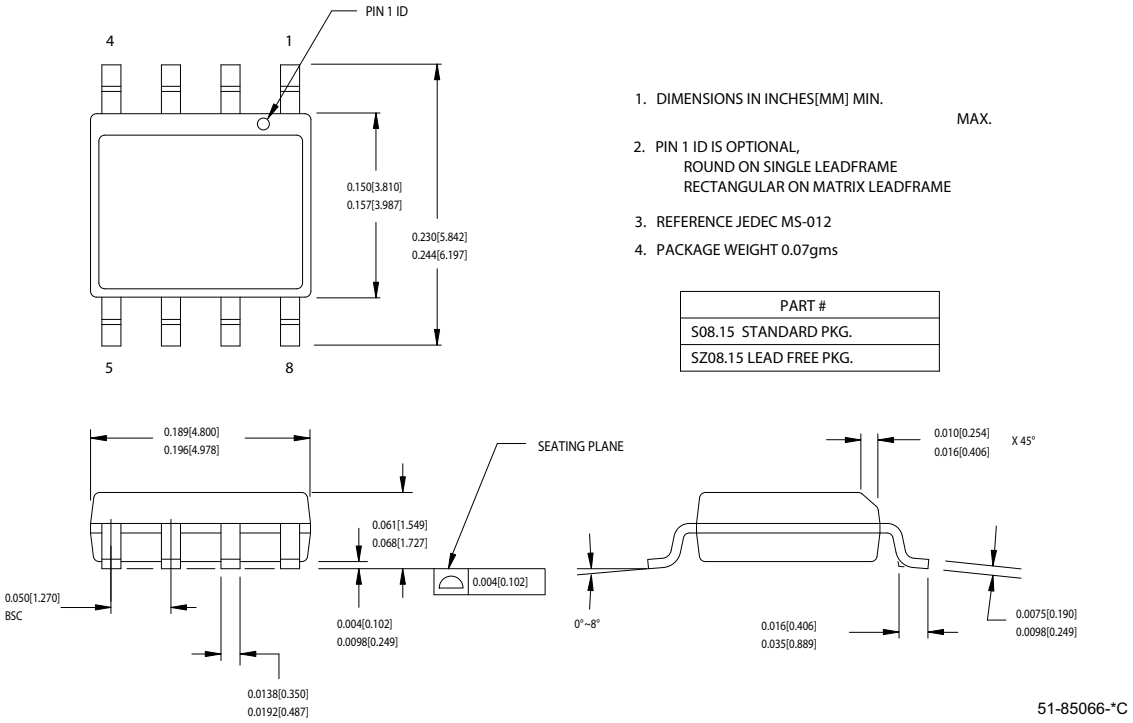
Ordering Information

Density	Ordering Code	Package Diagram	Package Type	Operating Range
1 Kbit	CY24C01-SXI	51-85066	8-Pin SOIC	Industrial
	CY24C01-SXIT		8-Pin SOIC (Tape & Reel)	
	CY24C01-ZXI	51-85093	8-Pin TSSOP	
	CY24C01-ZXIT		8-Pin TSSOP (Tape & Reel)	
2 Kbit	CY24C02-SXI	51-85066	8-Pin SOIC	Industrial
	CY24C02-SXIT		8-Pin SOIC (Tape & Reel)	
	CY24C02-ZXI	51-85093	8-Pin TSSOP	
	CY24C02-ZXIT		8-Pin TSSOP (Tape & Reel)	
4 Kbit	CY24C04-SXI	51-85066	8-Pin SOIC	Industrial
	CY24C04-SXIT		8-Pin SOIC (Tape & Reel)	
	CY24C04-ZXI	51-85093	8-Pin TSSOP	
	CY24C04-ZXIT		8-Pin TSSOP (Tape & Reel)	
8 Kbit	CY24C08-SXI	51-85066	8-Pin SOIC	Industrial
	CY24C08-SXIT		8-Pin SOIC (Tape & Reel)	
	CY24C08-ZXI	51-85093	8-Pin TSSOP	
	CY24C08-ZXIT		8-Pin TSSOP (Tape & Reel)	
16 Kbit	CY24C16-SXI	51-85066	8-Pin SOIC	Industrial
	CY24C16-SXIT		8-Pin SOIC (Tape & Reel)	
	CY24C16-ZXI	51-85093	8-Pin TSSOP	
	CY24C16-ZXIT		8-Pin TSSOP (Tape & Reel)	

Above table contains Preliminary information. Please contact your local Cypress sales representative for availability of these parts.

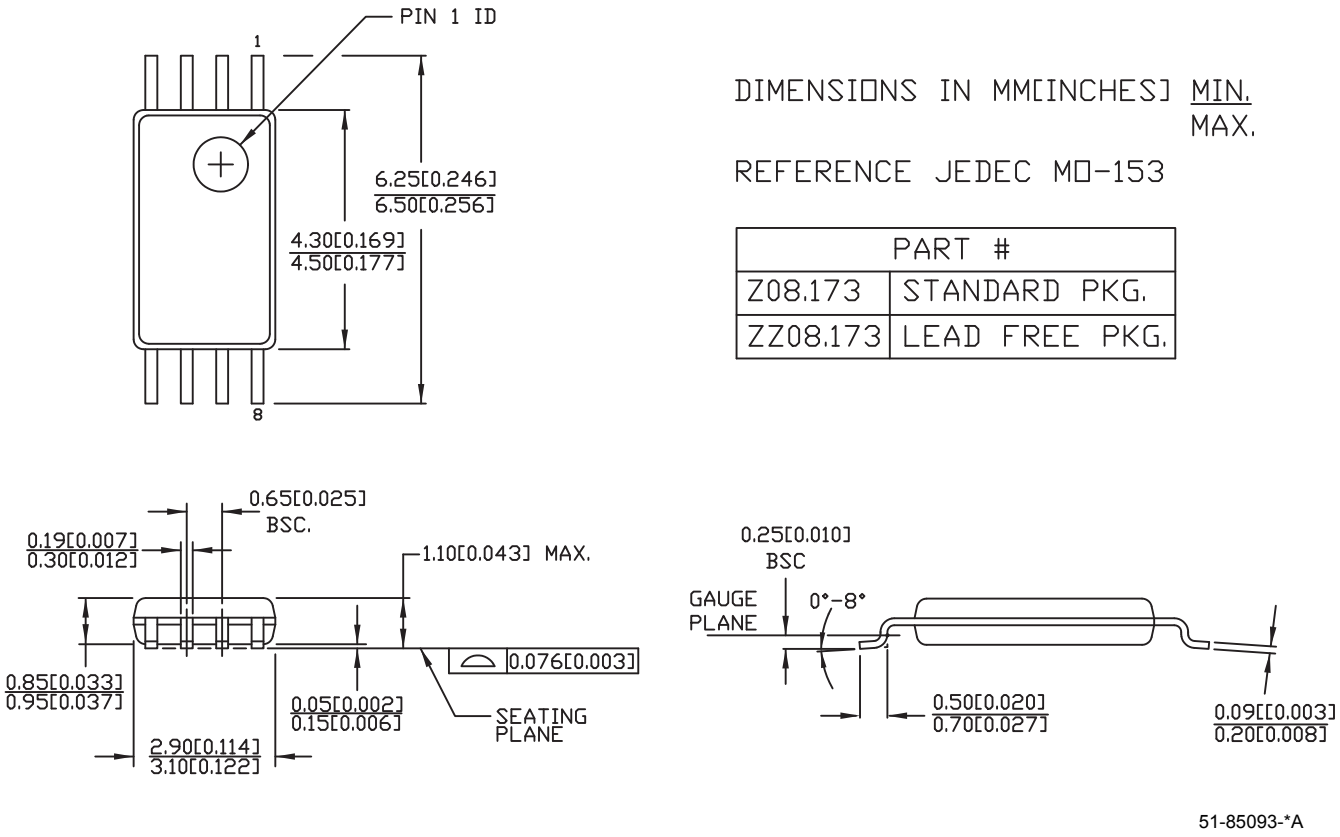
Package Diagrams

Figure 13. 8-Pin (150-Mil) SOIC, 51-85066



Package Diagrams (continued)

Figure 14. 8-Pin (4.4 mm) TSSOP, 51-85093



Document History Page

Document Title: CY24C01/02/04/08/16, 1 Kbit, 2 Kbit, 4 Kbit, 8 Kbit, and 16 Kbit (x8) Two Wire (I2C) Serial EEPROM Document Number: 001-15632				
Revision	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	1069220	UHA	See ECN	New Data Sheet
*A	2522135	GVCH/PYRS	06/27/08	Added Pb-Free and RoHS Compliant information in “Features” Removed PDIP Package Removed Automotive Temperature range Updated Figure 4. Changed Memory page addressing naming convention from A10,A9,A8 to P2,P1,P0 Changed Supply voltage on V_{CC} relative to GND max value from 5.0V to 6.0V Corrected Typo of Vcc max value from 5.0V to 5.5V Added I_{CC1} spec for 1 MHz Table 8: Added Thermal Resistance values for 8-TSSOP package Added AC test load values for different Frequency Table 10: Added tI (Noise suppression time) value for 1 MHz and 100 KHz Frequency Updated Part Numbering Nomenclature and Ordering Information
*B	2611873	VKN/PYRS	11/24/08	Added 1 Kbit and 2 Kbit parts and their related information
*C	2656511	VKN/PYRS	02/09/09	Converted from preliminary to final Changed V_{CC} operating range for 1MHz operation from 1.65V-5.5V to 2.5V-5.5V Changed I_{CC3} spec from 1.5mA to 2mA Added footnote #6 Updated V_{OL} test conditions On page 9, corrected AC measurement reference points from V_{IT} and V_{OT} to V_{LT} and V_{HT} respectively Changed V_{LT} level from $0.3V_{CC}$ to $V_{CC}/2$ - 0.1V Changed V_{HT} level from $0.7V_{CC}$ to $V_{CC}/2$ + 0.1V

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