

Spread Spectrum Clock Generator IC

Features

- Supports Clock requirements for Printers
- 48 MHz Spread Spectrum Clock Output
- Reference Clock Output
- Two Spread Bandwidths: -1%, -3%
- Integrated Loop Filter
- 48 MHz External Clock or Cera-Lock Filter Input
- 3.3V operation (2.5V functional)
- 8-pin SOIC Package

Functional Description

The CY27020 clock generator provides a low EMI clock output for printers. It features Spread Spectrum technology, a modulation technique designed specifically for reducing EMI at fundamental frequency and its harmonics.

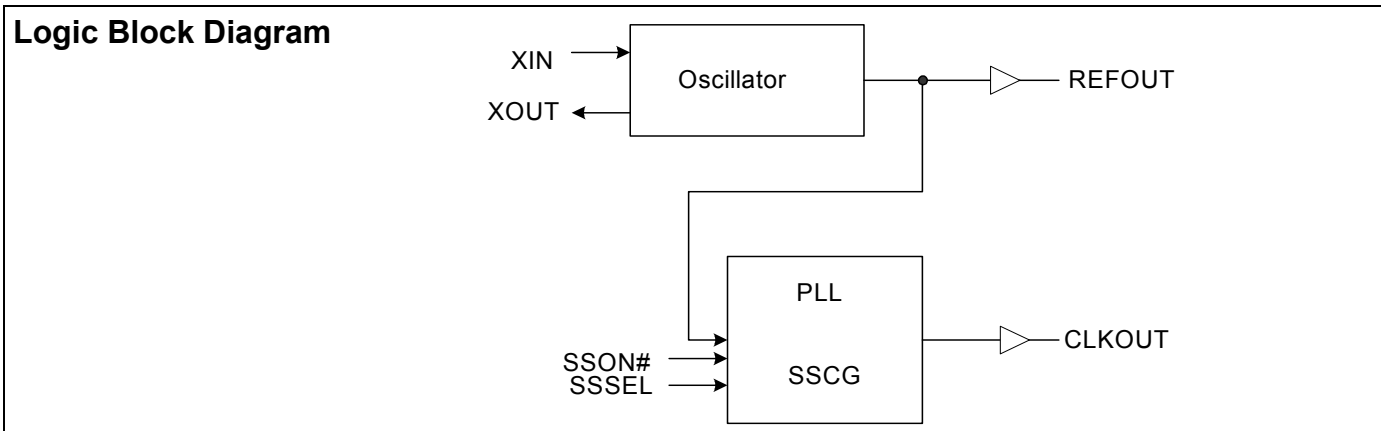
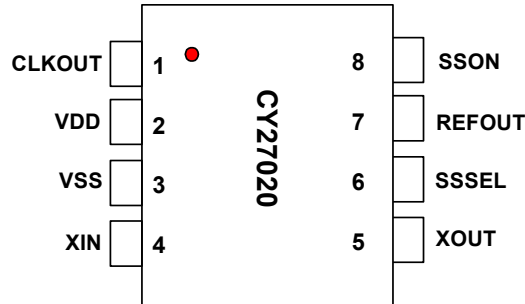


Table 1. Frequency Table

| XIN | SSON | SSSEL | REFOUT | CLKOUT |
|-----------|------|-----------------|-----------|-----------------------|
| 48.00 MHz | 0 | 0 | 48.00 MHz | 48.00 MHz at -1% |
| 48.00 MHz | 0 | 1 | 48.00 MHz | 48.00 MHz at -3% |
| 48.00 MHz | 1 | does not matter | 48.00 MHz | 48.00 MHz (No Spread) |

Pin Configuration

Figure 1. 8-Pin SOIC



Pin Description

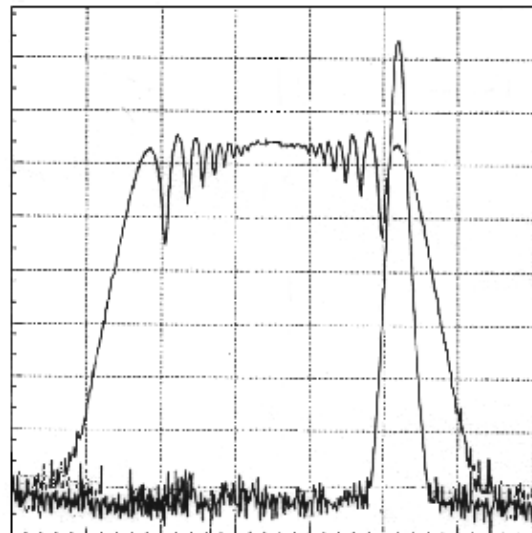
| Pin | Name | I/o | Type ^[1] | Description |
|-----|--------|-----|---------------------|--|
| 1 | CLKOUT | O | | Fixed Frequency 48.00 MHz Spread Spectrum Clock Output. See Table 1 on page 1 for frequency selections |
| 2 | VDD | PWR | | 3.3V Power Supply |
| 3 | VSS | PWR | | Common Ground |
| 4 | XIN | I | | Oscillator Buffer Input. Connect to an external parallel resonant crystal (nominally 48.00 MHz) or externally generated 48 MHz reference clock. |
| 5 | XOUT | O | | Oscillator Buffer Output. Connect to an external parallel resonant crystal. Do not connect when an externally generated reference clock is applied at XIN. |
| 6 | SSSEL | I | PU | Spread Spectrum Bandwidth (BW%) Selection Input. See Table 1 on page 1 for selections. |
| 7 | REFOUT | O | – | Buffered Output of XIN. |
| 8 | SSON | I | PD | Spread Spectrum Enable Input. When asserted LOW, Spread Spectrum is enabled. |

Spread Spectrum Clock Generation (SSCG)

Spread Spectrum Clock Generator (SSCG) is a frequency modulation technique used to reduce electromagnetic interference radiation generated by repetitive digital signals, mainly clocks. A clock accumulates EM energy at its center frequency and its harmonics. Spread Spectrum distributes this energy over a small frequency bandwidth and decreases the peak value of radiated energy over the spectrum. This technique is achieved by modulating the clock around or below the center of its resting frequency by a certain percentage (which also determines the energy distribution bandwidth).

The SSCG function is enabled when SSON pin is asserted low resulting in a spread bandwidth that is down spread by either -1% or -3% selected by SSSEL (see Table 1 on page 1).

Figure 2. Down Spread



Note

1. PU = Internal Pull-up, PD = Internal Pull-down.

Absolute Maximum Conditions

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.^[2]

Maximum Input Voltage Relative to V_{SS} : $V_{SS} - 0.3V$
 Maximum Input Voltage Relative to V_{DD} : $V_{DD} + 0.3V$
 Storage Temperature: $-65^{\circ}C$ to $+150^{\circ}C$
 Operating Temperature: $0^{\circ}C$ to $+70^{\circ}C$
 Maximum ESD protection: 2 kV
 Maximum Power Supply: 5.5V
 Operating Voltage: 2.5–3.6V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, care should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, V_{in} and V_{out} should be constrained to the range:

$$V_{SS} < (V_{in} \text{ or } V_{out}) < V_{DD}$$

Unused inputs must always be tied to an appropriate logic voltage level (either V_{SS} or V_{DD}).

DC Parameters ($V_{DD} = 3.3V \pm 10\%$, $T_A = 0^{\circ}C$ to $+70^{\circ}C$)^[3,4]

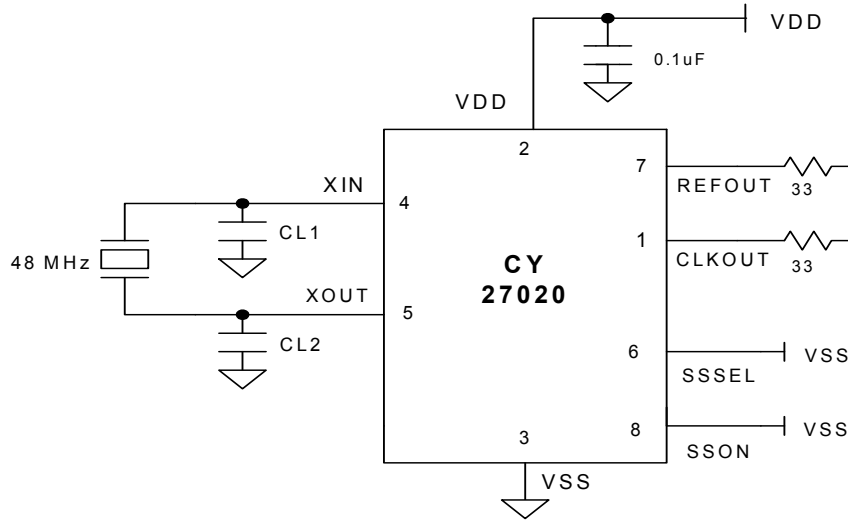
| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|--------------|------------------------------|--------------------|--------------------|--------------------|--------------------|-----------|
| V_{IL} | Input Low Voltage | SSON, SSSEL | | | 0.8 | V |
| V_{IH} | Input High Voltage | | 2.2 | | | V |
| V_{thXIN} | XIN Threshold Voltage | | $0.3 \cdot V_{DD}$ | $0.5 \cdot V_{DD}$ | $0.7 \cdot V_{DD}$ | V |
| I_{IL1} | Input Low Current | SSON# = V_{SS} | -5 | 0 | 5 | μA |
| I_{IH1} | Input High Current | SSON# = V_{DD} | 3 | 8 | 20 | μA |
| I_{IL2} | Input Low Current | SSEL = V_{SS} | -36 | -16.5 | -7.4 | μA |
| I_{IH2} | Input High Current | SSEL = V_{DD} | -5 | 0 | 5 | μA |
| $I_{dd3.3V}$ | Dynamic Supply Current | No Output Load | | 20 | 25 | mA |
| V_{OL} | Output Low Voltage | $I_{OL} = 4.0$ mA | | | 0.4 | V |
| V_{OH} | Output High Voltage | $I_{OH} = -4.0$ mA | 2.4 | | | V |
| C_{in} | Input Capacitance | Pins 6 and 8 | | 3 | 5 | pF |
| C_x | XIN, XOUT Capacitance | Pins 4 and 5 | | 3 | 5 | pF |
| PU/PD | Pull Up/Pull Down Resistance | SSON, SSSEL | 100 | 200 | 400 | $k\Omega$ |

AC Parameters

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|-----------|---|----------------------|-----|-----|-----|------|
| IFR | Input Frequency Range | | 44 | 48 | 52 | MHz |
| t_r | Rise Time ^[5,6] | | | 1 | 2 | ns |
| t_f | Fall Time ^[5,6] | | | 1 | 2 | ns |
| BW% | Bandwidth Spread in% | SSON# = 0, SSSEL = 0 | | -1 | | % |
| BW% | Bandwidth Spread in% | SSON# = 0, SSSEL = 1 | | -3 | | % |
| t_{PU} | Power up to Stable Output ^[7] | All output clocks | | | 3 | ms |
| t_{DC} | Clock Duty Cycle ^[5,7] | CL = 15 pF | 45 | 50 | 55 | % |
| t_{ccj} | REFOUT Cycle to Cycle jitter ^[5,7] | CL = 15 pF | | | 350 | ps |
| t_{ccj} | CLKOUT Cycle to Cycle jitter ^[5,7] | | | 100 | 250 | ps |

Notes

- Multiple Supplies:** The Voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.
- Although internal pull-down, pull-up resistors have a typical value of 200K (range 100K to 400K).
- In applications if a crystal is used for the input reference clock, refer to crystal manufacturer's specifications for the required crystal load capacitor value.
- Parameters are guaranteed by design and characterization. Not 100% tested in production. All parameters specified with fully loaded outputs. All outputs loaded with 15 pF.
- Measured between $0.1 \cdot V_{DD}$ and $0.9 \cdot V_{DD}$ volts.
- Triggering is done at 1.5V.

Figure 2. Application Schematic^[8,9]


Ordering Information

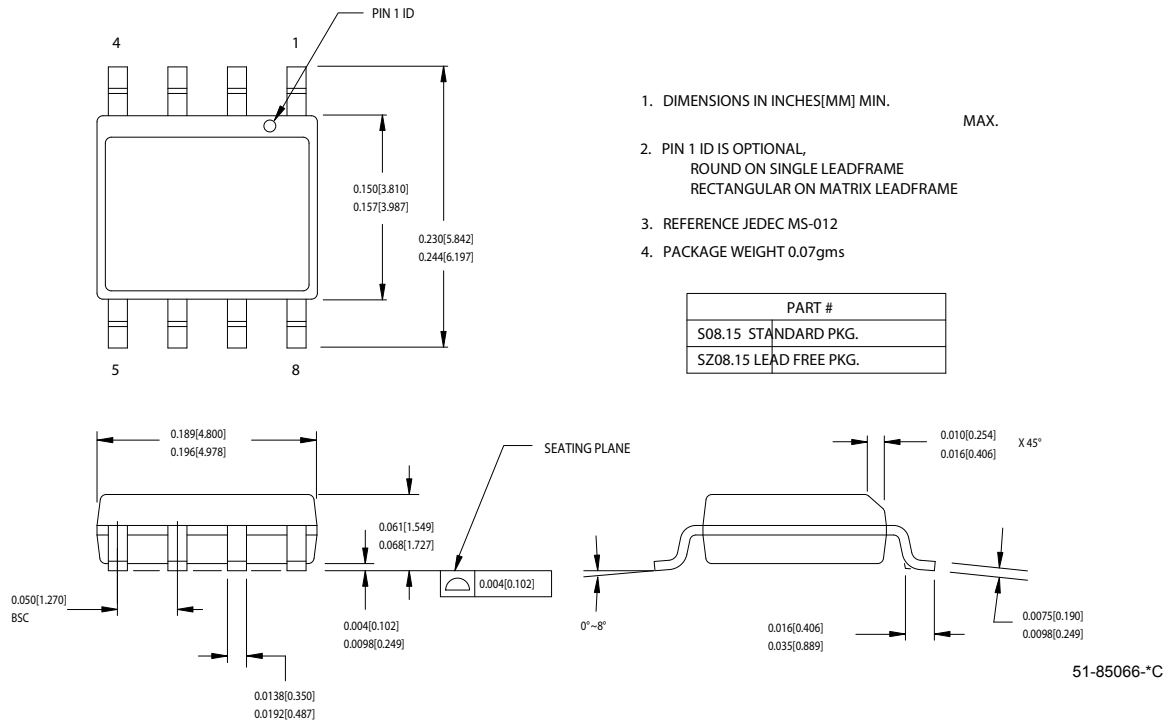
| Part Number | Package Type | Production Flow |
|----------------|----------------------------|--------------------------|
| CY27020SC | 8-Pin SOIC | Commercial, 0°C to +70°C |
| CY27020SCT | 8-Pin SOIC - Tape and Reel | Commercial, 0°C to +70°C |
| Pb-free | | |
| CY27020SXC | 8-Pin SOIC | Commercial, 0°C to +70°C |
| CY27020SXCT | 8-Pin SOIC - Tape and Reel | Commercial, 0°C to +70°C |

Notes

- The circuit shows -1.0% spread. Refer to [Table 1](#) on page 1 for selections.
- Use crystal or Cera-Lock Filter manufacturer's recommended values for CL1 and CL2 load capacitors.

Package Drawing and Dimension

Figure 3. 8-Pin (150-Mil) SOIC



Document History Page

| Document Title: CY27020 Spread Spectrum Clock Generator IC Document Number: 38-07273 | | | | |
|---|---------|-----------------|-----------------|---|
| REV. | ECN NO. | Submission Date | Orig. of Change | Description of Change |
| ** | 110661 | 02/19/02 | XHT | New data sheet |
| *A | 122868 | 12/21/02 | RBI | Add power up requirements to maximum rating information |
| *B | 279429 | See ECN | RGL | Added Lead-free Devices |
| *C | 2759365 | 09/02/2009 | TSAI | Updated template. Post to external web. |

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