CY2SSTU32866

1.8V, 25-bit (1:1) or 14-bit (1:2) JEDEC-Compliant Data Register with Parity

Features

- **Operating frequency: DC to 500 MHz**
- **Supports DDRII SDRAM**
- **Two operations modes: 25 bit (1:1) and 14 bit (1:2)**
- **1.8V operation**
- **Fully JEDEC-compliant (JESD 82-10)**
- **96-ball FBGA**

Functional Description

All clock and data inputs are compatible with the JEDEC standard for SSTL_18. The control inputs are LVCMOS. All outputs are 1.8-V CMOS drivers that have been optimized to drive the DDR-II DIMM load. The CY2SSTU32866 operates from a differential clock (CK and CK#). Data are registered at the crossing of CK going high, and CK# going LOW.

The C0 input controls the pinout configuration of the 1:2 pinout from A configuration (when LOW) to B configuration (when HIGH). The C1 input controls the pinout configuration from 25-bit 1:1 (when LOW) to 14-bit 1:2 (when HIGH).

The device monitors both DCS# and CSR# inputs and will gate the Qn outputs from changing states when both DCS# and CSR# inputs are HIGH. If either DCS# or CSR# input is LOW, the Qn outputs will function normally. The RESET# input has priority over the DCS# and CSR# control and will force the outputs LOW. If the DCS#-control functionality is not desired, the CSR# input can be hardwired to ground, in which case the set-up time requirement for DCS# would be the same as for the other D data inputs.

The device supports low-power standby operation. When the reset input (RESET#) is LOW, the differential input receivers are disabled, and undriven (floating) data, clock, and reference voltage (VREF) inputs are allowed. In addition, when RESET# is LOW, all registers are reset and all outputs are forced LOW. The LVCMOS RESET# and Cn inputs must always be held at a valid logic HIGH or LOW level. To ensure defined outputs from the register before a stable clock has been supplied, RESET# must be held in the LOW state during power-up.

In the DDR-II RDIMM application, RESET# is specified to be completely asynchronous with respect to CK and CK#. Therefore, no timing relationship can be guaranteed between the two. When entering reset, the register will be cleared and the outputs will be driven low quickly, relative to the time to disable the differential input receivers. However, when coming out of reset, the register will become active quickly, relative to the time to enable the differential input receivers.

Pin Configuration

	1	2	3	4	5	6
A	DCKE	PPO	VREF	VDD	QCKE	NC
B	D2	D15	GND	GND	Q2	Q15
C	D3	D16	VDD	VDD	Q3	Q16
D	DODT	QERR#	GND	GND	QODT	NC
E	D5	D17	VDD	VDD	Q5	Q17
F	D6	D18	GND	GND	Q6	Q18
G	PAR IN	RST#	VDD	VDD	C1	C0
H	CK	DCS#	GND	GND	QCS#	NC
J	CK#	CSR#	VDD	VDD	ZOH	ZOL
K	D8	D19	GND	GND	Q8	Q19
L	D9	D20	VDD	VDD	Q9	Q20
M	D10	D21	GND	GND	Q10	Q21
N	D11	D22	VDD	VDD	Q11	Q22
P	D12	D23	GND	GND	Q12	Q23
R	D13	D24	VDD	VDD	Q13	Q24
T	D14	D25	VREF	VDD	Q14	Q25
	1	2	3	4	5	6

1:1 Register C0 = 0, C1=0

	1	2	3	4	5	6
A	DCKE	PPO	VREF	VDD	QCKEA	QCKEB
B	D2	NC	GND	GND	Q2A	Q2B
C	D3	NC	VDD	VDD	Q3A	Q3B
D	DODT	QERR#	GND	GND	QODTA	QODTB
E	D5	NC	VDD	VDD	Q5A	Q5B
F	D6	NC	GND	GND	Q6A	Q6B
G	PAR IN	RST#	VDD	VDD	C1	C0
H	CK	DCS#	GND	GND	QCSA#	QCSB#
J	CK#	CSR#	VDD	VDD	ZOH	ZOL
K	D8	NC	GND	GND	Q8A	Q8B
L	D9	NC	VDD	VDD	Q9A	Q9B
M	D10	NC	GND	GND	Q10A	Q10B
N	D11	NC	VDD	VDD	Q11A	Q11B
P	D12	NC	GND	GND	Q12A	Q12B
R	D13	NC	VDD	VDD	Q13A	Q13B
T	D14	NC	VREF	VDD	Q14A	Q14B
	1	2	3	4	5	6

1:2 Register A C0 = 0, C1=1

	1	2	3	4	5	6
A	D1	PPO	VREF	VDD	Q1A	Q1B
B	D2	NC	GND	GND	Q2A	Q2B
C	D3	NC	VDD	VDD	Q3A	Q3B
D	D4	QERR#	GND	GND	Q4A	Q4B
E	D5	NC	VDD	VDD	Q5A	Q5B
F	D6	NC	GND	GND	Q6A	Q6B
G	PAR IN	RST#	VDD	VDD	C1	C0
H	CK	DCS#	GND	GND	QCSA#	QCSB#
J	CK#	CSR#	VDD	VDD	ZOH	ZOL
K	D8	NC	GND	GND	Q8A	Q8B
L	D9	NC	VDD	VDD	Q9A	Q9B
M	D10	NC	GND	GND	Q10A	Q10B
N	DODT	NC	VDD	VDD	QODTA	QODTB
P	D12	NC	GND	GND	Q12A	Q12B
R	D13	NC	VDD	VDD	Q13A	Q13B
T	DCKE	NC	VREF	VDD	QCKEA	QCKEB
	1	2	3	4	5	6

1:2 Register B C0 = 1, C1=1

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The CY2SSTV32866 accepts a parity bit from the memory controller on its parity bit (PAR_IN) input, compares it with the data received on the DIMM-independent D-inputs and indicates whether a parity error has occurred on its open-drain QERR# pin (active LOW). The convention is even parity, i.e., valid parity is defined as an even number of ones across the DIMM-independent data inputs combined with the parity input bit.

When used as a single device, the C0 and C1 inputs are tied LOW. In this configuration, parity is checked on the PAR_IN input which arrives one cycle after the input data to which it applies. The partial-parity-out (PPO) and QERR# signals are produced three cycles after the corresponding data inputs.

When used in pairs, the C0 input of the first register is tied LOW and the C0 input of the second register is tied HIGH. The C1 input of both registers are tied HIGH. Parity, which arrives one cycle after the data input to which it applies, is checked on the PAR_IN input of the first device. The PPO and QERR# signals are produced on the second device three clock cycles after the corresponding data inputs. The PPO output of the first register is cascaded to the PAR_IN of the second register. The QERR# output of the first register is left floating and the valid error information is latched on the QERR# output of the second register. If an error occurs and the QERR# output is driven LOW, it stays latched LOW for two clock cycles or until RESET# is driven LOW. The DIMM-dependent signals (DCKE, DCS#, DODT, and CSR#) are not included in the parity check computation.

Parity is calculated using *Table 1*.

Table 1. Parity Function Table

Inputs							Outputs	
RESET#	**DCS#**	**CSR#**	**CK**	**CK#**	**Sum of inputs = H (D1-25)**	**PAR_IN**	**PPO**	**QERR#**
H	L	X	↓↑	↓↑	Even	L	L	H
H	L	X	↓↑	↓↑	Odd	L	H	L
H	L	X	↓↑	↓↑	Even	H	H	L
H	L	X	↓↑	↓↑	Odd	H	L	H
H	H	L	↓↑	↓↑	Even	L	L	H
H	H	L	↓↑	↓↑	Odd	L	H	L
H	H	L	↓↑	↓↑	Even	H	H	L
H	H	L	↓↑	↓↑	Odd	H	L	H
H	H	H	↓↑	↓↑	X	X	PPO_0	$QERR\#_0$
H	X	X	L or H	L or H	X	X	PPO_0	$QERR\#_0$
L	X or Floating	X or Floating	X or Floating	X or Floating	X or Floating	X or Floating	L	H

Pin Definition

Pin Name	Pin Number (C0 = 0, C1 = 0)	Pin Number (C0 = 0, C1 = 1)	Pin Number (C0 = 1, C1 = 1)	Description
GND	B3, B4, D3, D4, F3, F4, H3, H4, K3, K4, M3, M4, P3, P4	B3, B4, D3, D4, F3, F4, H3, H4, K3, K4, M3, M4, P3, P4	B3, B4, D3, D4, F3, F4, H3, H4, K3, K4, M3, M4, P3, P4	Ground
VDD	A4, C3, C4, E3, E4, G3, G4, J3, J4, L3, L4, N3, N4, R3, R4, T4	A4, C3, C4, E3, E4, G3, G4, J3, J4, L3, L4, N3, N4, R3, R4, T4	A4, C3, C4, E3, E4, G3, G4, J3, J4, L3, L4, N3, N4, R3, R4, T4	Power Supply Voltage
VREF	A3, T3	A3, T3	A3, T3	Input Reference Voltage
ZOH	J5	J5	J5	Reserved
ZOL	J6	J6	J6	Reserved
CK	H1	H1	H1	Positive Master Clock
CK#	J1	J1	J1	Negative Master Clock
C0	G6	G6	G6	Configuration control input
C1	G5	G5	G5	Configuration control input

Pin Definition (continued)

Pin Name	Pin Number (C0 = 0, C1 = 0)	Pin Number (C0 = 0, C1 = 1)	Pin Number (C0 = 1, C1 = 1)	Description
RESET#	G2	G2	G2	Asynchronous reset – resets registers and disables Vref data and clock differential input receivers
CSR#	J2	J2	J2	Chip Select – Disables D1-D24 when both CSR# and DCS# are HIGH (V_{DD})
DCS#	H2	H2	H2	Chip Select – Disables D1-D24 when both CSR# and DCS# are HIGH (V_{DD})
D1			A1	Data input – clocked in on the crossing points of CK and CK#
D2-3	B1, C1	B1, C1	B1, C1	Data input – clocked in on the crossing points of CK and CK#
D4			D1	Data input – clocked in on the crossing points of CK and CK#
D5, 6, 8, 9, 10	E1, F1, K1, L1, M1	E1, F1, K1, L1, M1	E1, F1, K1, L1, M1	Data input – clocked in on the crossing points of CK and CK#
D11	N1	N1		Data input – clocked in on the crossing points of CK and CK#
D12, 13	P1, R1	P1, R1	P1, R1	Data input – clocked in on the crossing points of CK and CK#
D14	T1	T1		Data input – clocked in on the crossing points of CK and CK#
D15-25	B2, C2, E2, F2, K2, L2, M2, N2, P2, R2, T2			Data input – clocked in on the crossing points of CK and CK#
DODT	D1	D1	N1	The outputs of this register bit will not be suspended by the DCS# and CSR# Control
DCKE	A1	A1	T1	The outputs of this register bit will not be suspended by the DCS# and CSR# Control
Q1A			A5	Data Outputs that are suspended by the DCS# and CSR# control
Q2A-3A	B5, C5	B5, C5	B5, C5	Data Outputs that are suspended by the DCS# and CSR# control
Q4A			D5	Data Outputs that are suspended by the DCS# and CSR# control
Q5A, 6A, 8A, 9A, 10A	E5, F5, K5, L5, M5	E5, F5, K5, L5, M5	E5, F5, K5, L5, M5	Data Outputs that are suspended by the DCS# and CSR# control
Q11A	N5	N5		
Q12A, Q13A	P5, R5	P5, R5	P5, R5	
Q14A	T5	T5		Data Outputs that are suspended by the DCS# and CSR# control
Q1B			A6	Data Outputs that are suspended by the DCS# and CSR# control
Q2B-3B		B6, C6	B6, C6	Data Outputs that are suspended by the DCS# and CSR# control
Q4B			D6	Data Outputs that are suspended by the DCS# and CSR# control
Q5B, 6B, 8B, 9B, 10B,		E6, F6, K6, L6, M6	E6, F6, K6, L6, M6	Data Outputs that are suspended by the DCS# and CSR# control
Q11B		N6		Data Outputs that are suspended by the DCS# and CSR# control

Pin Definition (continued)

Pin Name	Pin Number (C0 = 0, C1 = 0)	Pin Number (C0 = 0, C1 = 1)	Pin Number (C0 = 1, C1 = 1)	Description
Q12B, 13B		P6, R6	P6, R6	Data Outputs that are suspended by the DCS# and CSR# control
Q14B		T6		Data Outputs that are suspended by the DCS# and CSR# control
Q15-25	B6, C6, E6, F6, K6, L6, M6, N6, P6, R6, T6			Data Outputs that are suspended by the DCS# and CSR# control
QCSA#	H5	H5	H5	Data outputs that will not be suspended by the DCS# and CSR# control
QCSB#		H6	H6	Data outputs that will not be suspended by the DCS# and CSR# control
QODTA	D5	D5	N5	Data outputs that will not be suspended by the DCS# and CSR# control
QODTB		D6	N6	Data outputs that will not be suspended by the DCS# and CSR# control
QCKEA	A5	A5	T5	Data outputs that will not be suspended by the DCS# and CSR# control
QCKEB		A6	T6	Data outputs that will not be suspended by the DCS# and CSR# control
PPO	A2	A2	A2	Partial parity out – indicates odd parity of inputs D1-D25
QERR#	D2	D2	D2	Output error bit – generated one clock cycle after the corresponding data output
PAR_IN	G1	G1	G1	Parity input – arrives one clock cycle after the corresponding data input
NC	A6, D6, H6	B2, C2, E2, F2, K2, L2, M2, N2, P2, R2, T2	B2, C2, E2, F2, K2, L2, M2, N2, P2, R2, T2	No Connect Pins

Table 2. Flip Flop Function Table

Inputs						Outputs		
RESET#	DCS#	CSR#	CK	CK#	Dn, DODT, DCKE	Qn	QCS#	QODT, QCKE
H	L	L	↓↑	↓↑	L	L	L	L
H	L	L	↓↑	↓↑	H	H	L	H
H	L	L	L or H	L or H	X	Q0	Q0	Q0
H	L	H	↓↑	↓↑	L	L	L	L
H	L	H	↓↑	↓↑	H	H	L	H
H	L	H	L or H	L or H	X	Q0	Q0	Q0
H	H	L	↓↑	↓↑	L	L	H	L
H	H	L	↓↑	↓↑	H	H	H	H
H	H	L	L or H	L or H	X	Q0	Q0	Q0
H	H	H	↓↑	↓↑	L	Q0	H	L
H	H	H	↓↑	↓↑	H	Q0	H	H
H	H	H	L or H	L or H	X	Q0	Q0	Q0
L	X or Floating	X or Floating	X or Floating	X or Floating	X or Floating	L	L	L

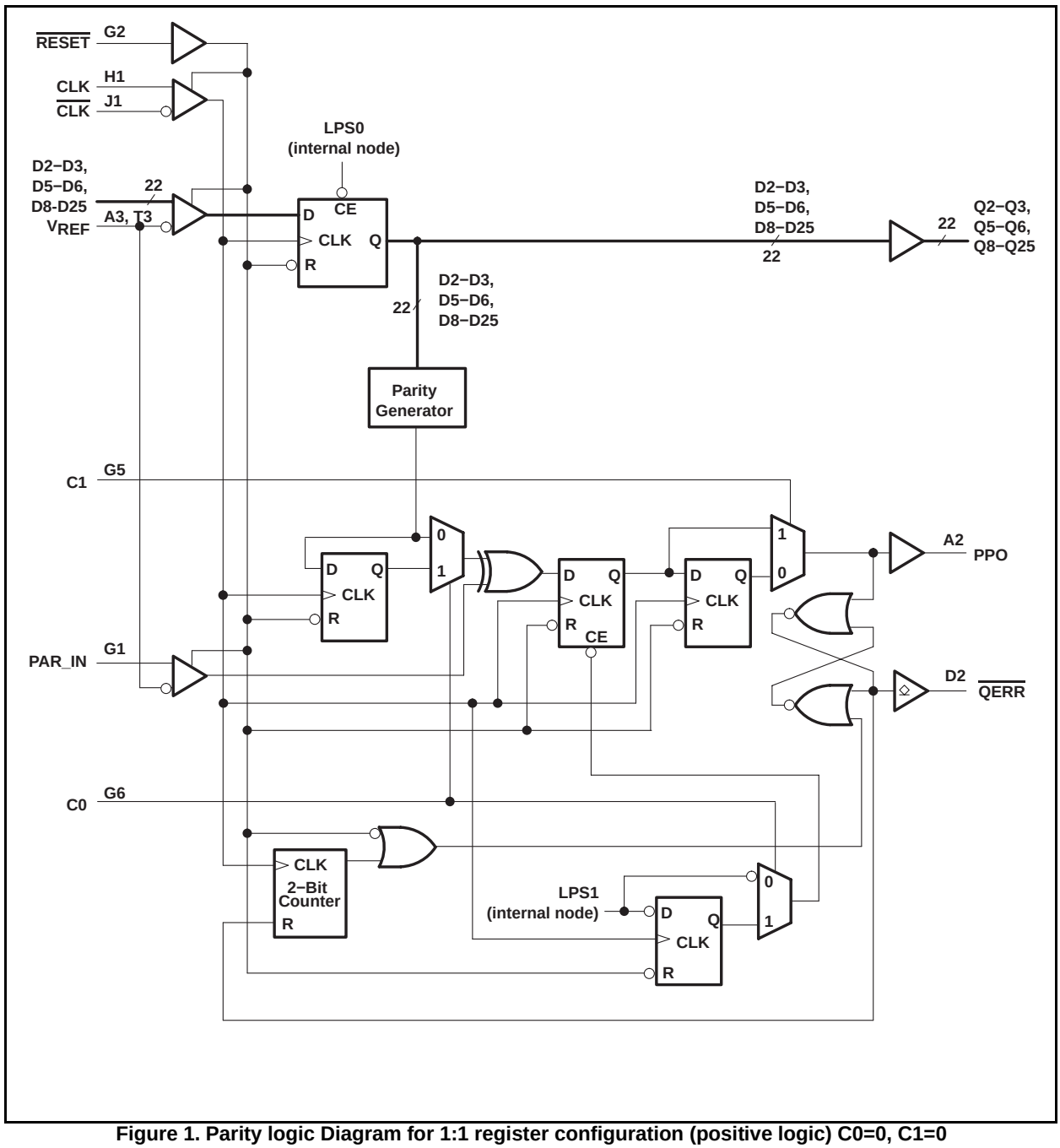


Figure 1. Parity logic Diagram for 1:1 register configuration (positive logic) C0=0, C1=0

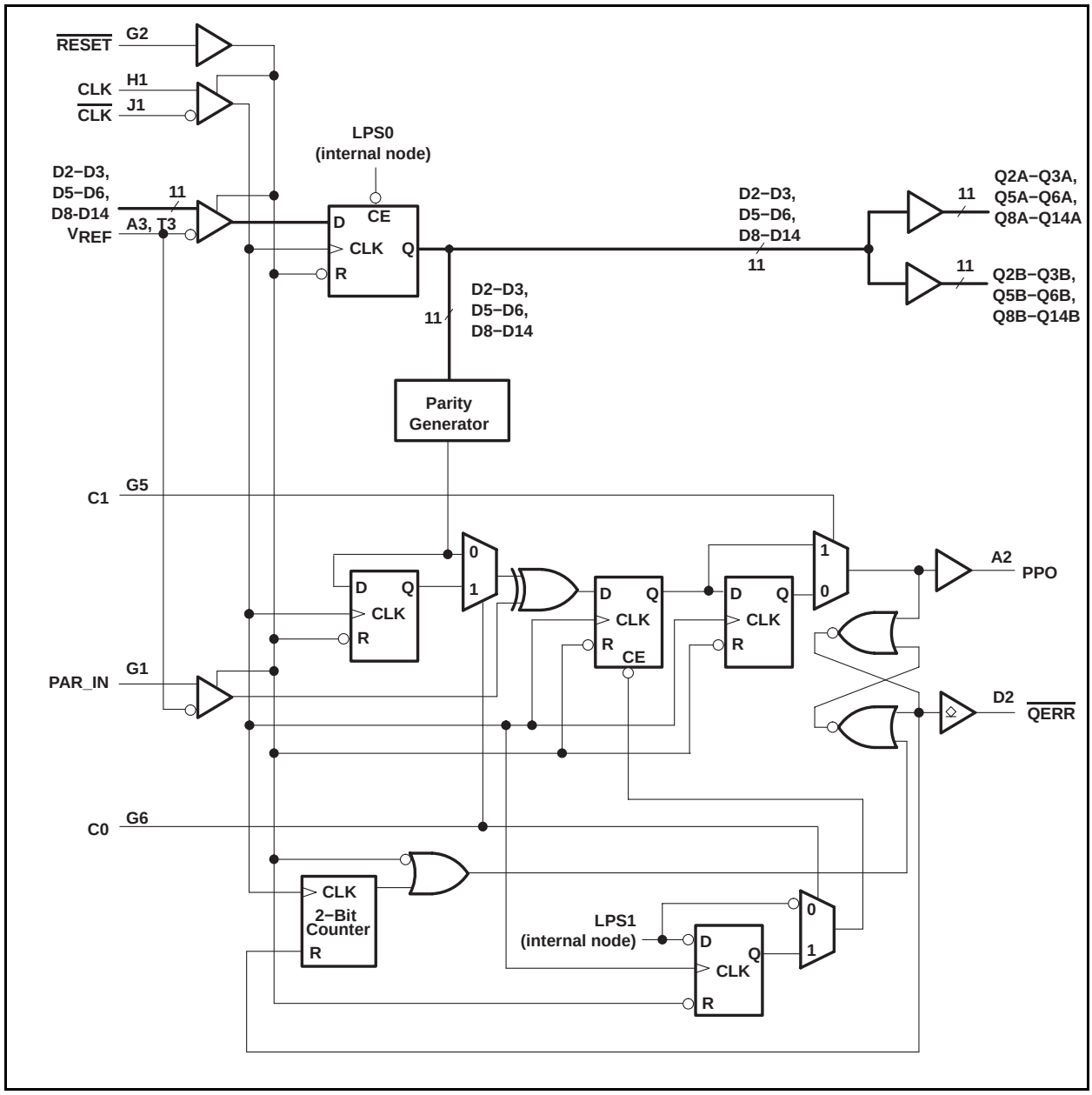


Figure 2. Parity logic Diagram for 1:2 register-A configuration (positive logic) C0=0, C1=1

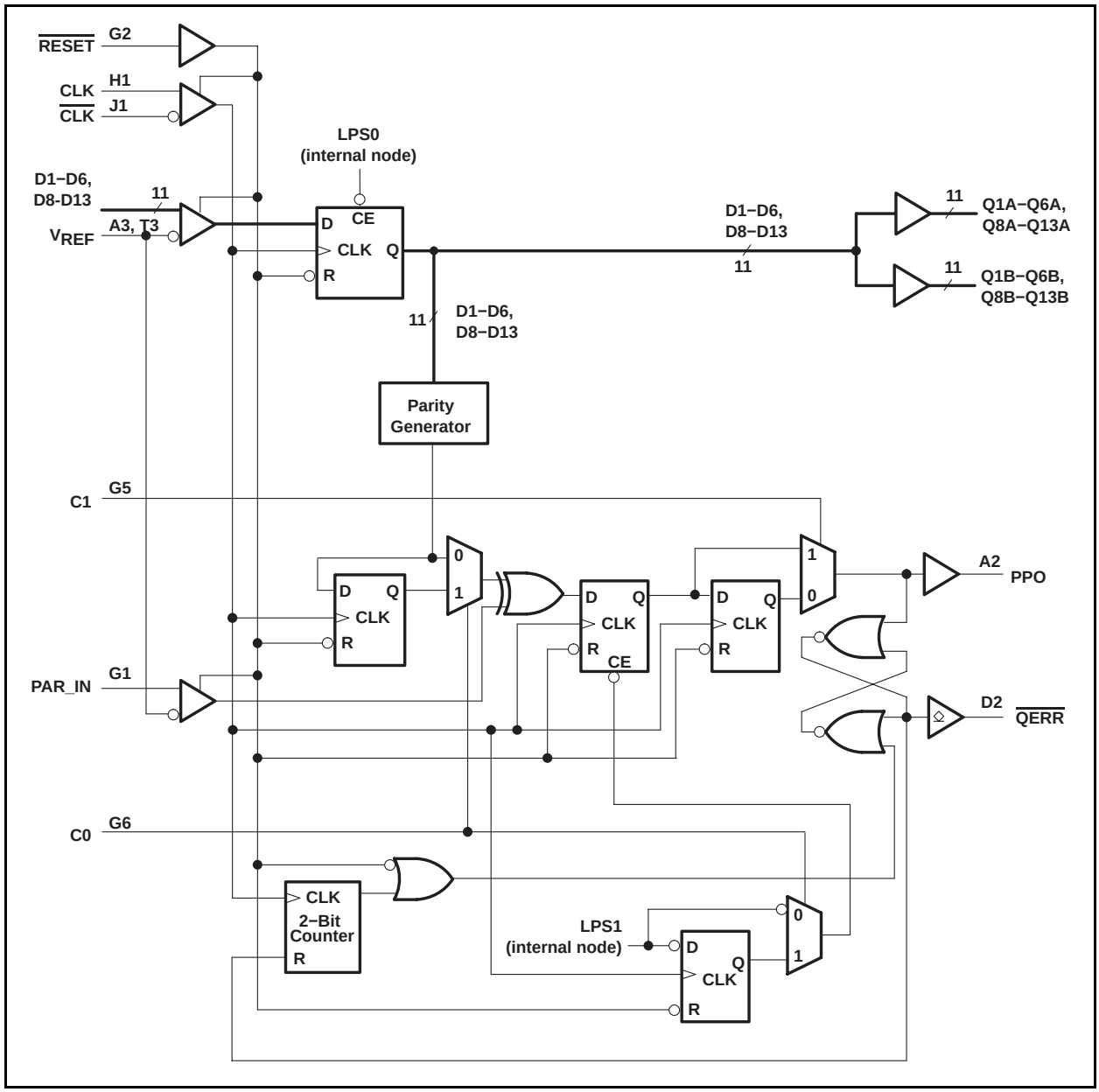


Figure 3. Parity logic Diagram for 1:2 register-B configuration (positive logic) C0=1, C1=1

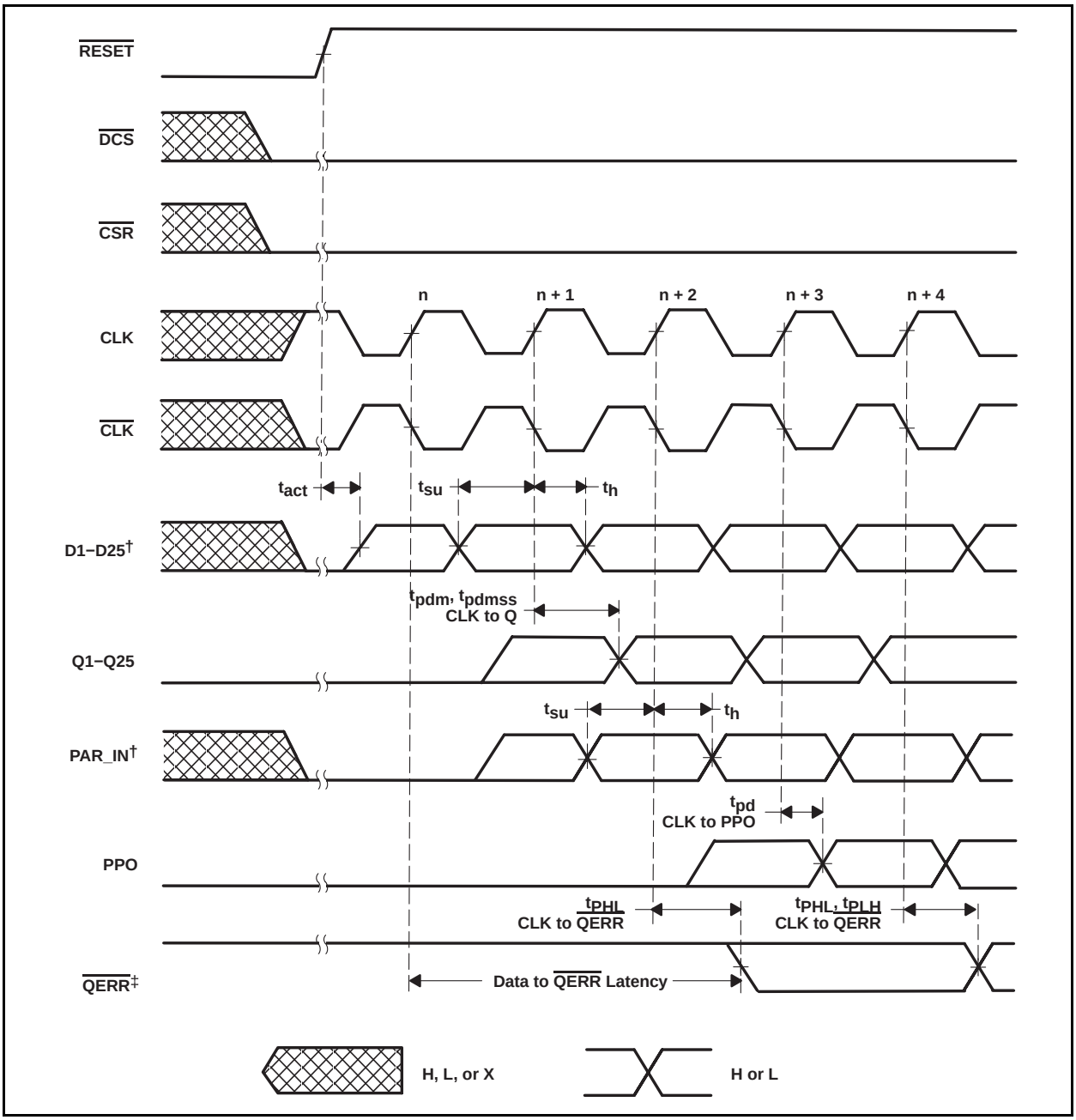


Figure 4. CY2SSTU32866 used as single device C0=0, C1=0, RST# Switchs L to H

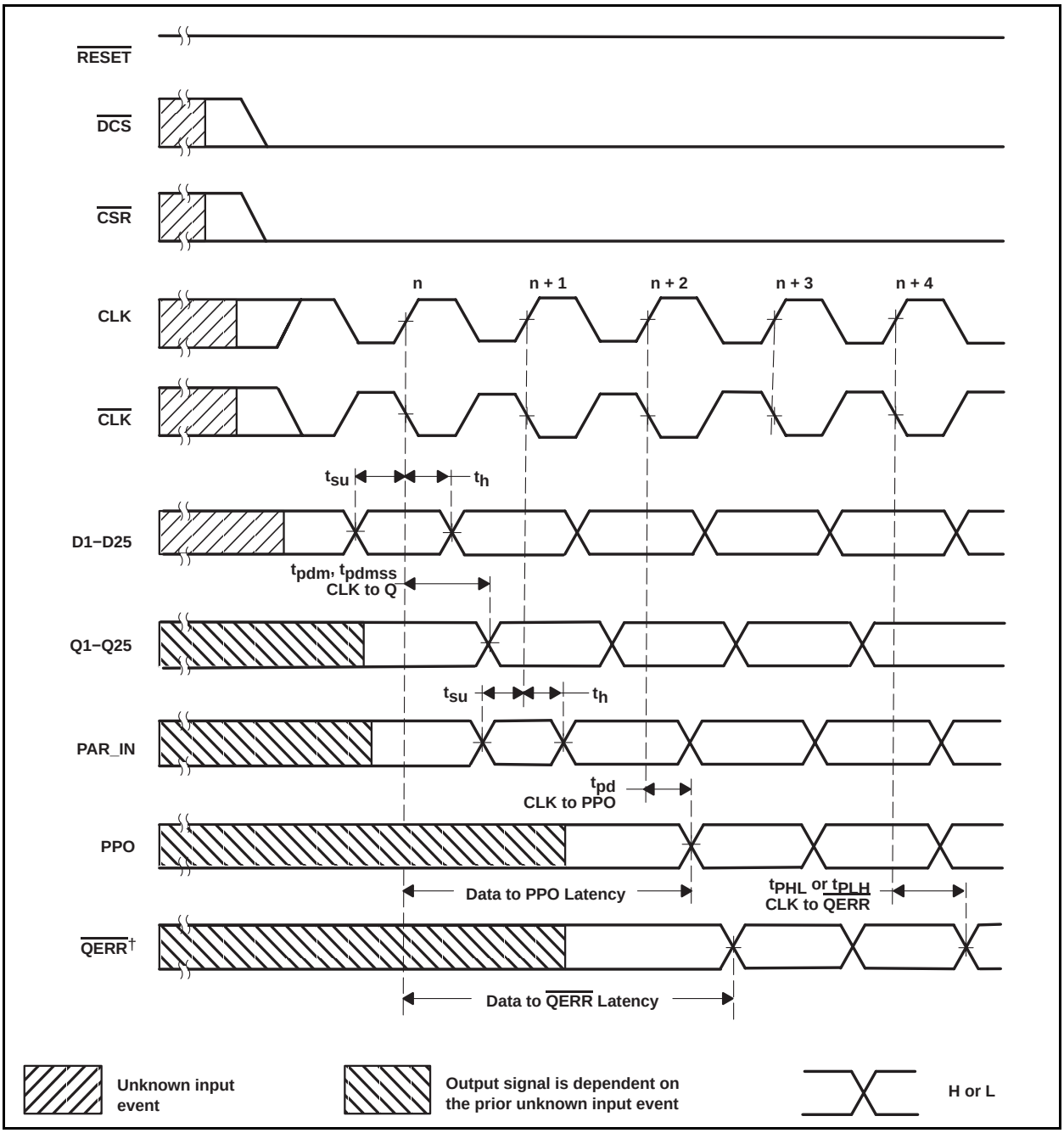


Figure 5. CY2SSTU32866 used as single device, C0=0, C1=0, RST# being held high

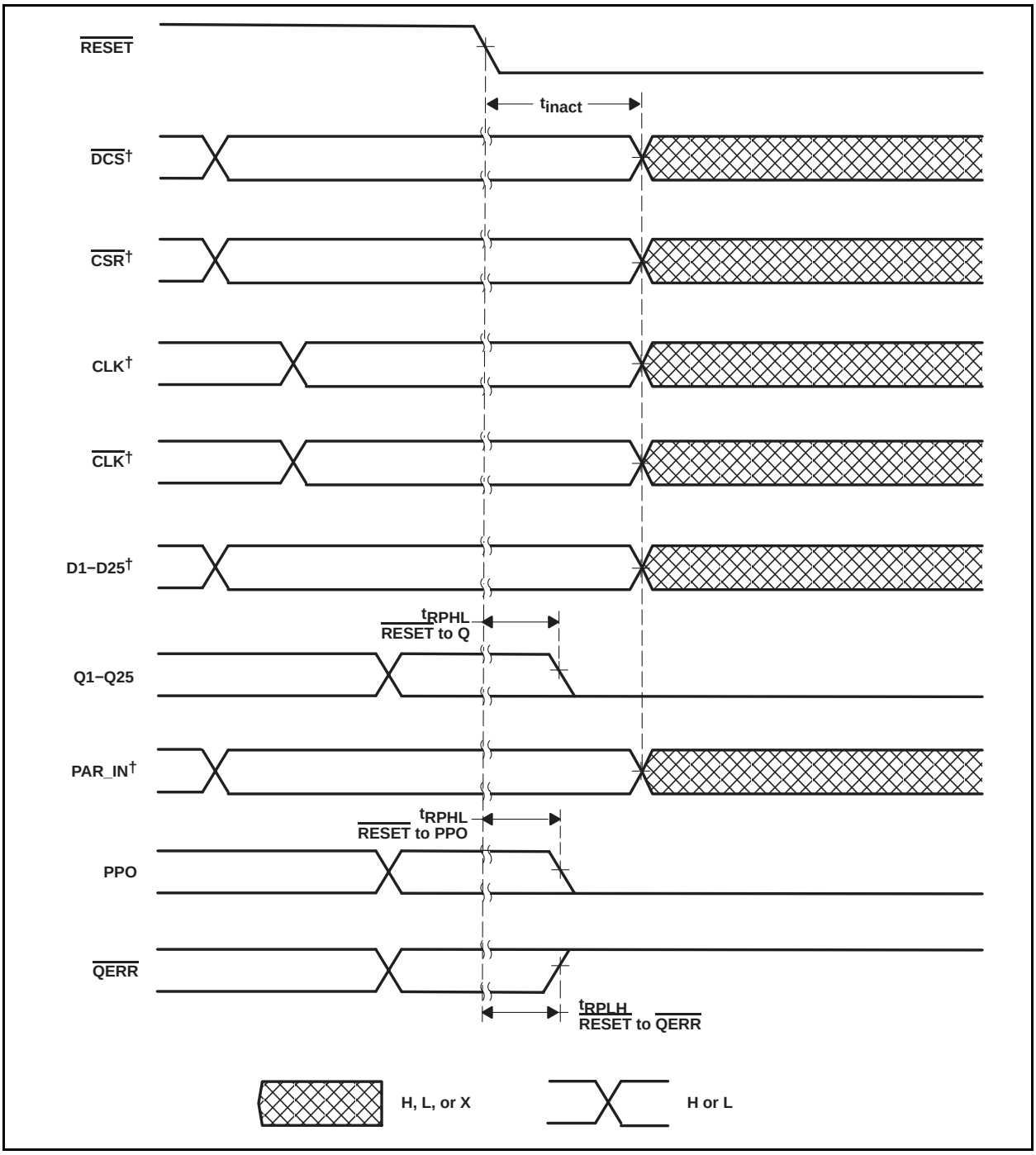


Figure 6. CY2SSTU32866 used as single device, C0=0, C1=0, RST# switchs from H to L

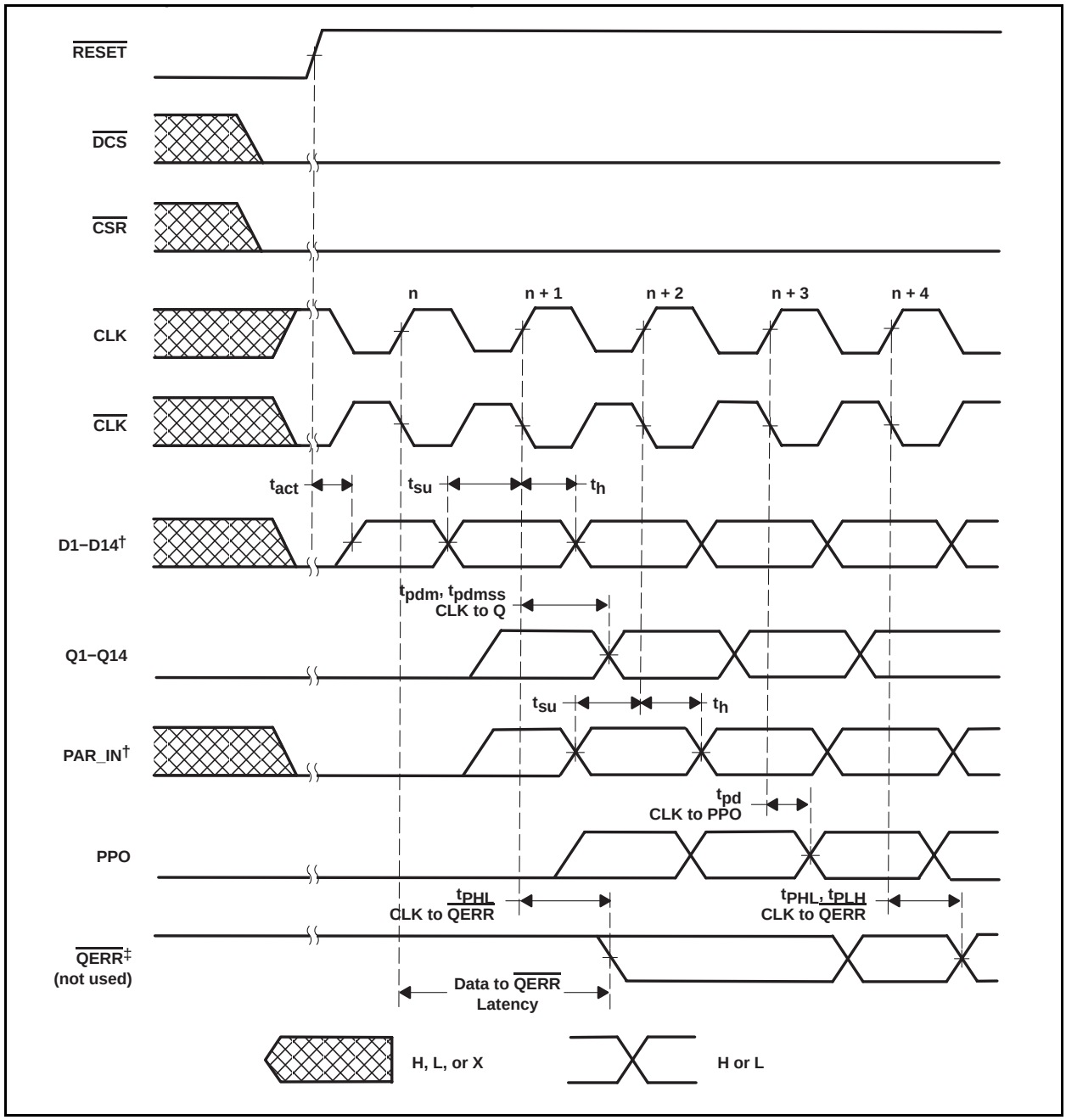


Figure 7. CY2SSTU32866 used as pair, C0=0, C1=1, RST# switches from L to H

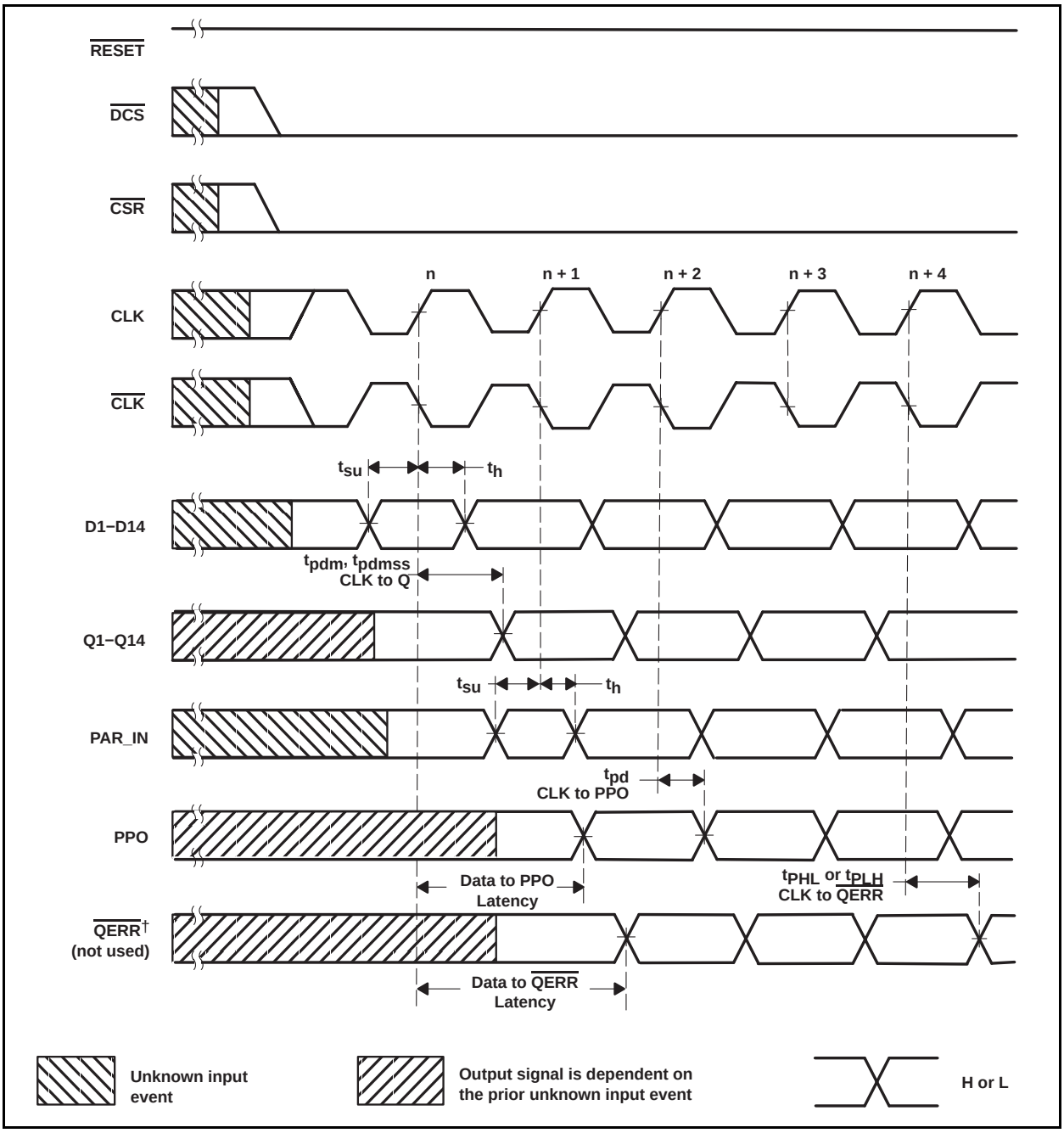


Figure 8. CY2SSTU32866 used as pair, C0=0, C1=1, RST# being held high

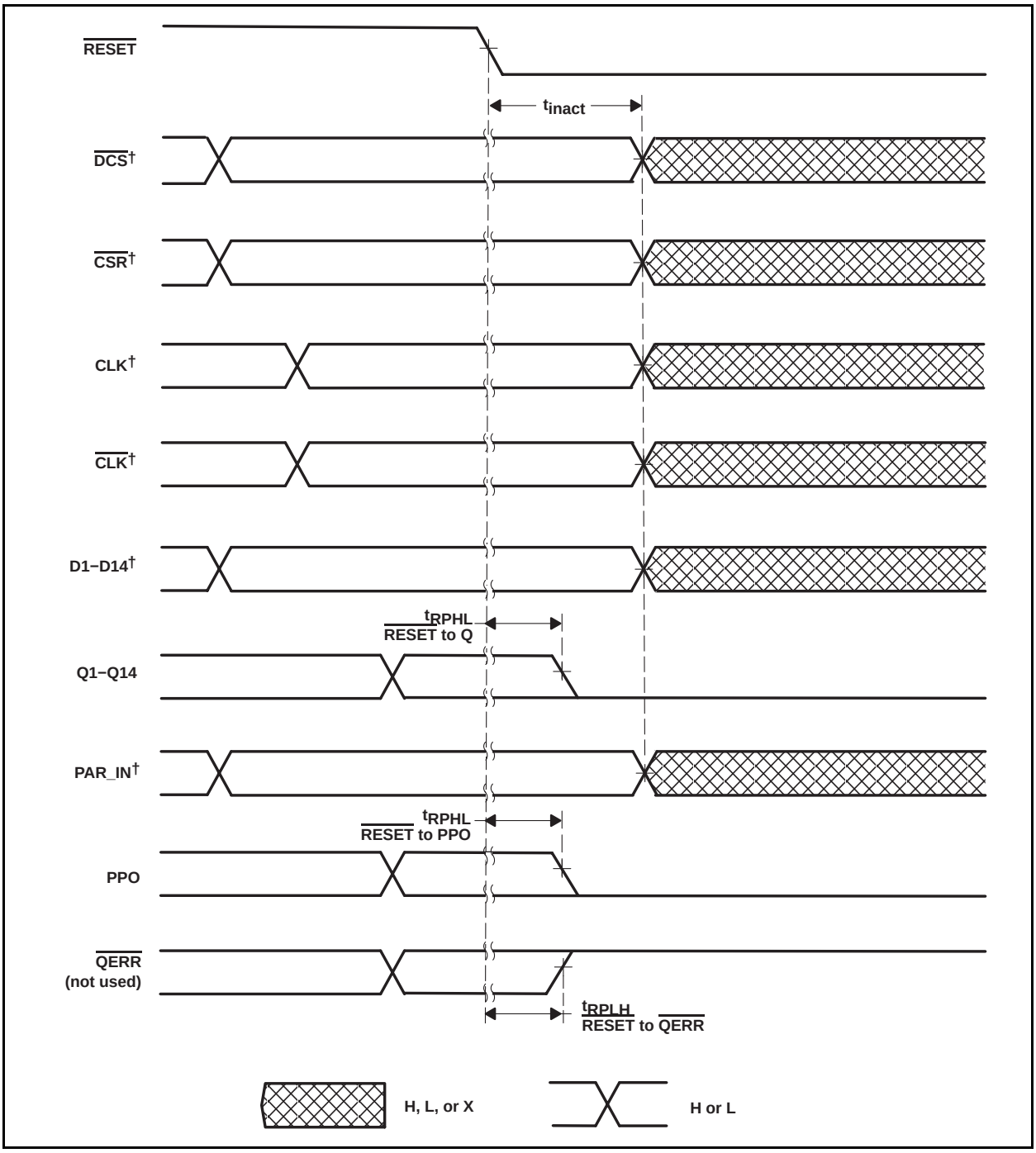


Figure 9. CY2SSTU32866 used as pair, C0=0, C1=1, RST# switches from H to L

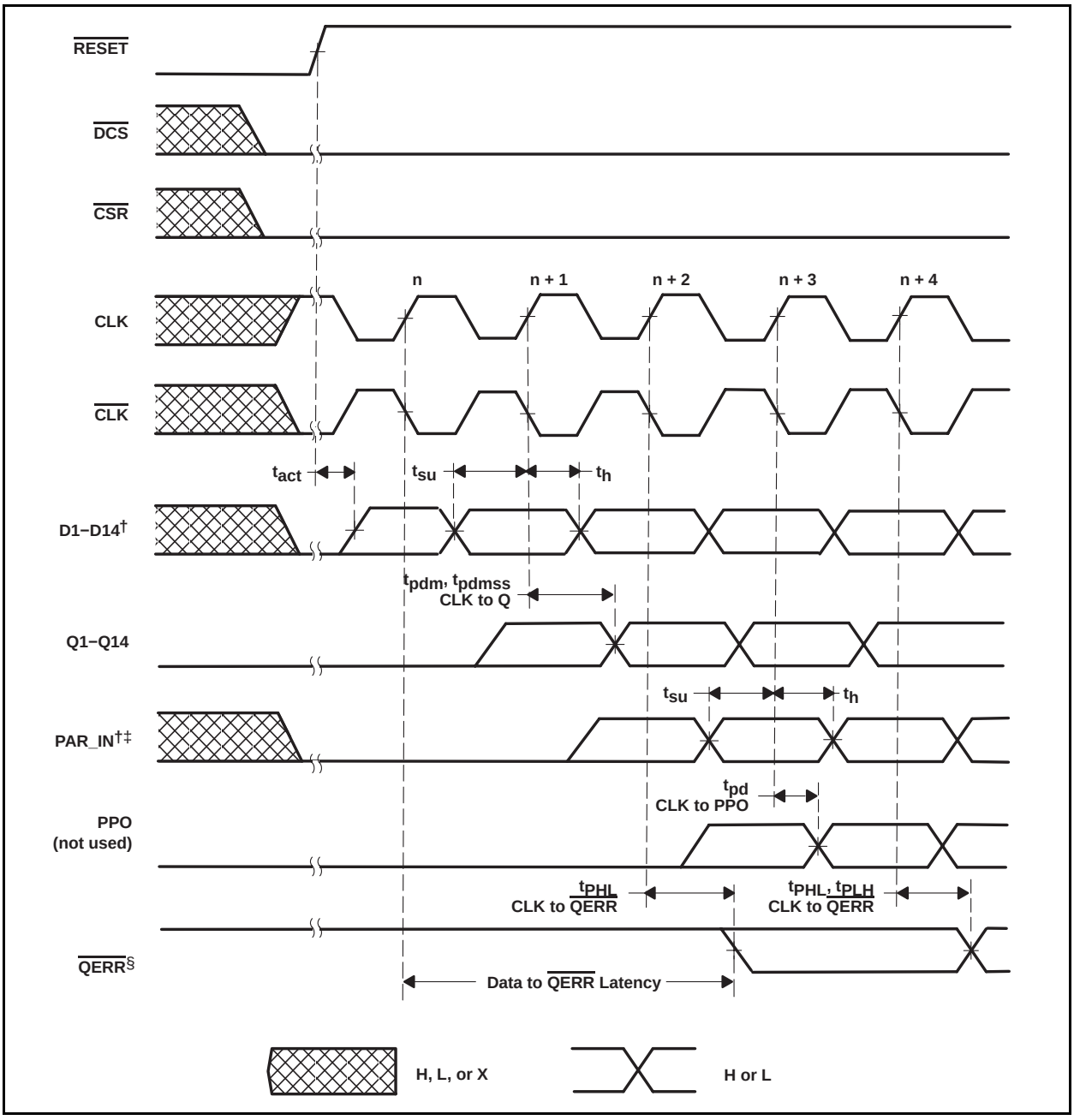


Figure 10. CY2SSTU32866 used as pair, C0=1, C1=1, RST# switches from L to H

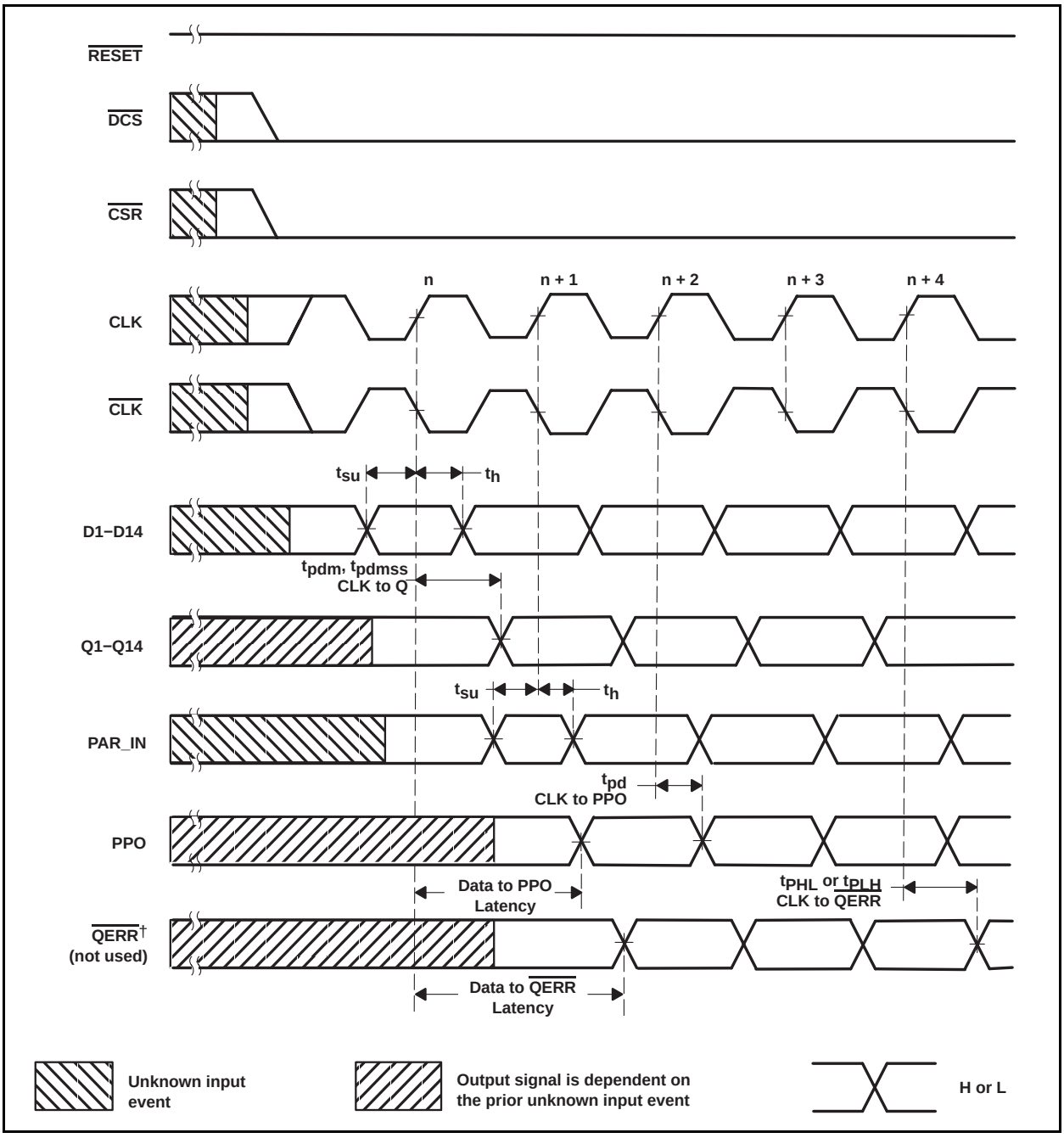


Figure 11. CY2SSTU32866 used as pair, C0=1, C1=1, RST# being held high

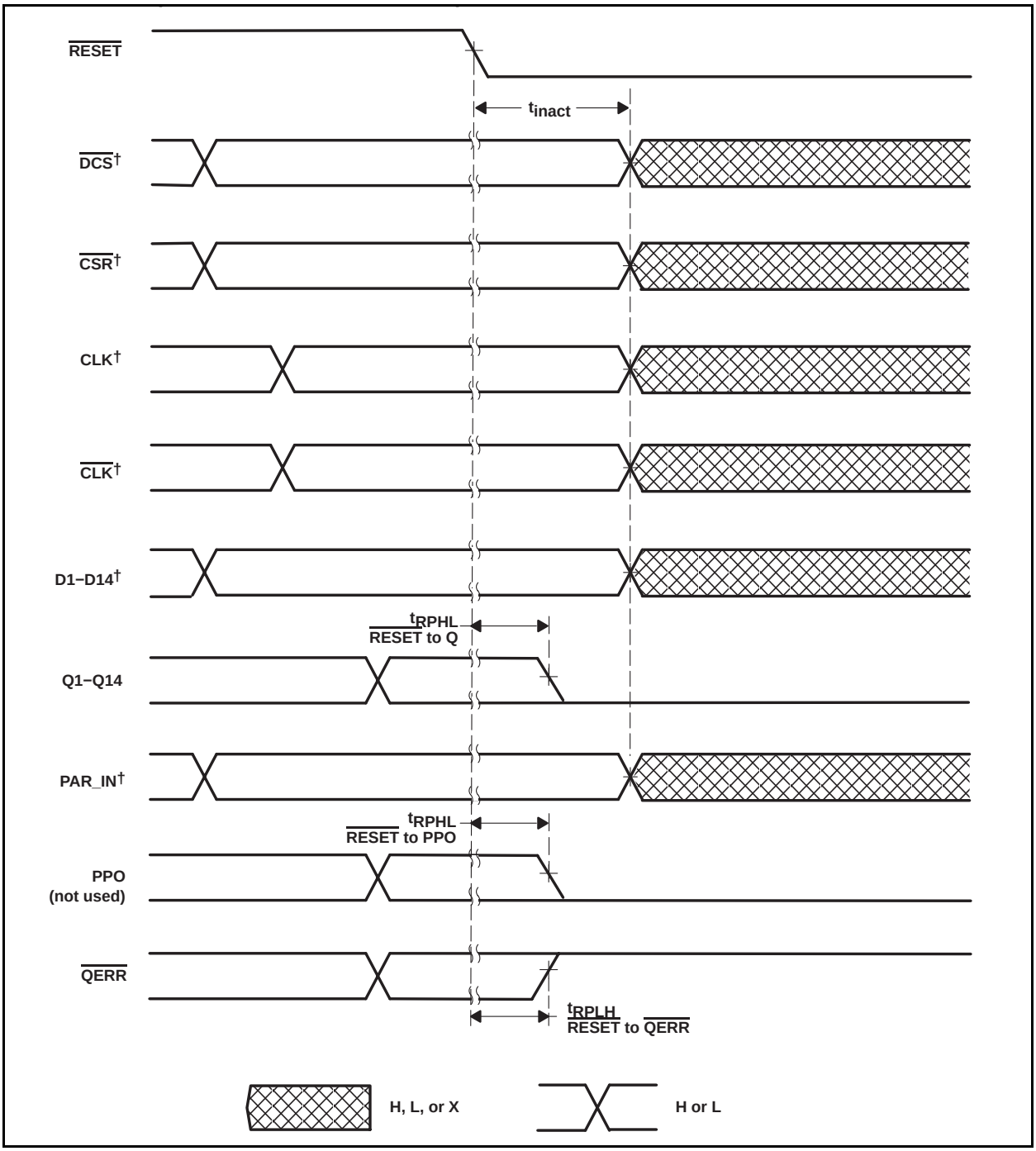


Figure 12. CY2SSTU32866 used as pair, C0=1, C1=1, RST# switches from H to L

Absolute Maximum Conditions [1]

Parameter	Description	Condition	Min.	Max.	Unit
T_S	Storage Temperature		–65	150	C
V_{CC}	Supply Voltage Range		–0.5	2.5	V
V_{IN}	Input Voltage Range[2, 3]		–0.5	V_{DD} + 0.5	V
V_{OUT}	Output Voltage Range[2, 3]		–0.5	V_{DD} + 0.5	V
I_{IK}	Input Clamp Current	V_O < 0 or V_O > V_{DD}	–50	50	mA
I_{OK}	Output Clamp Current	V_O < 0 or V_O > V_{DD}	–50	50	mA
I_O	Continuous Output Current	V_O = 0 to V_{DD}	–50	50	mA
I_{CCC}	Continuous Current through V_{DD}/GND		–100	100	mA

DC Electrical Specifications

Parameter	Description	Conditions	Min.	Max.	Unit
T_A (Com.)	Ambient Operating Temp		0	70	C
V_{DD}	Operating Voltage		1.7	1.9	V
V_{REF}	Voltage Reference		0.49*V_{DD}	0.51*V_{DD}	V
V_{TT}	Terminating Voltage		V_{REF}–40mV	V_{REF}+40mV	V
V_I	Input Voltage		0	V_{DD}	V
I_I	Input Current	V_I = V_{DD} or GND	–5	5	µA
V_{IL}	AC Input Low Voltage	Data, CSR#, and PAR_IN inputs	–	V_{REF} – 250mV	V
	DC Input Low Voltage		–	V_{REF} – 125mV	V
V_{IH}	AC Input High Voltage		V_{REF} + 250mV	–	V
	DC Input High Voltage		V_{REF} + 125mV	–	V
V_{IL}	Input Low Voltage	RESET#, Cn		0.35 X V_{DD}	V
V_{IH}	Input High Voltage		0.65 X V_{DD}		V
V_{ICR}	Input Low Voltage	CK, CK#	0.675	1.125	V
V_{ID}	Input Differential Voltage		600	–	mV
V_{OL}	Output Low Voltage	I_{OL} = 100 µA, V_{CC} = 1.7V to 1.9V	–	0.2	V
		I_{OL} = 6 mA, V_{CC} = 1.7V	–	0.5	V
V_{OH}	Output High Voltage	I_{OH} = –100 µA, V_{CC} = 1.7V to 1.9V	V_{DD} – 0.2	–	V
		I_{OH} = –6 mA, V_{CC} = 1.7V	1.2	–	V
I_{OH}	Output High Current		–	–8	mA
I_{OL}	Output Low Current		–	8	mA
I_{DD}	Static Standby Power Supply Current	RESET# = G_{ND}, IO = 0, V_{DD} = 1.9V		100	µA
	Static Operating Power Supply Current	RESET# = V_{DD}, V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$, IO = 0, V_{DD} = 1.9V		40	mA

Notes:
1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. This value is limited to 2.5V (max.)

DC Electrical Specifications (continued)

Parameter	Description	Conditions	Min.	Max.	Unit
I_{DDD}	Power Supply Current Dynamic Operating Clock Only	RESET# = V_{DD}, V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$, CK, CK# switching 50% duty cycle, V_{DD} = 1.8V	28 (typical)		µA/MHz
	Dynamic Operating per each Data Input	RESET# = V_{DD}, V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$, CK, CK# switching 50% duty cycle, V_{DD} = 1.8V, 1 IO switching 1:1 configuration	18 (typical)		µA/MHz
		RESET# = V_{DD}, V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$, CK, CK# switching 50% duty cycle, V_{DD} = 1.8V, 1 IO switching 1:2 configuration	36 (typical)		µA/MHz
	Low Power Active Mode, CLK only	RESET# = V_{DD}, V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$, CK, CK# switching 50% duty cycle, V_{DD} = 1.8V, CS Enabled	27 (typical)		µA/MHz
	Low Power Active Mode per each Data Input	RESET# = V_{DD}, V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$, CK, CK# switching 50% duty cycle, V_{DD} = 1.8V, 1 IO switching 1:1 configuration, CS Enabled	2 (typical)		µA/MHz
		RESET# = V_{DD}, V_I = $V_{IH(AC)}$ or $V_{IL(AC)}$, CK, CK# switching 50% duty cycle, V_{DD} = 1.8V, 1 IO switching 1:2 configuration; CS Enabled	2 (typical)		µA/MHz
C_{IN}	Ci (Data and CSR#)	V_I = V_{REF} ± 250mV	2.5	3.5	pF
	Ci (CK and CK#)	V_{IX} = 0.9V, V_{ID} = 600 mV	2	3	pF
	Ci (RESET#)	V_I = V_{DD} or GND	2.5		pF

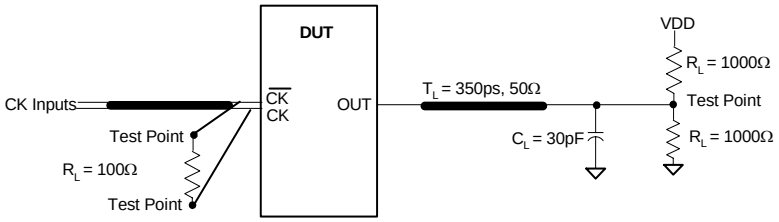
AC Timing Specifications

Parameter	Description	Conditions	Min.	Max.	Unit
F_{CLK}	Clock Frequency		–	500	MHz
T_W	Pulse Duration	CK, CK# H or L	1	–	ns
T_{ACT}[4]	Differential Input Active time		–	10	ns
T_{INACT}[5]	Differential Input Inactive time		–	15	ns
T_{SU}	Set-up Time	DSR# before crossing CK,CK#, CSR = H	0.7	–	ns
		CSR# before crossing CK,CK#, DCS = H	0.7	–	ns
		DCS# before crossing CK,CK#, CSR = L	0.5	–	ns
		DODT, DCKE and data before crossing CK,CK#, CK going HIGH	0.5	–	ns
		PAR_IN after crossing CK,CK#	0.5		ns
T_H	Hold Time	DCS#, DODT, DCKE and data after crossing CK, CK#	0.5	–	ns
		PAR_IN after crossing CK, CK#	0.5	–	ns
T_{PDM}	Propagation Delay single bit switching	From CK, CK# crossing to Q		1.86	ns
T_{PDMSS}	Propagation Delay simultaneous switching	From CK, CK# to Q - simultaneous switching		1.87	ns
T_{PD}	Propagation Delay from Low to High	From CK, CK# crossing to PPO	2.15 (typical)		ns

Notes:
4. Data and V_{REF} inputs must be low a minimum time of T_{ACT} max, after RESET# is taken HIGH.
5. Data, V_{REF} and clock inputs must be held at valid levels (not floating) a minimum time of T_{INACT} max after RESET# is taken LOW.

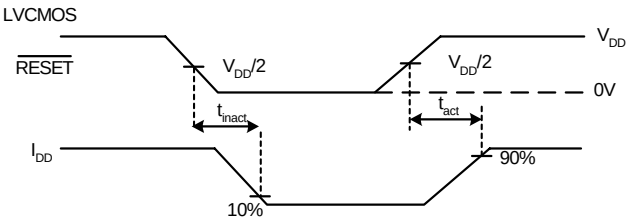
AC Timing Specifications (continued)

Parameter	Description	Conditions	Min.	Max.	Unit
T_{PLH}	Propagation Delay from Low to High	From CK, CK# crossing to QERR#	1.2	3	ns
T_{PHL}	Propagation Delay from Low to High		1	2.4	ns
T_{rPLH}	Propagation Delay from Low to High	RESET# LOW to QERR# HIGH	3 (typical)		ns
T_{rPHL}	Propagation Delay from High to Low	RESET# LOW to Q, PPO LOW		3	ns
S_{LR}	Slew Rate Rising	dv/dt_r (20 to 80%)	1	4	V/ns
	Slew Rate Falling	dv/dt_f (20 to 80%)	1	4	V/ns
dv/dt Δ	Delta between Rising/Falling Rates		–	1	V/ns



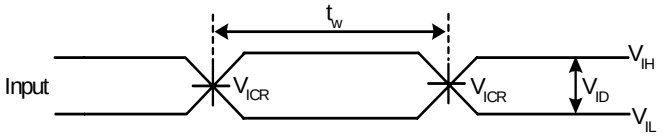
C_L includes probe and jig capacitance

Figure 13. Test Load for Timing Measurements #1



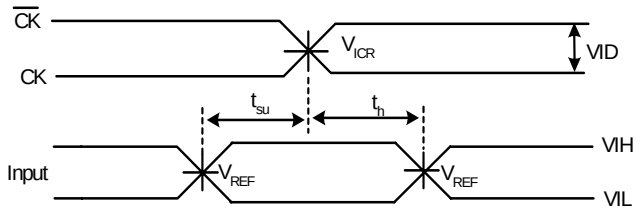
I_{DD} tested with clock and data inputs held at V_{DD} or GND, and I_O = 0mA

Figure 14. Active and Inactive Times



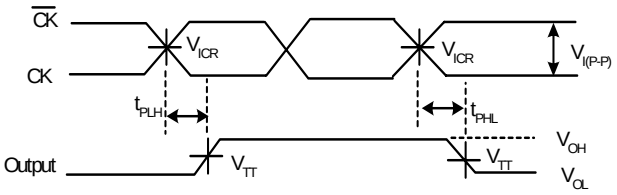
V_{ID} = 600mV
V_{IH} = V_{REF} + 250mV (AC Voltage levels) for differential inputs. V_{IH} = V_{DD} for LVCMOS inputs.
V_{IL} = V_{REF} - 250mV (AC voltage levels) for differential inputs. V_{IL} = V_{DD} for LVCMOS inputs

Figure 15. Pulse Duration



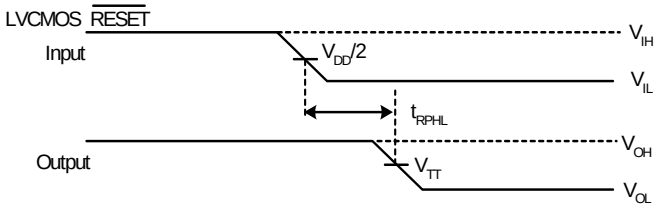
V_{ID} = 600mV
V_{REF} = V_{DD}/2
V_{IH} = V_{REF} + 250mV (AC Voltage levels) for differential inputs. V_{IH} = V_{DD} for LVCMOS inputs.
V_{IL} = V_{REF} - 250mV (AC voltage levels) for differential inputs. V_{IL} = V_{DD} for LVCMOS inputs

Figure 16. Set-up and Hold Times



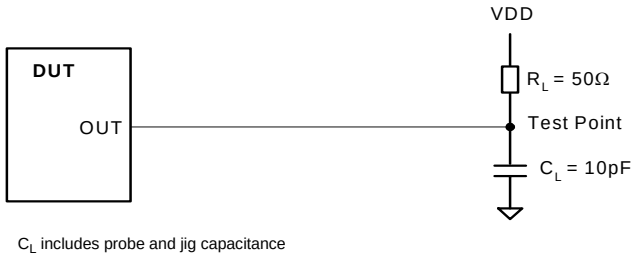
t_{PLH} and t_{PHL} are the same as t_{PD}

Figure 17. Propagation Delay



t_{PLH} and t_{PHL} are the same as t_{PD}
V_{IH} = V_{REF} + 250mV (AC Voltage levels) for differential inputs. V_{IH} = V_{DD} for LVCMOS inputs.
V_{IL} = V_{REF} - 250mV (AC voltage levels) for differential inputs. V_{IL} = V_{DD} for LVCMOS inputs

Figure 18. Propagation Delay after RESET#



C_L includes probe and jig capacitance

Figure 19. Load Circuit - High to Low Slew Measurement

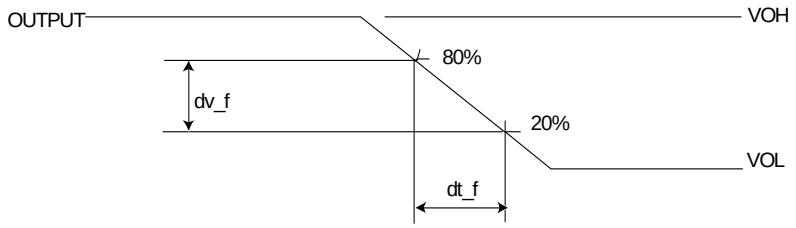
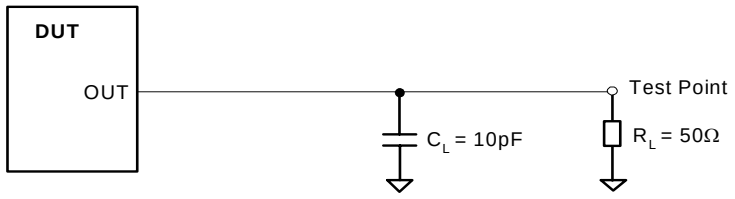


Figure 20. High to Low Slew Rate Measurement



C_L includes probe and jig capacitance

Figure 21. Load Circuit, Low to High slew measurement

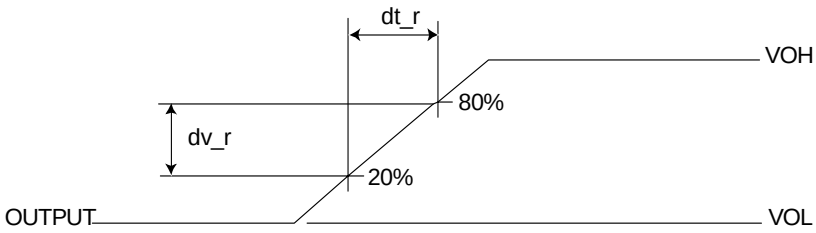


Figure 22. Low to High Slew Rate Measurement

C_L includes probe and jig capacitance

Figure 23. Load Circuit - High to Low Slew Rate Measurement

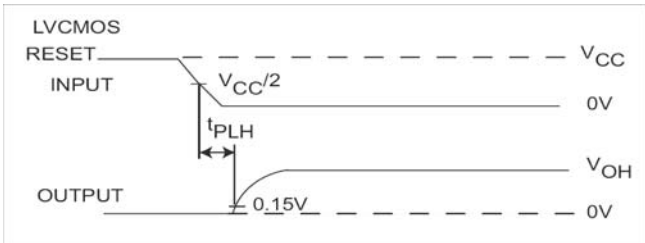


Figure 24. Open drain output - Low to High transition with respect to reset inputs

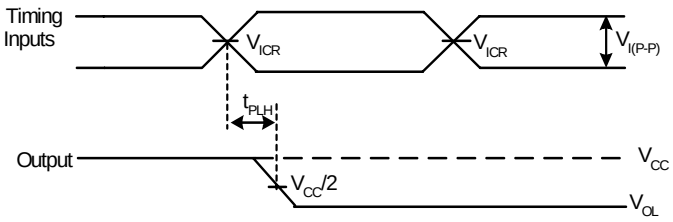


Figure 25. Open drain output - High to Low transition with respect to clock inputs

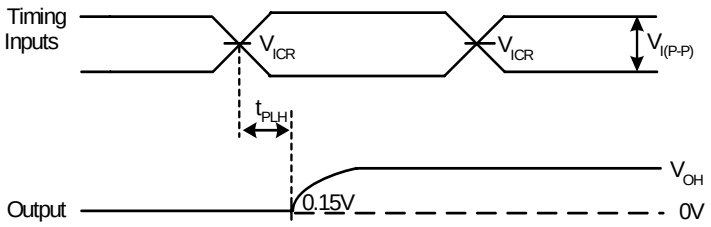
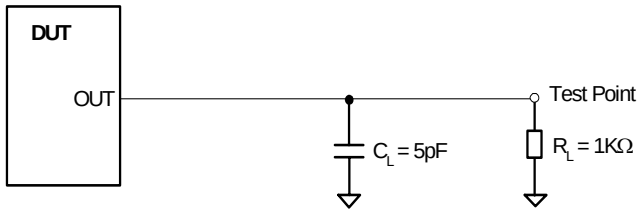
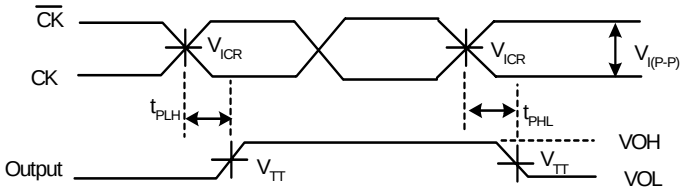


Figure 26. Open drain output - High to Low transition with respect to clock inputs



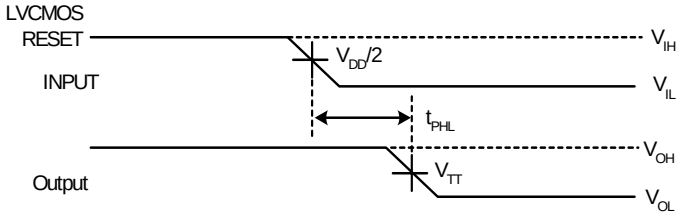
C_L includes probe and jig capacitance

Figure 27. Partial-parity-out Load Circuit



$V_{TT} = V_{DD}/2$
t_{PLH} and t_{PHL} are the same as t_{PD}
$V_{I(P-P)}$ = 600mV

Figure 28. Partial-parity-out ; propagation delay times with respect to clock inputs



$V_{TT} = V_{DD}/2$
t_{PLH} and t_{PHL} are the same as t_{PD}
$V_{IH} = V_{REF}$ + 250mV (AC Voltage levels) for differential inputs. $V_{IH} = V_{DD}$ for LVCMOS inputs.
$V_{IL} = V_{REF}$ - 250mV (AC voltage levels) for differential inputs. $V_{IL} = V_{DD}$ for LVCMOS inputs

Figure 29. Partial-parity-out ; propagation delay times with respect to clock inputs

Ordering Information

Part Number	Package Type	Product Flow
Lead Free		
CY2SSTU32866BFXC	96-pin FBGA	Commercial, 0° to 70°C
CY2SSTU32866BFXCT	96-pin FBGA – Tape and Reel	Commercial, 0° to 70°C

Package Drawing and Dimensions

96-Ball FBGA (5.5 x 13.5 x 1.2 MM) BF96A