CY2048WAF

Flash Programmable Capacitor Tuning Array Die for Crystal Oscillator(XO)

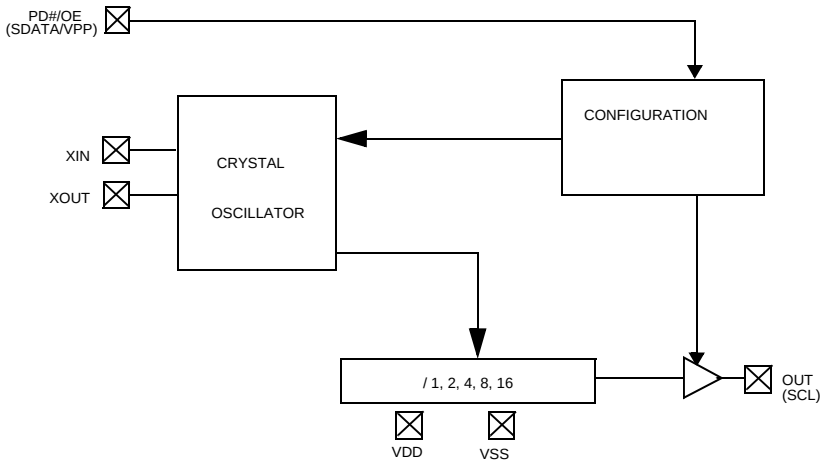
Features

- Flash-programmable capacitor tuning array for low ppm initial frequency clock output
- Low clock output jitter
  - — 4 ps typ. RMS period jitter
  - — ±30 ps typ. peak-to-peak period jitter
- Flash-programmable dividers
- Two-pin programming interface
- On-chip oscillator runs from 10–48-MHz crystal
- Five selectable post-divide options, using reference oscillator output
- Programmable asynchronous or synchronous OE and PWR_DWN modes
- 2.7V to 3.6V operation
- Controlled rise and fall times and output slew rate

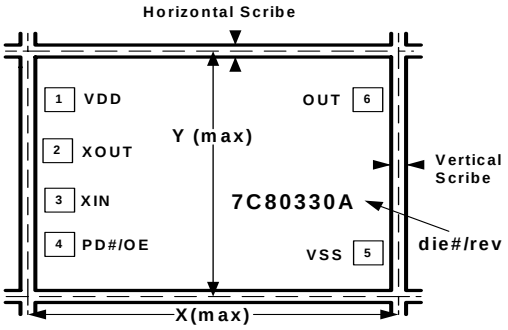
Benefits

- Enables fine-tuning of output clock frequency by adjusting C_{Load} of the crystal
- Allows multiple programming opportunities to correct errors, and control excess inventory
- Enables programming of output frequency after packaging
- PPM clock output error can be adjusted in package
- Provides flexibility in output configurations and testing
- Enables low-power operation or output enable function
- Provides flexibility for system applications through selectable instantaneous or synchronous change in outputs
- Enables encapsulation in small-size, surface-mount packages

Block Diagram



Die Pad Description



Notes:

X(max): 980 µm, Y(max): 988 µm

Scribe: X = 70 µm, Y = 86 µm

Bond pad opening: 85 µm x 85 µm

Pad pitch: 175 µm (min.)

Wafer thickness: 11 mils (Typ.)

Die Pad Summary (Pad coordinates are referenced from the center of the die (X = 0, Y = 0))

Name	Pad Number	Description	X coordinate (μm)	Y coordinate (μm)
VDD	1	Voltage Supply	–360.8	353.7
XOUT	2	Oscillator Drain	–360.8	134.1
XIN	3	Oscillator Gate	–360.8	–42.6
PD#/OE	4	Programmable power-down or output enable pin	–360.8	–275.9
VPP		High voltage for programming NV memory		
SDATA		Serial data pin used for programming in test mode		
OUT	6	Clock output	360.0	353.7
SCL		Serial clock for programming in test mode		
VSS	5	Ground	360.0	–354.5

Absolute Maximum Conditions

(Above which the useful life may be impaired.
For user guidelines, not tested.)

Supply Voltage (V_{DD}) .....–0.5 to +7.0V

DC Input Voltage ..... –0.5V to V_{DD} + 0.5

Output Short Circuit Current ..... ± 50 mA

Storage Temperature (Non-condensing) .... –55°C to +125°C

Junction Temperature ..... –40°C to +125°C

Data Retention @ Tj = 125°C .....> 10 years

ESD (Human Body Model) MIL-STD-883..... > 2000V

Crystal Specifications[1]

Parameter	Description	Comments	Min.	Typ.	Max.	Unit
F_{NOM}	Nominal crystal frequency	Fundamental mode, AT cut	10	–	48	MHz
R_1	Equivalent series resistance (ESR)	Fundamental mode	–	–	40	Ω
R_3/R_1	Ratio of third overtone mode ESR to fundamental mode ESR	Ratio used because typical R_1 values are much less than the maximum spec	4.5	–	–	–
C_0	Crystal shunt capacitance		–	–	5	pF
C_1	Crystal motional capacitance		2	–	–	fF

Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Unit
V_{DD}	Operating Voltage	2.7	–	3.6	V
T_J	Junction Temperature	–40	–	125	°C
C_{XIN}	Capacitance XIN, all tuning caps OFF	–	10	–	pF
C_{XOUT}	Capacitance XOUT, all tuning caps OFF	–	10	–	pF
C_L	All tuning Caps OFF	4	5	6	pF
	All tuning Caps ON	9.2	10	11.4	pF
C_{OUT}	Output Load Capacitance	–	–	15	pF
t_{RAMP}	Power-up time for V_{DD} to reach minimum specified voltage (power ramps must be monotonic)	0.05	–	500	ms
T_S	Start up time, 90% V_{DD} to valid frequency on output	–	–	10	ms

DC Electrical Specifications TJ = –40 to 125°C over the operating range

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
V_{IL}	Input Low Voltage	CMOS Levels	–	–	20	%VDD
V_{IH}	Input High Voltage	CMOS Levels	80	–	–	%VDD
V_{OL}	Output Low Voltage	V_{DD} = 2.7V–3.6V, I_{OL} = 8 mA	–	–	0.4	V
V_{OH}	Output High Voltage	V_{DD} = 2.7V–3.6V, I_{OL} = –8 mA	V_{DD}–0.4	–	–	V
I_{IL}	Input Low Current	Input = V_{SS}	–	1	10	µA
I_{IH}	Input High Current	Input = V_{DD}	–	1	10	µA
I_{OZL}	Output Leakage Current	Output = V_{SS}	–	1	10	µA
I_{OZH}	Output Leakage Current	Output = V_{DD}	–	–	50	µA
I_{DD}	Power Supply Current	No Load, V_{DD} = 3.3V, 48 MHz	–	–	20	mA
I_{PD}	Power Down Current	PD# = 0V	–	–	25	µA
R_{UP}	Input Pull-up resistor	$V_{IN} = V_{SS}$	1	3	6	MΩ
		V_{IN}> = 0.8V_{DD}	80	120	150	kΩ
R_{DN}	Output Pull-down resistor	V_{IN} = 0.5V_{DD}	500	900	1500	kΩ
C_{IN}	Input Pin Capacitance	PD#/OE pin	–	–	7	pF
R_F	Crystal Feedback R	XIN = 0	300	–	800	kΩ

Note:
1. Not 100% tested.

AC Electrical Specifications[1] over the operating range, except as noted

Parameter[1]	Description	Condition	Min.	Typ.	Max.	Unit
F_{OUT}	Output Frequency		0.625	–	48	MHz
DC	Output Duty Cycle	XTAL Buffered or Divided	45	50	55	%
T_R	Rise Time	Output Clock Rise Time, Measured from 20% to 80% of V_{DD}, C_{OUT} = 15 pF.			2.5	ns
T_F	Fall Time	Output Clock Fall Time, Measured from 80% to 20% of V_{DD}, C_{OUT} = 15 pF.			2.5	ns
t_{PJ1}	RMS Period Jitter	XIN = 10–48 MHz. Measured at $V_{DD}/2$	–	4	15	ps
t_{PJ2}[2]	Peak-to-peak Period Jitter	XIN = 10–48 MHz. Measured at $V_{DD}/2$	–	30	80	ps
DL	Crystal drive level	48-MHz crystal, C_L = 7 pF, C_0 = 2 pF, R1 = 10 Ohms, Temp. = 25°C, V_{DD} = 3.6V	350–400			µW
–R	Negative Resistance	Measured at 48 MHz, C_L = 10 pF, C_0 = 5 pF	–	–	–150	Ω
F_{DRIFT}	Output Frequency Drift	3.0V ± 10%, 3.3V ± 10% for Temp. = 25°C	–2	–	2	ppm

Phase Noise, Temp = 25°C, V_{DD} = 3.3V, F_{NOM} = 10MHz, X_{CAP} = 7F (Hex)

Offset	dBc/Hz (Typ)
10 Hz	–90
100 Hz	–115
1 kHz	–130
10 kHz	–140
100 kHz	–140
1 MHz	–140

Crystal Oscillator Tuning Capacitor Values

Capacitor Bit	Capacitance (pF) per Side
C_7	5.000
C_6	2.500
C_5	1.250
C_4	0.625
C_3	0.313
C_2	0.156
C_1	0.078
C_0	0.039

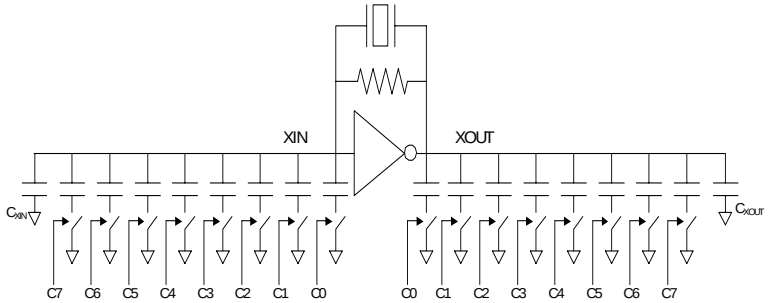


Figure 1. Programmable Load Capacitance

Notes:
2. T_{PJ2} measured using DTS-2075, # of events set to 10, 000.

Timing Parameters over the operating range

Parameter	Description	Min.	Max.	Unit
$T_{STP,SYNC}$	Time from falling edge on PD# to stopped output, synchronous mode, T=1/F_{out}		1.5T + 350	ns
$T_{STP,ASYNC}$	Time from falling edge on PD# to stopped output, asynchronous mode		350	ns
$T_{PU,SYNC}$	Time from rising edge on PD# to output at valid frequency, synchronous mode, T = 1/F_{out}		3	ms
$T_{PU,ASYNC}$	Time from rising edge on PD# to output at valid frequency, asynchronous mode		3	ms
$T_{PZX,SYNC}$	Time from rising edge on OE to running output, synchronous mode, T=1/F_{out}		1.5T + 350	ns
$T_{PZX,ASYNC}$	Time from rising edge on OE to running output, asynchronous mode		350	ns
$T_{PXZ,SYNC}$	Time from falling edge on OE to high impedance output, synchronous mode, T = 1/F_{out}		1.5T + 350	ns
$T_{PXZ,ASYNC}$	Time from falling edge on OE to high impedance output, asynchronous mode		350	ns

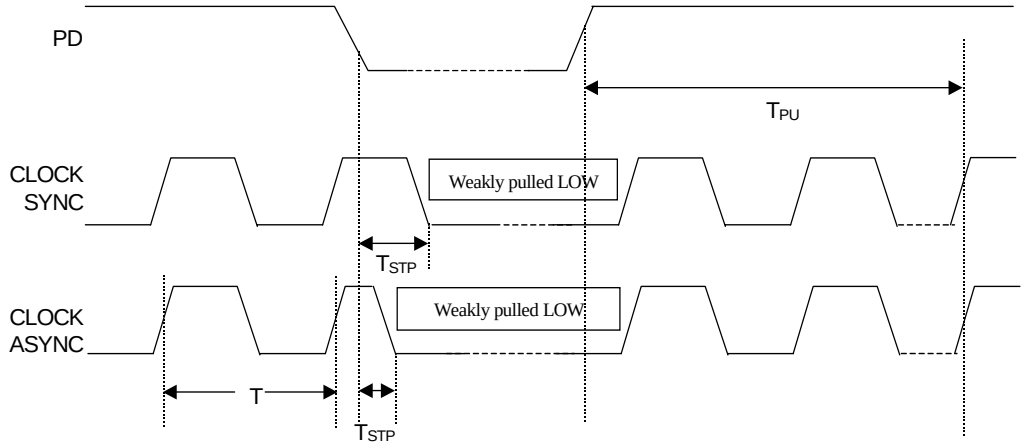


Figure 2. Power-down Timing

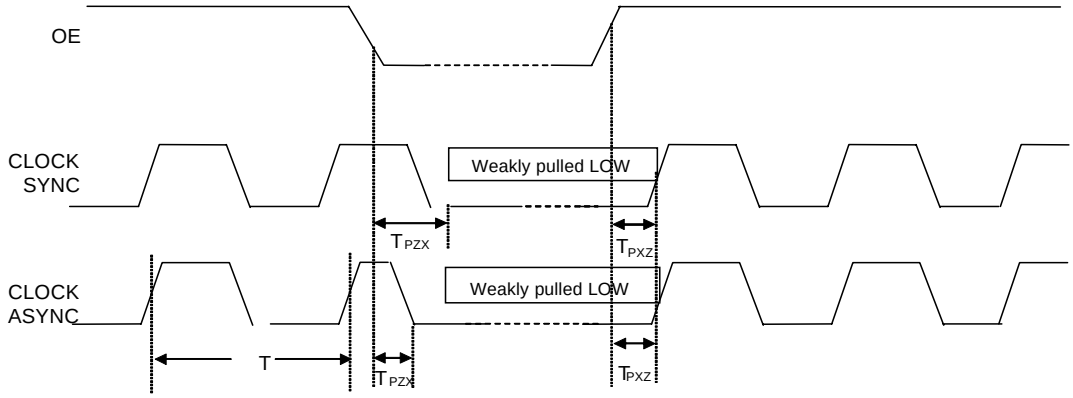


Figure 3. Output Enable Timing

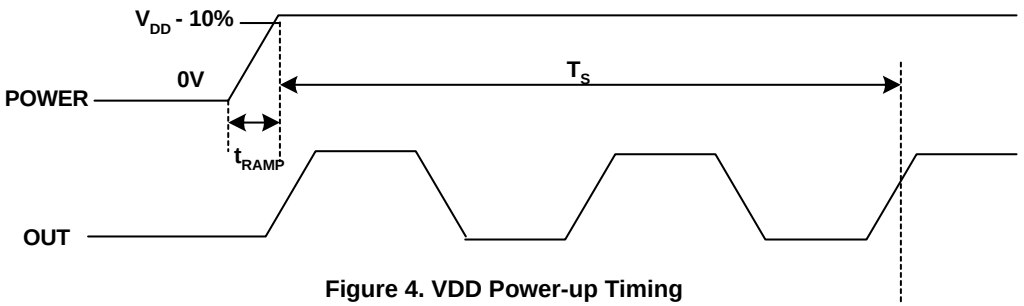
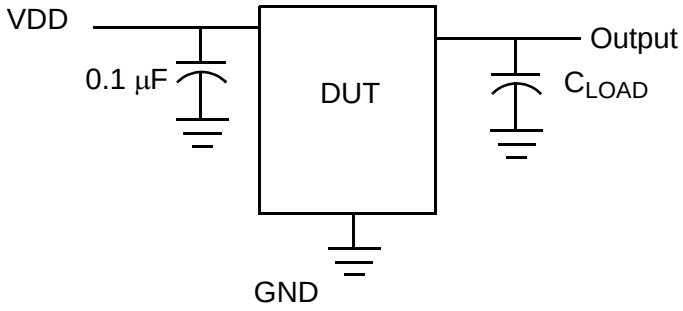


Figure 4. VDD Power-up Timing

Test and Measurement Set-up



Voltage and Timing Definitions

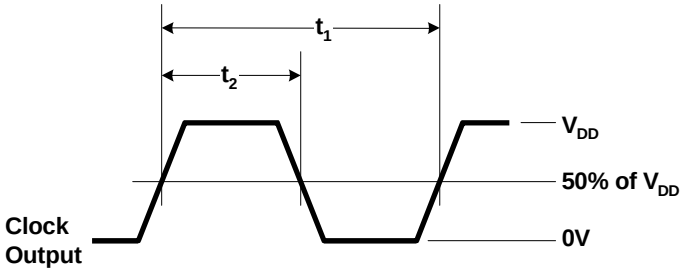


Figure 5. Duty Cycle Definition

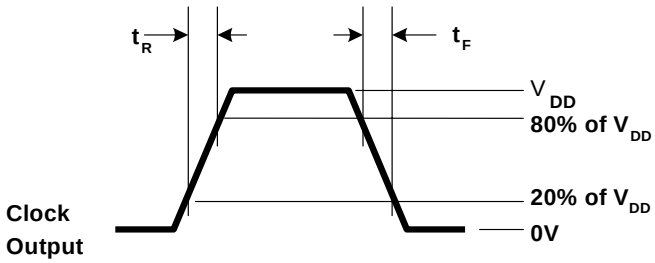


Figure 6.

Ordering Information

Ordering Code	Package Type	Operating Range (TJ)
CY2048WAF[3]	Wafer	Industrial,–40 °C to 125°C

Note:
3. The product is offered as tested die-on-wafer form. Contact Cypress Sales for additional programming information and support.

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Document History Page

Document Title: CY2048WAF Flash Programmable Capacitor Tuning Array Die for Crystal Oscillator(XO) Document Number: 38-07738				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	319840	See ECN	RGL	New data sheet
*A	413511	See ECN	RGL	Minor Change: Pls. post in the web