PRELIMINARY

CY2VC511

27 MHz Clock Generator with VCXO

Features

- Generates 27 MHz Output Clock
- Uses 27 MHz LVCMOS Reference Clock
- LVCMOS Output
- VCXO with 230 ppm Minimum Pull Range
- Fully Integrated Low Noise Phase Locked Loop (PLL)
- Linear Voltage-to-Frequency Control Curve
- Supply Voltage: 3.3V
- Pb-free 16-Pin TSSOP Package

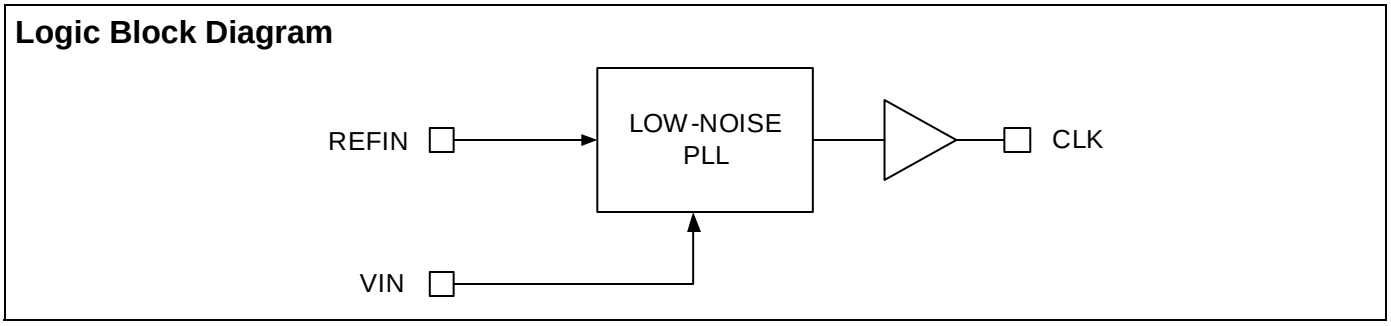
Description

The CY2VC511 is a PLL based clock generator with VCXO control. It takes a low swing 27 MHz reference clock, and generates an adjustable 27 MHz output clock. The device has a single LVCMOS output and operates from a 3.3V power supply.

The VIN pin is an analog input that enables the user to pull the output frequency. The pullability range is at least 230 ppm (±115 ppm). The pull curve is very linear.

Unlike conventional VCXO designs, the output frequency adjustment is achieved by a proprietary PLL design. This permits the use of 27 MHz clock reference.

Logic Block Diagram



Pinout

Figure 1. Pin Diagram - 16-Pin TSSOP

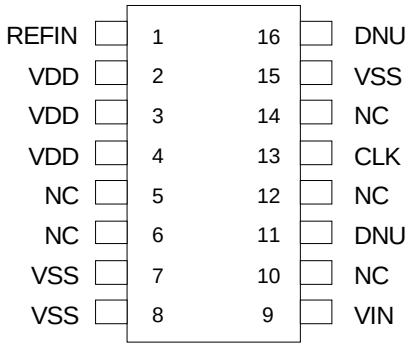


Table 1. Pin Definitions - 16-Pin TSSOP

Pin	Name	Type	Description
1	REFIN	1.8V CMOS Input	**Reference Clock Input**
9	VIN	Analog Input	**VCXO Control Voltage** - VIN has a positive control slope; that is, increasing the voltage on VIN causes the output frequency to increase The nominal output frequency is determined when VIN = 1.65V
13	CLK	CMOS Output	27 MHz Output Clock
11, 16	DNU	–	**Do Not Use**: DNU pins are electrically connected, but perform no function
5, 6, 10, 12, 14	NC	–	**No Connect**: NC pins are not connected to the die
2, 3, 4	VDD	Power	**Supply Voltage**: 3.3V
7, 8, 15	VSS	Power	Ground

Frequency Table

Input		Output Frequency (MHz)
Reference Frequency (MHz)	PLL Multiplier Value	
27	1	27

VCXO and VIN

The output frequency of the device is adjusted over a limited range by use of the VCXO feature. This feature is typically used to phase and frequency lock to a separate reference clock. The frequency is controlled by the analog voltage on the VIN pin. The nominal output frequency is generated when VIN = 1.65V. As the voltage on VIN is increased, the output frequency increases. The voltage range for VIN is from 0V (V_{SS}) to V_{DD}. The relationship between output frequency (ppm) to VIN voltage is very linear over a large portion of the control voltage range.

Application Information

Power Supply Filtering Techniques

As in any high speed analog circuitry, noise on the power supply pins can degrade device performance. For general power plane decoupling, make certain there is at least one tantalum capacitor (~5 to 10 μF) in the general vicinity of this device. Additionally, ensure there is one or two multi-layer ceramic chip capacitors (0.01 or 0.1 μF) located as close as possible to the power and ground pins of the device. Ensure the layout is optimized to minimize power and ground inductance and locate the capacitor as close to the device pins as possible.

Absolute Maximum Conditions

Parameter	Description	Condition	Min	Max	Unit
V_{DD}	Supply Voltage		–0.5	4.4	V
V_{IN}[1]	Input Voltage, DC	Relative to V_{SS}	–0.5	V_{DD} + 0.5	V
T_S	Temperature, Storage	Non operating	–65	150	°C
T_J	Temperature, Junction		–	125	°C
ESD_{HBM}	ESD Protection (Human Body Model)	JEDEC STD 22-A114-B	2000	–	V
UL–94	Flammability Rating	At 1/8 in	V–0		
Θ_{JA}[2]	Thermal Resistance, Junction to Ambient	0 m/s airflow	84		°C/W
		1 m/s airflow	79		
		2.5 m/s airflow	76		

Operating Conditions

Parameter	Description	Min	Typ	Max	Unit
V_{DD}	Supply Voltage Range	3.135	3.3	3.465	V
T_A	Ambient Temperature	0	–	70	°C
T_{PU}	Power up time for V_{DD} to reach minimum specified voltage (ensure power ramp is monotonic)	0.05	–	500	ms
C_{LOAD}	Load Capacitance on CLK output	–	–	15	pF

Notes
1. The voltage on any input or output pin cannot exceed the power pin during power up.
2. Simulated using Apache Sentinel TI software. The board is derived from the JEDEC multilayer standard. It measures 76 x 114 x 1.6 mm and has 4-layers of copper (2/1/1/2 oz.). The internal layers are 100% copper planes, while the top and bottom layers have 50% metalization. No vias are included in the model.

DC Electrical Characteristics

Parameter	Description	Condition	Min	Typ	Max	Unit
I_{DD}	Operating Supply Current	V_{DD} = 3.465V, output unloaded	–	–	110	mA
V_{OH}	High Output Voltage	V_{DD} = min, I_{OH} = –4 mA	0.9*V_{DD}	–	–	V
V_{OL}	Low Output Voltage	V_{DD} = max, I_{OL} = 4 mA	–	–	0.1*V_{DD}	V
V_{IH}	Input High Voltage	For REFIN	1.25	–	1.8	V
V_{IL}	Input Low Voltage	For REFIN	–	–	0.25	V
V_{VIN}	VIN Input Voltage		0	–	V_{DD}	V
I_{VIN}	VIN Input Current	$V_{SS} \le VIN \le V_{DD}$	–10	–	60	µA
INL_{VIN}[3, 4]	VIN to F_{OUT} Integral Nonlinearity	$V_{SS} \le VIN \le V_{DD}$	–	1	–	%

AC Electrical Characteristics [3]

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
F_{OUT}	Output Frequency		–	27	–	MHz
PR	Pull Range	VIN = V_{DD} to V_{SS}, relative to nominal f_{OUT} (VIN = 1.65V) across operating temperature and supply voltage.	±115	–	–	ppm
T_{DC}	Duty Cycle	Measured at V_{DD}/2, defined in Figure 2	45	50	55	%
T_R	Output Rise Time	20% to 80% of V_{DD}, C_{LOAD} = 15 pF	–	0.7	1.5	ns
T_F	Output Fall Time	80% to 20% of V_{DD}, C_{LOAD} = 15 pF	–	0.8	1.5	ns
T_{LOCK}	Start Up Time	Time for CLK to reach valid frequency measured from the time V_{DD} = V_{DD} (min)	–	–	5	ms

Parameter Measurements

Figure 2. Output Duty Cycle Timing

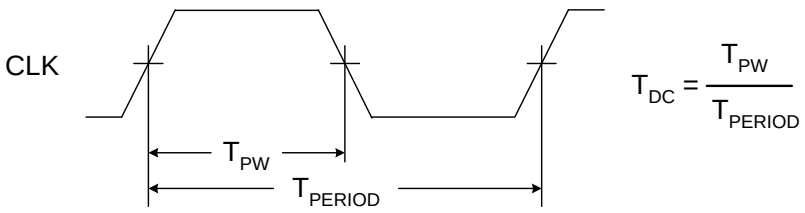
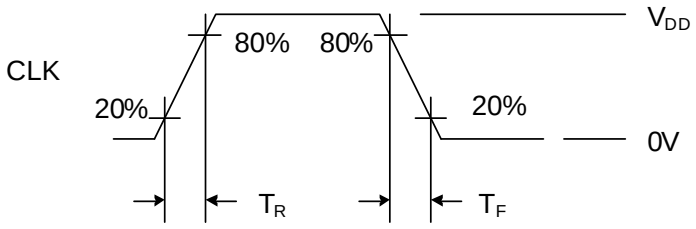


Figure 3. Output Rise and Fall Time



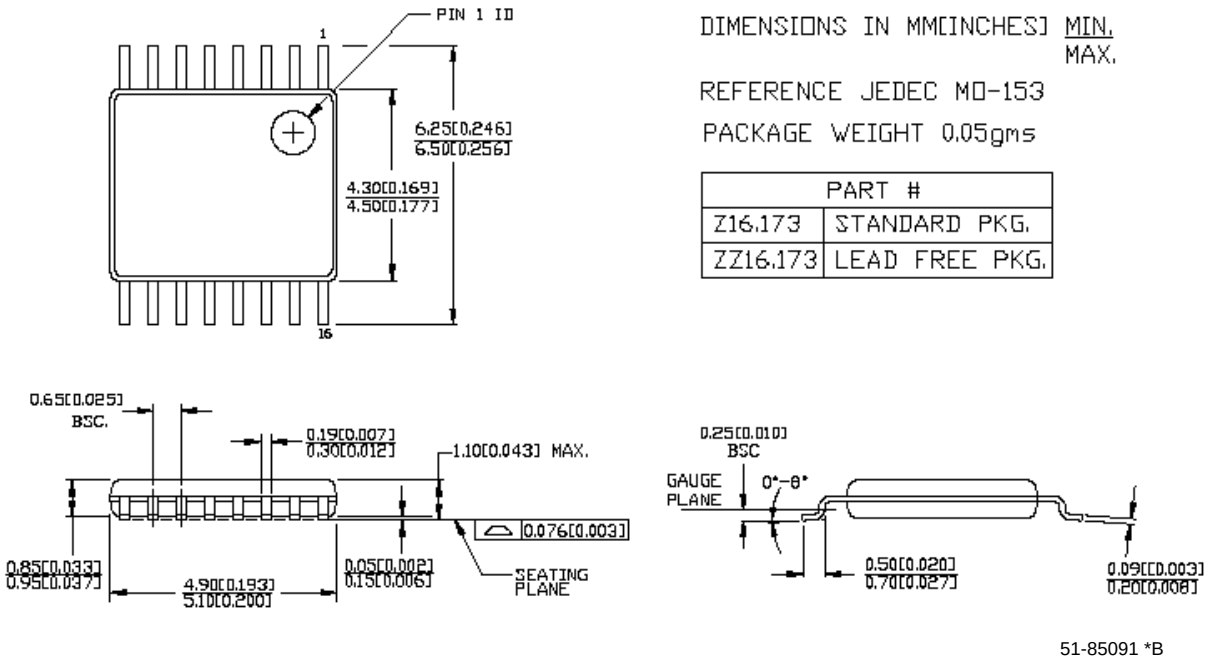
Note
3. Not 100% tested, guaranteed by design and characterization.
4. Integral nonlinearity is defined in IEEE Standard 1241-2000.

Ordering Information

Part Number	Package Description	Product Flow
Pb-Free		
CY2VC511ZXC	16-Pin TSSOP	Commercial, 0° to 70°C
CY2VC511ZXCT	16-Pin TSSOP - Tape and Reel	Commercial, 0° to 70°C

Package Drawings and Dimensions

Figure 4. 16-Pin TSSOP 4.40 mm Body



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Document History Page

Document Title: CY2VC511 27 MHz Clock Generator with VCXO Document Number: 001-10796				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	506248	RGL	See ECN	New data sheet
*A	1285703	JWK/KVM/ ARI	See ECN	Changed definition of nominal frequency to VIN = 1.65V Added C_{LOAD} specification Changed R_{UP} value Corrected T_R/T_F conditions and specification Removed pull down resistor on SEL Updated several drawings Edited data sheet for template compliance
*B	2705638	XHT/KVM/ AESA	05/13/2009	Changed title from Low Noise Clock Generator with VCXO to 27 MHz Clock Generator with VCXO, Basic configuration change: Reference changed from crystal to driven clock, Output changed from 216 MHz to 27 MHz, Pinout changed to show no connects, Pin 11 changed to DNU, V_{DD} range changed from ±0.2V to ±5%, Thermal resistance data added, IOL & IOH changed from 2mA to 4mA Phase noise specs removed, IIVIN changed from 10µA to 60µA, Rise & fall times changed, IDD changed
*C	2768029	KVM	09/18/2009	Remove reference to OE/PD# pin in I_{DD} spec Change parameter name I_{IVIN} to I_{VIN} Change parameter LIN to INL_{VIN}, add note to definition Add max limit for T_R, T_F: 1.5 ns Change T_{LOCK} max from 10 ms to 5 ms
*D	2905106	KVM	05/14/10	Updated package diagram.

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