MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MTD3055EL

Motorola Preferred Device

Designer's Data Sheet

TMOS IV
Power Field Effect Transistor
N-Channel Enhancement-Mode Silicon Gate

TMOS POWER MOSFET
LOGIC LEVEL
10 AMPERES
$R_{DS(on)}$ = 0.18 OHM
60 VOLTS

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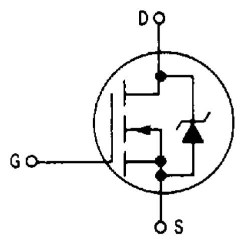
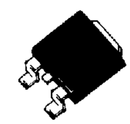
This advanced E-FET is a TMOS power MOSFET designed to withstand high energy in the avalanche and commutation modes. This device is also designed with a low threshold voltage so it is fully enhanced with 5 Volts. This new energy efficient device also offers a drain-to-source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

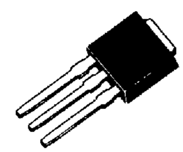
- Low Drive Requirement to Interface Power Loads to Logic Level ICs or Microprocessors — $V_{GS(th)}$ = 2 Volts Max
- Internal Source-to-Drain Diode Designed to Replace External Zener Transient Suppressor — Absorbs High Energy in the Avalanche Mode — Unclamped Inductive Switching (UIS) Energy Capability Specified at 100°C
- Commutating Safe Operating Area (CSOA) Specified for Use in Half and Full Bridge Circuits
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS}, $V_{GS(th)}$ and $V_{DS(on)}$ Specified at 150°C
- Available With Long Leads, Add 1 Suffix

TMOS®





CASE 369A-10
MTD3055EL



CASE 369-06
MTD3055EL1

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	60	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	60	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ($t_p \leq 50\ \mu s$)	V_{GS}	±15 ±20	Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	10 26	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	40 0 32	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	3.12 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design

Preferred device is a Motorola recommended choice for future use and best overall value.

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ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	$V_{(BR)DSS}$	60	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 60 V, V_{GS} = 0) (V_{DS} = 60 V, V_{GS} = 0, T_J = 150°C)	I_{DSS}	— —	10 50	μA
Gate-Body Leakage Current, Forward (V_{GSF} = 15 Vdc, V_{DS} = 0)	I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 15 Vdc, V_{DS} = 0)	I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*				
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) T_J = 150°C	$V_{GS(th)}$	1 0.6	2 1.6	Vdc
Static Drain-Source On-Resistance (V_{GS} = 5 Vdc, I_D = 6 Adc)	$R_{DS(on)}$	—	0 18	Ohm
Drain-Source On-Voltage (V_{GS} = 5 V) (I_D = 10 Adc) (I_D = 6 Adc, T_J = 150°C)	$V_{DS(on)}$	— —	2.4 1.95	Vdc
Forward Transconductance (V_{DS} = 15 V, I_D = 6 A)	g_{FS}	5	—	mhos
DRAIN-TO-SOURCE AVALANCHE CHARACTERISTICS				
Unclamped Drain-to-Source Avalanche Energy See Figures 13 and 14 (I_D = 26 A, V_{DD} = 6 V, T_C = 25°C, Single Pulse, Non-repetitive) (I_D = 12 A, V_{DD} = 6 V, T_C = 25°C, P.W ≤ 100 μs, Duty Cycle ≤ 1%) (I_D = 4.8 A, V_{DD} = 6 V, T_C = 100°C, P.W. ≤ 100 μs, Duty Cycle ≤ 1%)	W_{DSR}	— — —	18 35 16	mJ

DYNAMIC CHARACTERISTICS

Characteristic	Conditions	Symbol	Min	Max	Unit
Input Capacitance	V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz	C_{iss}	400 (Typ)	—	pF
	V_{GS} = 15 V, V_{DS} = 0, f = 1 MHz See Figure 15		1000 (Typ)	—	
Reverse Transfer Capacitance	V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz	C_{rss}	30 (Typ)	—	pF
	V_{GS} = 15 V, V_{DS} = 0, f = 1 MHz See Figure 15		660 (Typ)	—	
Output Capacitance	V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz See Figure 15	C_{oss}	175 (Typ)	—	pF

SWITCHING CHARACTERISTICS (T_J = 100°C)

Characteristic	Conditions	Symbol	Min	Max	Unit
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 6 A, V_{GS} = 5 V, R_{gen} = 50 ohms, R_{GS} = 50 ohms)	$t_{d(on)}$	20 (Typ)	—	ns
Rise Time		t_r	95 (Typ)	—	
Turn-Off Delay Time		$t_{d(off)}$	38 (Typ)	—	
Fall Time		t_f	50 (Typ)	—	
Total Gate Charge	(V_{DS} = 48 V, I_D = 12 A, V_{GS} = 5 Vdc) See Figures 16 and 17	Q_g	7.2 (Typ)	17	nC
Gate-Source Charge		Q_{gs}	2 (Typ)	—	
Gate-Drain Charge		Q_{gd}	4 (Typ)	—	

SOURCE DRAIN DIODE CHARACTERISTICS

Characteristic	Conditions	Symbol	Min	Max	Unit
Forward On-Voltage	(I_S = 12 A, V_{GS} = 0)	V_{SD}	1.04 (Typ)	1.18	Vdc
Forward Turn-On Time	(I_S = 26 A, V_{GS} = 0, dI_S/dt = 400 A/μs, V_R = 30 V)	t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	55 (Typ)	—	ns

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TYPICAL ELECTRICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

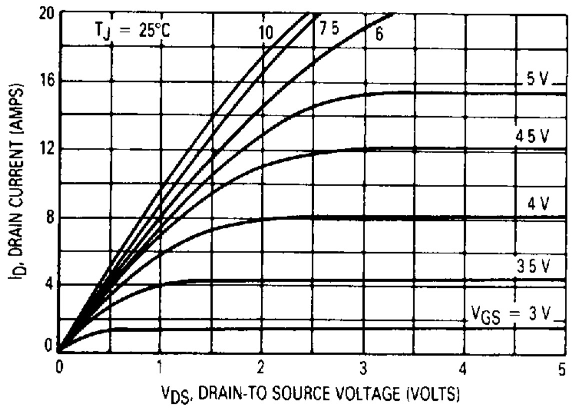


Figure 2. Gate-Threshold Voltage Variation With Temperature

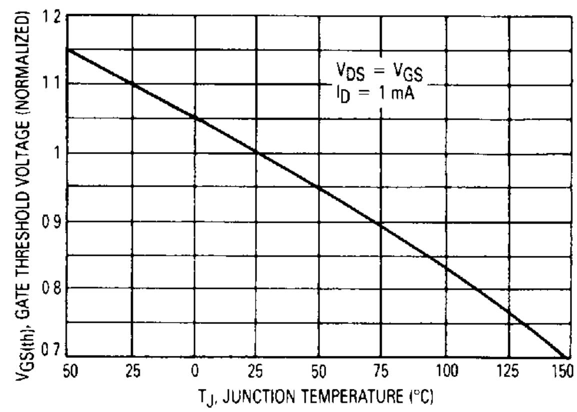


Figure 3. Transfer Characteristics

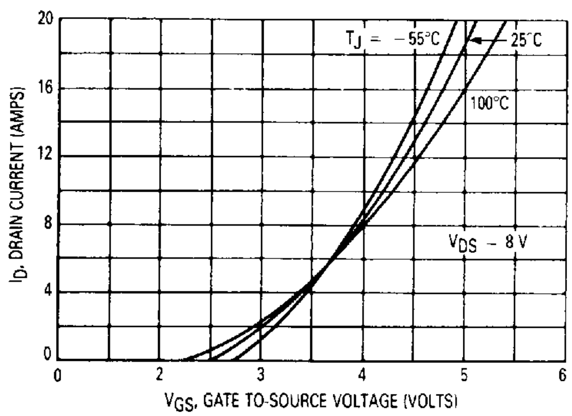


Figure 4. On-Resistance versus Drain Current

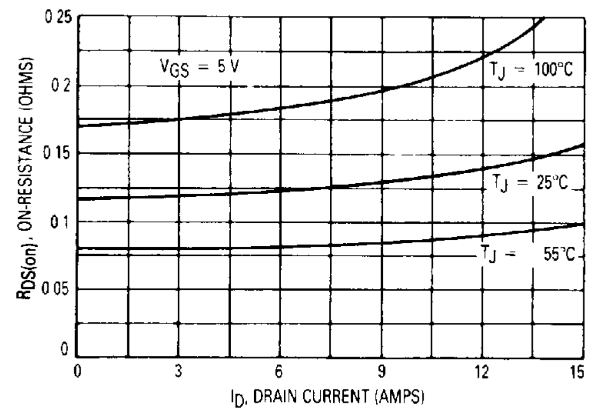


Figure 5. On-Resistance versus Gate-to-Source Voltage

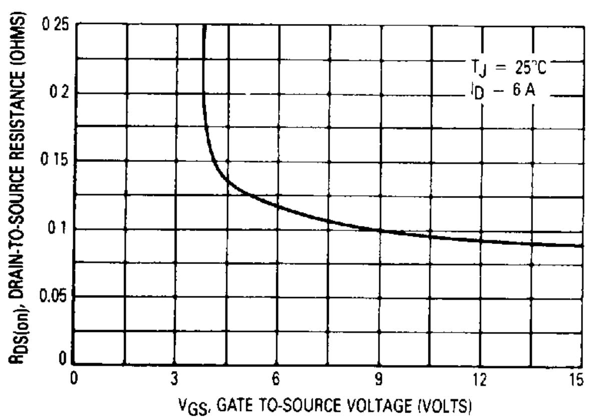


Figure 6. On-Resistance Variation With Temperature

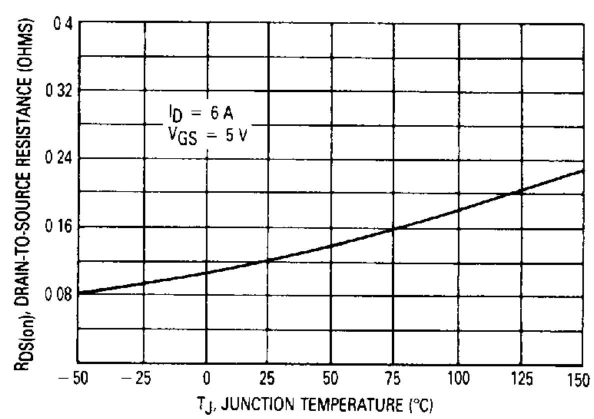


Figure 7. Breakdown Voltage Variation With Temperature

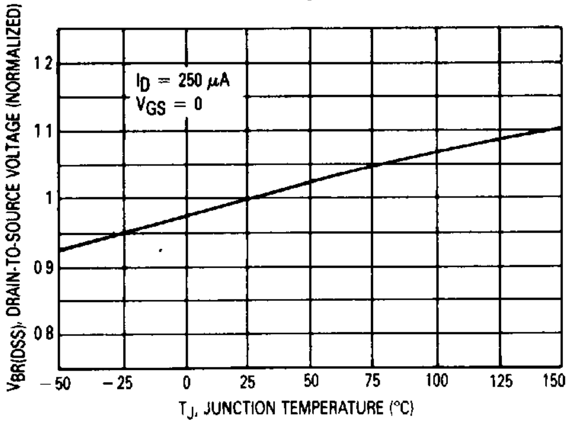
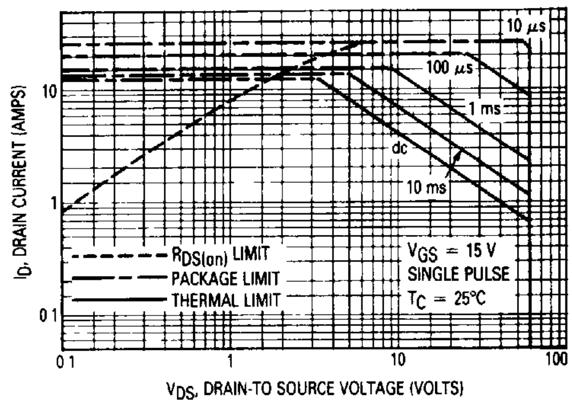


Figure 8. Maximum Rated Forward Biased Safe Operating Area



FORWARD BIASED SAFE OPERATING AREA

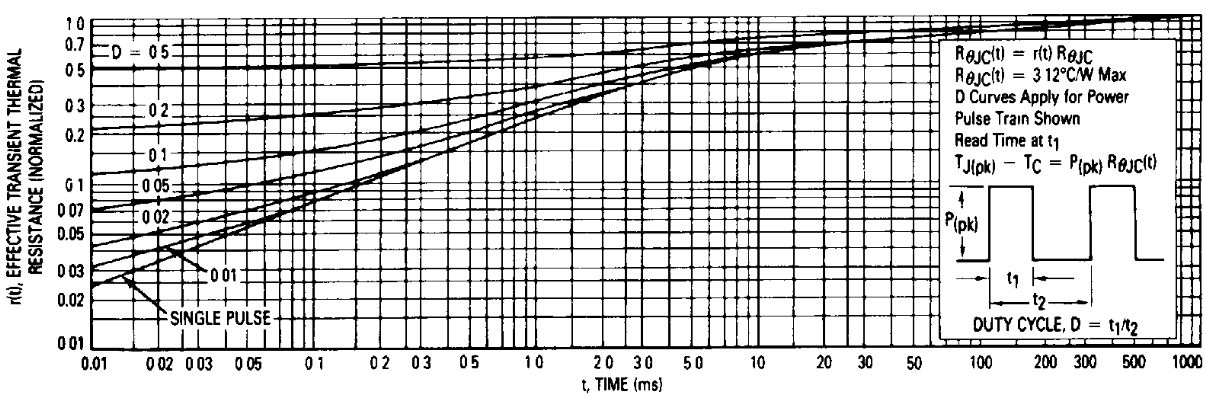
The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

The switching safe operating area fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. This is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

Figure 9. Thermal Response



COMMUTATING SAFE OPERATING AREA (CSOA)

The Commutating Safe Operating Area (CSOA) of Figure 11 defines the limits of safe operation for commutated source-drain current versus re-applied drain voltage when the source-drain diode has undergone forward bias. The curve shows the limitations of I_{FM} and peak V_{DS} for a given rate of change of source current. It is applicable when waveforms similar to those of Figure 10 are present. Full or half-bridge PWM DC motor controllers are common applications requiring CSOA data.

Device stresses increase with increasing rate of change of source current so dI_S/dt is specified with a maximum value. Higher values of dI_S/dt require an appropriate derating of I_{FM}, peak V_{DS} or both. Ultimately dI_S/dt is limited primarily by device, package, and circuit impedances. Maximum device stress occurs during t_{rr} as the diode goes from conduction to reverse blocking.

$V_{DS(pk)}$ is the peak drain-to-source voltage that the device must sustain during commutation; I_{FM} is the maximum forward source-drain diode current just prior to the onset of commutation.

V_R is specified at 80% of $V_{(BR)DSS}$ to ensure that the CSOA stress is maximized as I_S decays from I_{RM} to zero.

R_{GS} should be minimized during commutation. T_J has only a second order effect on CSOA.

Stray inductances in Motorola's test circuit are assumed to be practical minimums. dV_{DS}/dt in excess of 10 V/ns was attained with dI_S/dt of 400 A/µs.

Figure 10. Commutating Waveforms

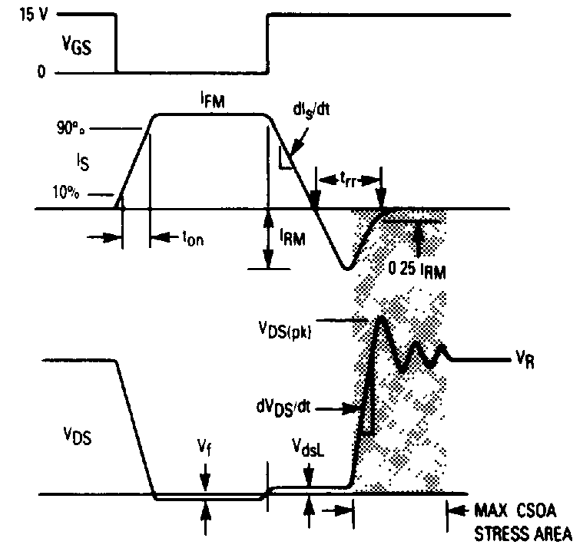


Figure 11. Commutating Safe Operating Area (CSOA)

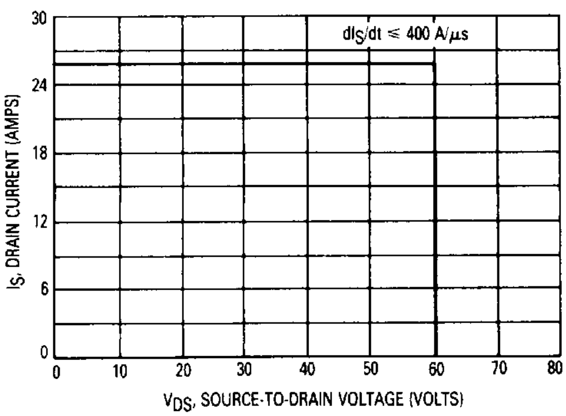


Figure 12. Commutating Safe Operating Area Test Circuit

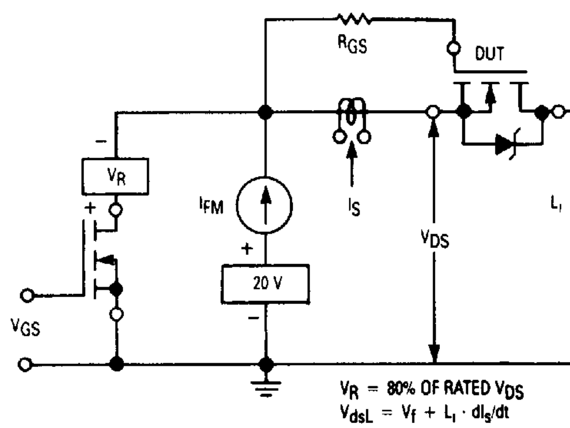


Figure 13. Unclamped Inductive Switching Test Circuit

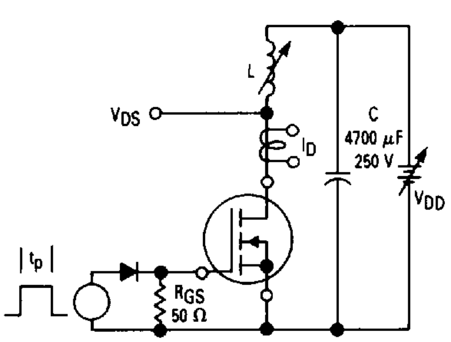
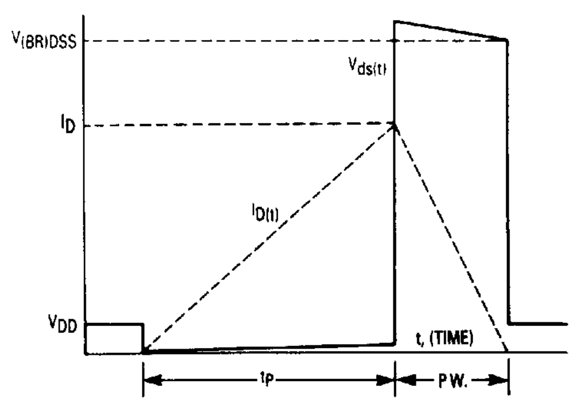


Figure 14. Unclamped Inductive Switching Waveforms



$$W_{DSR} = \left(\frac{1}{2} L I_D^2\right)\left(\frac{V_{(BR)DSS}}{V_{(BR)DSS} - V_{DD}}\right)$$

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Figure 15. Capacitance Variation

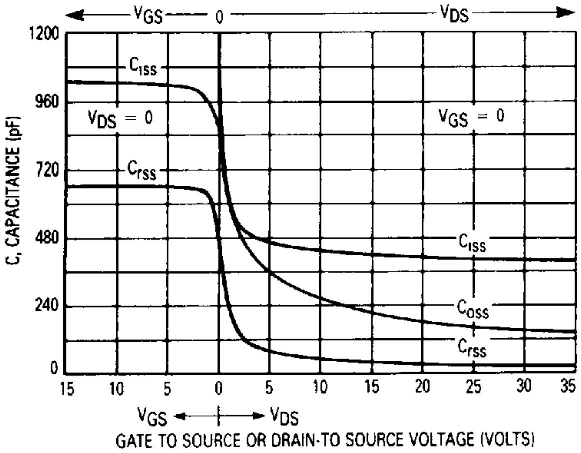

Figure 16. Gate Charge versus Gate-to-Source Voltage

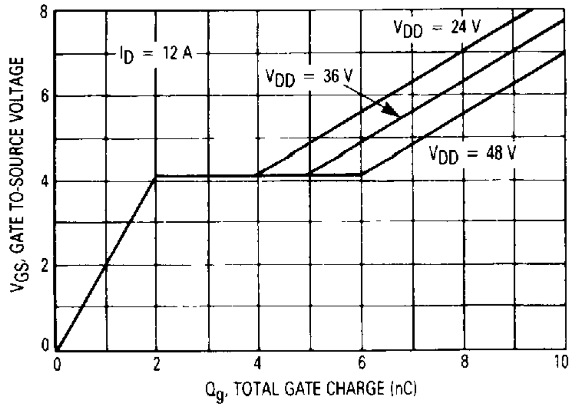

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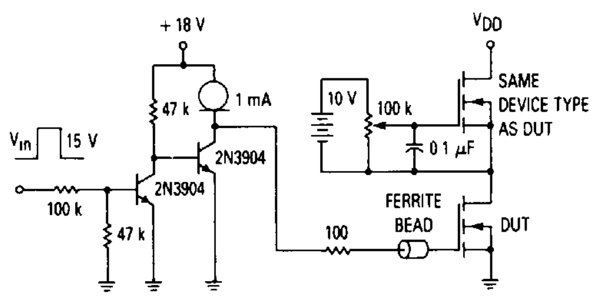
Figure 17. Gate Charge Test Circuit



V_{in} = 15 V_{pk}, PULSE WIDTH ≤ 100 μs, DUTY CYCLE ≤ 10%