Data Sheet | October 1999 | File Number 3598.3

## 7A, 100V, 0.300 Ohm, N-Channel, Logic Level, Power MOSFETs

These N-Channel power MOSFETs are manufactured using a modern process. This process, which uses feature sizes approaching those of LSI integrated circuits gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers and emitter switches for bipolar transistors. This performance is accomplished through a special gate oxide design which provides full rated conductance at gate bias in the 3V to 5V range, thereby facilitating true on-off power control directly from logic level (5V) integrated circuits.

Formerly developmental type TA49046.

## Ordering Information

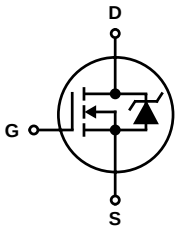
| PART NUMBER | PACKAGE | BRAND |
|---|---|---|
| RFD7N10LE | TO-251AA | 7N10L |
| RFD7N10LESM | TO-252AA | 7N10LE |

NOTE: When ordering, use the entire part number. Add suffix 9A to obtain the TO-252AA variant in the tape and reel, i.e., RFD7N10LESM9A.

## Features

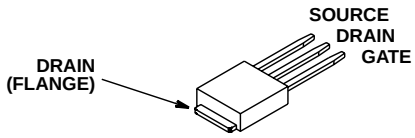
- 7A, 100V
- $r_{DS(ON)} = 0.300\Omega$
- Temperature Compensating PSPICE® Model
- Can be Driven Directly from CMOS, NMOS, TTL Circuits
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- $175^{o}C$ Operating Temperature
- Related Literature
  - TB334 “Guidelines for Soldering Surface Mount Components to PC Boards”

## Symbol

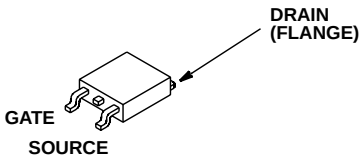



## Packaging

JEDEC TO-251AA




JEDEC TO-252AA



## Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

| | | RFD7N10LE, RFD7N10LESM | UNITS |
|---|---|---|---|
| Drain to Source Voltage | $V_{DSS}$ | 100 | V |
| Drain to Gate Voltage | $V_{DGR}$ | 100 | V |
| Gate to Source Voltage | $V_{GS}$ | +10, -8 | V |
| Drain Current | | | |
| Continuous | $I_D$ | 7 | A |
| Pulsed Drain Current | $I_{DM}$ | Refer to Peak Current Curve | |
| Pulsed Avalanche Rating | $E_{AS}$ | Refer to UIS Curve | |
| Power Dissipation | $P_D$ | 47 | W |
| Derate Above $25^oC$ | | 0.318 | $W/^oC$ |
| Operating and Storage Temperature | $T_J$, $T_{STG}$ | -55 to 175 | $^oC$ |
| Maximum Temperature for Soldering | | | |
| Leads at 0.063in (1.6mm) from Case for 10s | $T_L$ | 300 | $^oC$ |
| Package Body for 10s, See Techbrief 334 | $T_{pkg}$ | 260 | $^oC$ |

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

NOTE:

1. $T_J = 25^oC$ to $150^oC$.

## Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

| PARAMETER | SYMBOL | TEST CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Drain to Source Breakdown Voltage | $BV_{DSS}$ | $I_D = 250\mu A$, $V_{GS} = 0V$ | | 100 | - | - | V |
| Gate Threshold Voltage | $V_{GS(TH)}$ | $V_{GS} = V_{DS}$, $I_D = 250\mu A$ | | 1 | - | 3 | V |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS} = 95V$, $V_{GS} = 0V$ | | - | - | 1 | μA |
| | | $V_{DS} = 90V$, $V_{GS} = 0V$, $T_C = 150^oC$ | | - | - | 250 | μA |
| Gate to Source Leakage Current | $I_{GSS}$ | $V_{GS} = +10, -8V$ | | - | - | 10 | μA |
| On Resistance | $r_{DS(ON)}$ | $I_D = 7A$, $V_{GS} = 5V$ | | - | - | 0.300 | Ω |
| Turn-On Time | $t_{ON}$ | $V_{DD} = 50V$, $I_D = 7A$, $R_L = 7.1\Omega$, $V_{GS} = 5V$, $R_{GS} = 2.5\Omega$ | | - | - | 110 | ns |
| Turn-On Delay Time | $t_{d(ON)}$ | | | - | 10 | - | ns |
| Rise Time | $t_r$ | | | - | 65 | - | ns |
| Turn-Off Delay Time | $t_{d(OFF)}$ | | | - | 23 | - | ns |
| Fall Time | $t_f$ | | | - | 18 | - | ns |
| Turn-Off Time | $t_{OFF}$ | | | - | - | 60 | ns |
| Total Gate Charge | $Q_{g(TOT)}$ | $V_{GS} = 0$ to $10V$ | $V_{DD} = 80V$, $I_D = 7A$, $R_L = 11.4\Omega$ | - | 125 | 150 | nC |
| Gate Charge at 5V | $Q_{g(5)}$ | $V_{GS} = 0$ to $5V$ | | - | 67 | 80 | nC |
| Threshold Gate Charge | $Q_{g(TH)}$ | $V_{GS} = 0$ to $1V$ | | - | 3.7 | 4.5 | nC |
| Input Capacitance | $C_{ISS}$ | $V_{DS} = 25V$, $V_{GS} = 0V$, f = 1MHz | | - | 360 | - | pF |
| Output Capacitance | $C_{OSS}$ | | | - | 70 | - | pF |
| Reverse Transfer Capacitance | $C_{RSS}$ | | | - | 20 | - | pF |
| Thermal Resistance Junction to Case | $R_{\theta JC}$ | | | - | - | 3.15 | $^oC/W$ |
| Thermal Resistance Junction to Ambient | $R_{\theta JA}$ | TO-251 and TO-252 Package | | - | - | 100 | $^oC/W$ |

## Source to Drain Diode Specifications

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Source to Drain Diode Voltage | $V_{SD}$ | $I_{SD} = 7A$ | - | - | 1.5 | V |
| Reverse Recovery Time | $t_{rr}$ | $I_{SD} = 7A$, $dI_{SD}/dt = 100A/\mu s$ | - | - | 130 | ns |

## Typical Performance Curves Unless Otherwise Specified

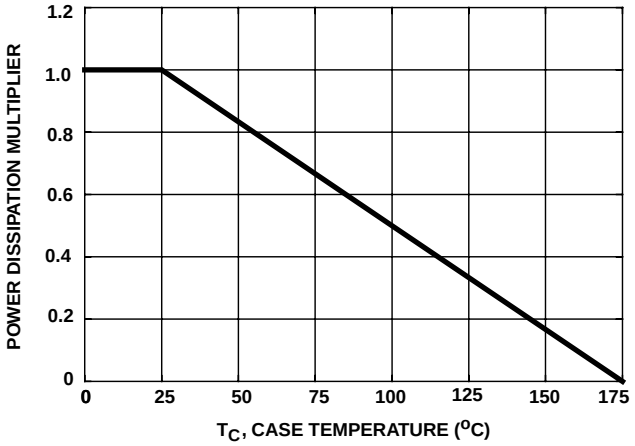



FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

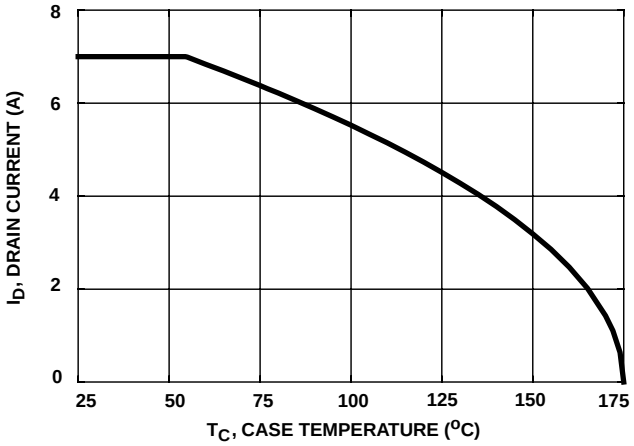



FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

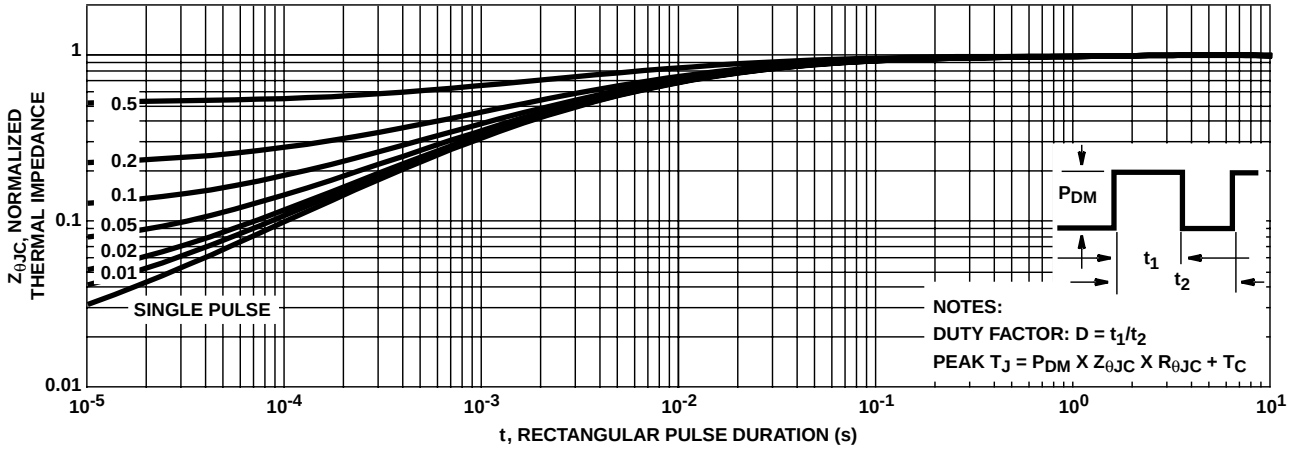



FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

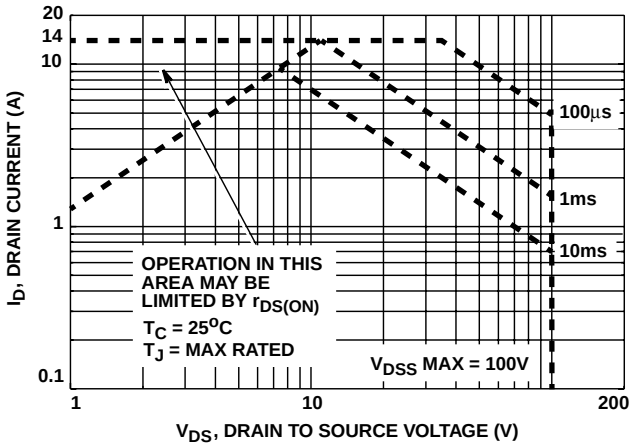



FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

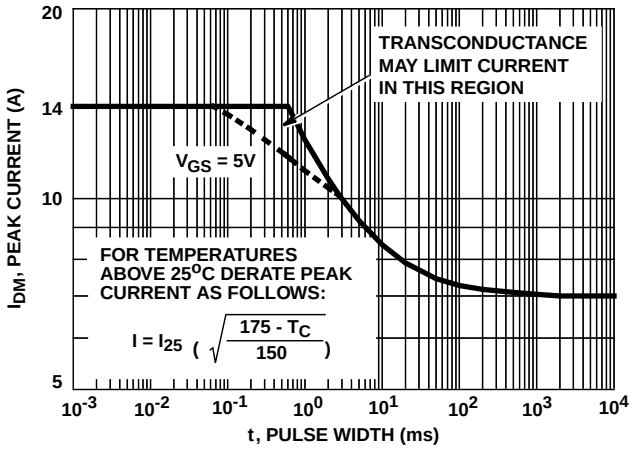



FIGURE 5. PEAK CURRENT CAPABILITY

## Typical Performance Curves Unless Otherwise Specified **(Continued)**

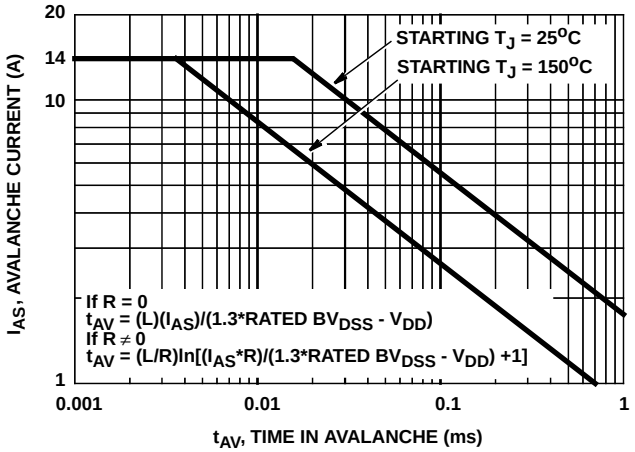



FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING

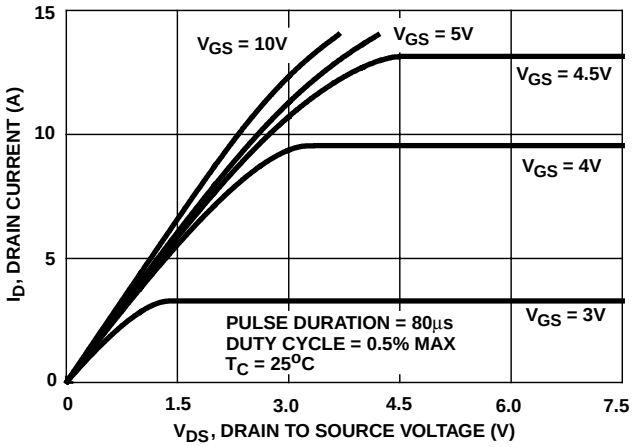



FIGURE 7. SATURATION CHARACTERISTICS

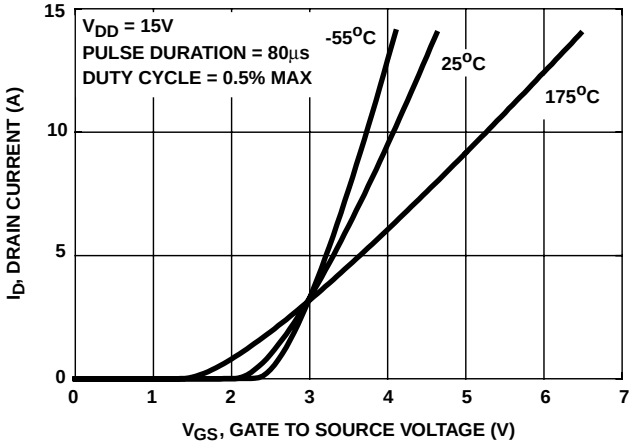



FIGURE 8. TRANSFER CHARACTERISTICS

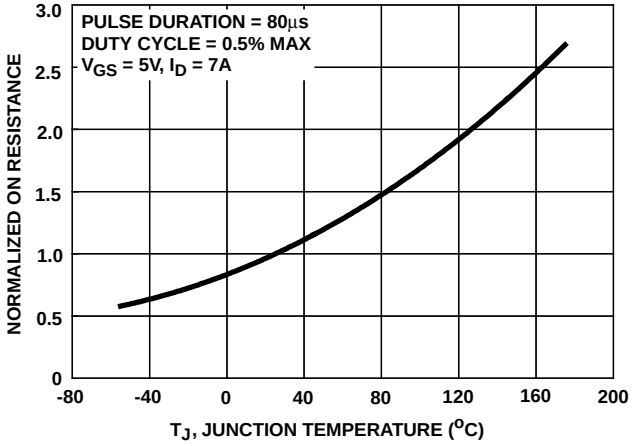



FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

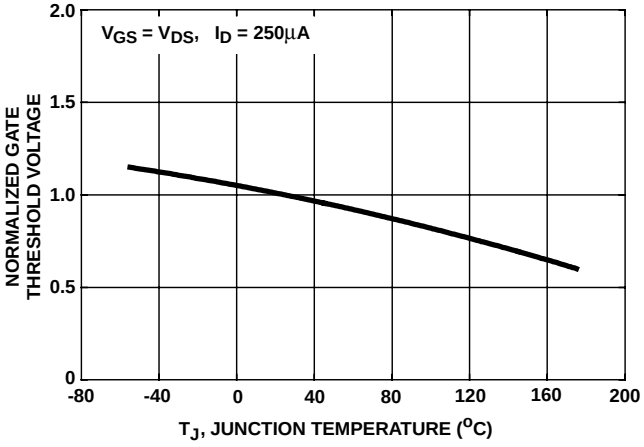



FIGURE 10. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

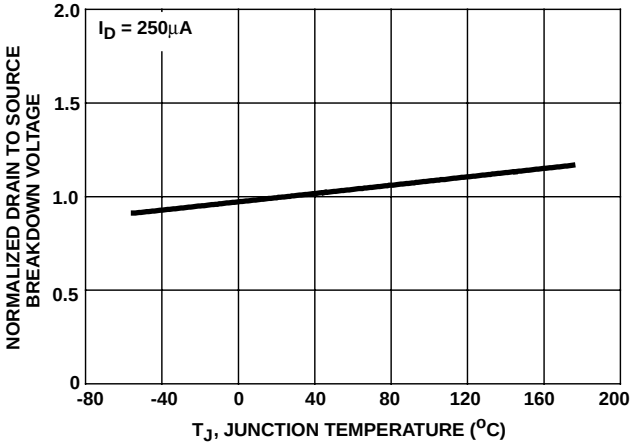



FIGURE 11. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

## Typical Performance Curves Unless Otherwise Specified **(Continued)**

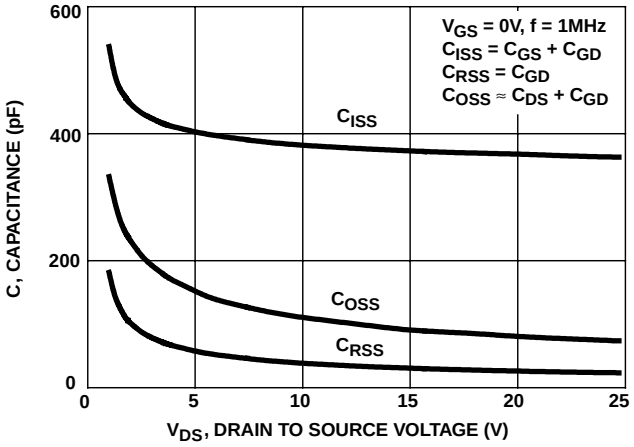
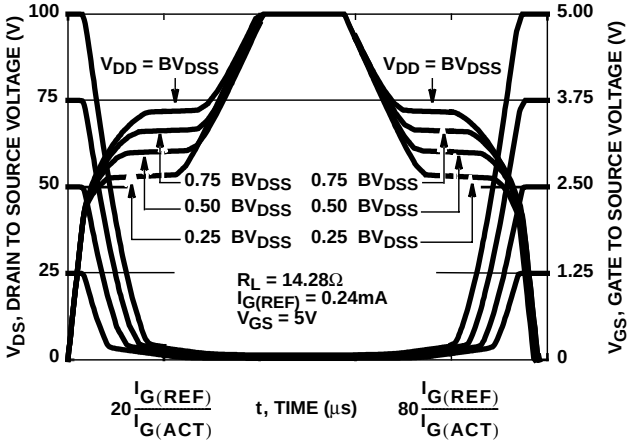



**FIGURE 12. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE**




NOTE: Refer to Intersil Application Notes AN7254 and AN7260.

**FIGURE 13. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT**

## Test Circuits and Waveforms

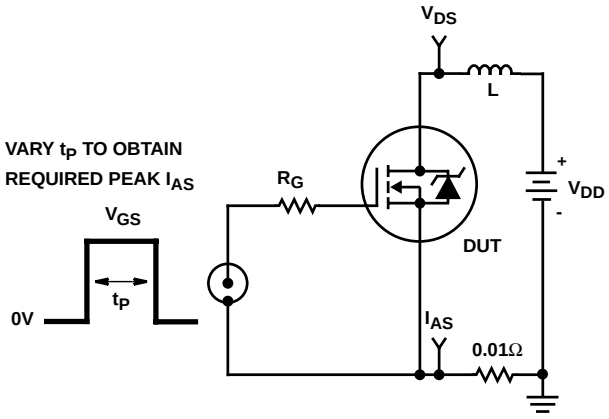



**FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT**

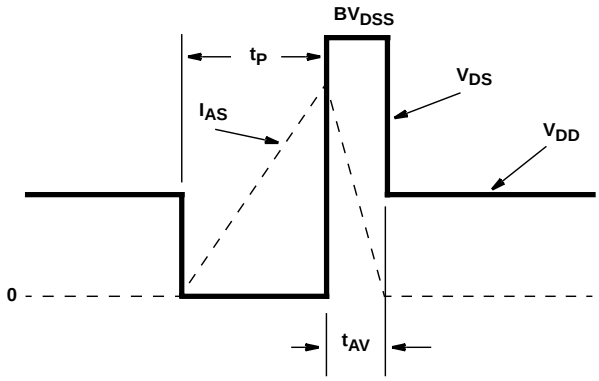



**FIGURE 15. UNCLAMPED ENERGY WAVEFORMS**

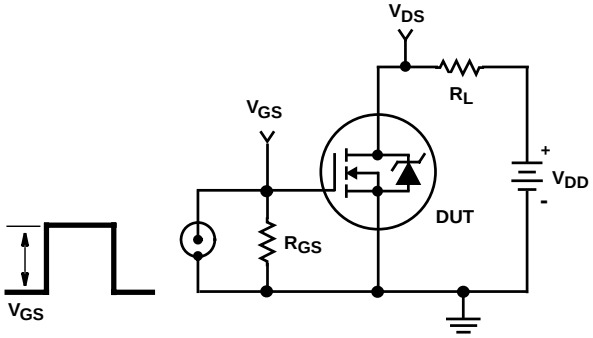



**FIGURE 16. RESISTIVE SWITCHING TEST CIRCUIT**

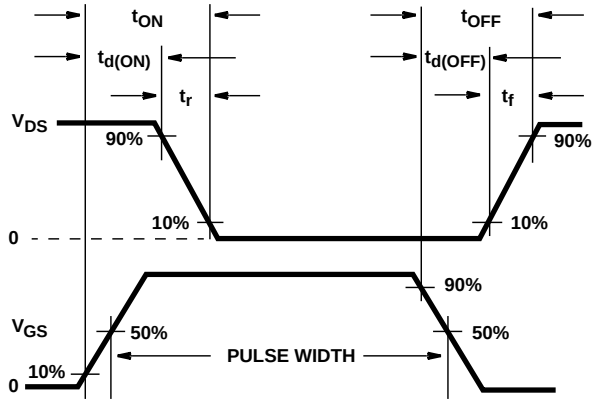



**FIGURE 17. RESISTIVE SWITCHING WAVEFORMS**

## PSPICE Electrical Model

SUBCKT RFD7N10LE 2 1 3;  rev 6/2/93

CA 12 8 7.5e-10
CB 15 14 7.6e-10
CIN 6 8 4.03e-10

DBODY 7 5 DBODYMOD
DBREAK 5 11 DBREAKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 116.7
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTHRES 6 21 19 8 1
EVTEMP 20 6 18 22 1

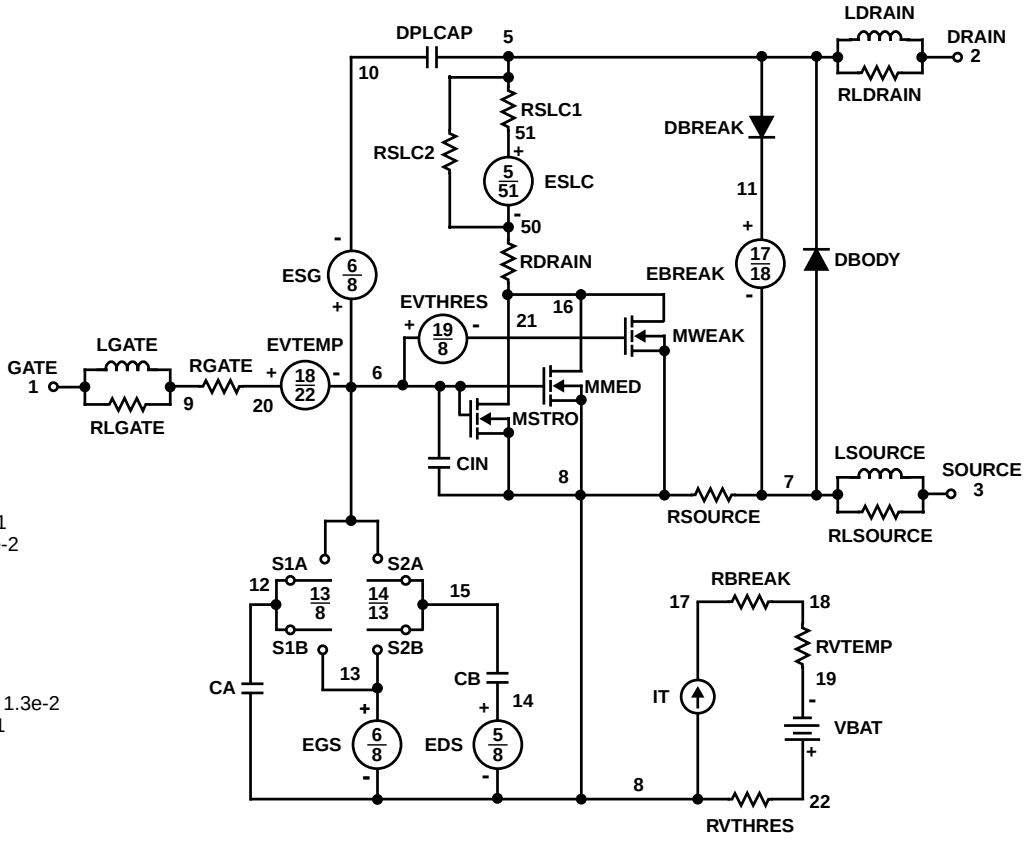
IT 8 17 1

LDRAIN 2 5 1e-9
LGATE 1 9 3.7e-9
LSOURCE 3 7 3.4e-9

MMED 16 6 8 8 MMEDMOD
MSTRO 16 6 8 8 MSTROMOD
MWEAK 16 21 8 8 MWEAKMOD

RBREAK 17 18 RBREAKMOD 1
RDRAIN 50 16 RDRAINMOD 9.4e-2
RGATE 9 20 3.3
RLDRAIN 2 5 10
RLGATE 1 9 37
RLSOURCE 3 7 34
RSLC1 5 51 RSLCMOD 1e-6
RSLC2 5 50 1e3
RSOURCE 8 7 RSOURCEMOD 1.3e-2
RVTHRES 22 8 RVTHRESMOD 1
RVTEMP 18 19 RVTEMPMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD




VBAT 22 19 DC 1

ESLC 51 50 VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*17.3),3.5))}

.MODEL DBODYMOD D (IS = 1.2e-12 RS = 1.2e-2 TRS1 = 1.2e-3 TRS2 = 1.03e-6 CJO = 6.7e-10 TT = 6.9e-8 M = 0.77)
.MODEL DBREAKMOD D (RS = 9.9e-1 TRS1 = 1e-3 TRS2 = -2e-5)
.MODEL DPLCAPMOD D (CJO = 4.3e-10 IS = 1e-30 M = 0.9 N = 10)
.MODEL MMEDMOD NMOS (VTO = 1.88 KP = 5 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 3.3)
.MODEL MSTROMOD NMOS (VTO = 2.13 KP = 12.4 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL MWEAKMOD NMOS (VTO = 1.59 KP = 0.12 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 33 RS = 0.1)
.MODEL RBREAKMOD RES (TC1 = 1.05e-3 TC2 = -5e-7)
.MODEL RDRAINMOD RES (TC1 = 8.1e-3 TC2 = 2.4e-5)
.MODEL RSLCMOD RES (TC1 = 3e-3 TC2 = 2e-6)
.MODEL RSOURCEMOD RES (TC1 = 1e-3 TC2 = 1e-6)
.MODEL RVTHRESMOD RES (TC1 = -1.5e-3 TC2 = -4.3e-6)
.MODEL RVTEMPMOD RES (TC1 = -1.6e-3 TC2 = 1.5e-6)

.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -4.5 VOFF= -2.5)
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -2.5 VOFF= -4.5)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -0.3 VOFF= 0.2)
.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 0.2 VOFF= -0.3)

.ENDS

NOTE: For further discussion of the PSPICE model consult A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options; IEEE Power Electronics Specialist Conference Records 1991.

## Sales Office Headquarters

**NORTH AMERICA**
Intersil Corporation
P. O. Box 883, Mail Stop 53-204
Melbourne, FL 32902
TEL: (407) 724-7000
FAX: (407) 724-7240

**EUROPE**
Intersil SA
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

**ASIA**
Intersil (Taiwan) Ltd.
7F-6, No. 101 Fu Hsing North Road
Taipei, Taiwan
Republic of China
TEL: (886) 2 2716 9310
FAX: (886) 2 2715 3029