



April 2000

**QFET™**

## FQD2N60 / FQU2N60

### 600V N-Channel MOSFET

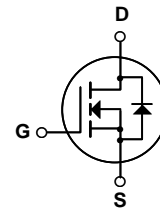
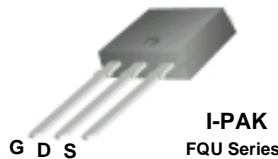
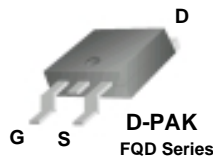
#### General Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switch mode power supply.

#### Features

- 2.0A, 600V,  $R_{DS(on)} = 4.7\Omega @ V_{GS} = 10V$
- Low gate charge ( typical 9.0 nC)
- Low  $C_{rss}$  ( typical 5.0 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



#### Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	FQD2N60 / FQU2N60	Units
$V_{DSS}$	Drain-Source Voltage	600	V
$I_D$	Drain Current - Continuous ( $T_C = 25^\circ\text{C}$ ) - Continuous ( $T_C = 100^\circ\text{C}$ )	2.0	A
		1.26	A
$I_{DM}$	Drain Current - Pulsed (Note 1)	8.0	A
$V_{GSS}$	Gate-Source Voltage	$\pm 30$	V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	140	mJ
$I_{AR}$	Avalanche Current (Note 1)	2.0	A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	4.5	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5	V/ns
$P_D$	Power Dissipation ( $T_A = 25^\circ\text{C}$ ) *	2.5	W
	Power Dissipation ( $T_C = 25^\circ\text{C}$ )	45	W
	- Derate above $25^\circ\text{C}$	0.36	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
$T_L$	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ\text{C}$

#### Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	--	2.78	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient *	--	50	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	110	$^\circ\text{C}/\text{W}$

\* When mounted on the minimum pad size recommended (PCB Mount)

Electrical Characteristics <small>T<sub>C</sub> = 25°C unless otherwise noted</small>						
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
<b>Off Characteristics</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	600	--	--	V
ΔBV <sub>DSS</sub> / ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, Referenced to 25°C	--	0.4	--	V/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 600 V, V <sub>GS</sub> = 0 V	--	--	10	μA
		V <sub>DS</sub> = 480 V, T <sub>C</sub> = 125°C	--	--	100	μA
I <sub>GSSF</sub>	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = 30 V, V <sub>DS</sub> = 0 V	--	--	100	nA
I <sub>GSSR</sub>	Gate-Body Leakage Current, Reverse	V <sub>GS</sub> = -30 V, V <sub>DS</sub> = 0 V	--	--	-100	nA
<b>On Characteristics</b>						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	3.0	--	5.0	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 1.0 A	--	3.7	4.7	Ω
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 50 V, I <sub>D</sub> = 1.0 A (Note 4)	--	2.25	--	S
<b>Dynamic Characteristics</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz	--	270	350	pF
C <sub>oss</sub>	Output Capacitance		--	40	50	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		--	5	7	pF
<b>Switching Characteristics</b>						
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 300 V, I <sub>D</sub> = 2.4 A, R <sub>G</sub> = 25 Ω  (Note 4, 5)	--	10	30	ns
t <sub>r</sub>	Turn-On Rise Time		--	25	60	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		--	20	50	ns
t <sub>f</sub>	Turn-Off Fall Time		--	25	60	ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> = 480 V, I <sub>D</sub> = 2.4 A, V <sub>GS</sub> = 10 V  (Note 4, 5)	--	9.0	11	nC
Q <sub>gs</sub>	Gate-Source Charge		--	1.6	--	nC
Q <sub>gd</sub>	Gate-Drain Charge		--	4.3	--	nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current		--	--	2.0	A
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current		--	--	8.0	A
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 2.0 A	--	--	1.4	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 2.4 A, dI <sub>F</sub> / dt = 100 A/μs (Note 4)	--	180	--	ns
Q <sub>rr</sub>	Reverse Recovery Charge		--	0.72	--	μC
<b>Notes:</b>						
1. Repetitive Rating : Pulse width limited by maximum junction temperature						
2. L = 64mH, I <sub>AS</sub> = 2.0A, V <sub>DD</sub> = 50V, R <sub>G</sub> = 25 Ω, Starting T <sub>J</sub> = 25°C						
3. I <sub>SD</sub> ≤ 2.4A, di/dt ≤ 200A/μs, V <sub>DD</sub> ≤ BV <sub>DSS</sub> , Starting T <sub>J</sub> = 25°C						
4. Pulse Test : Pulse width ≤ 300μs, Duty cycle ≤ 2%						
5. Essentially independent of operating temperature						

Typical Characteristics

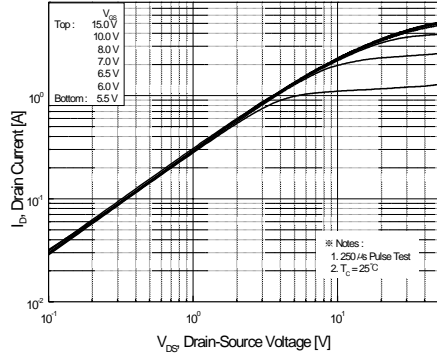


Figure 1. On-Region Characteristics

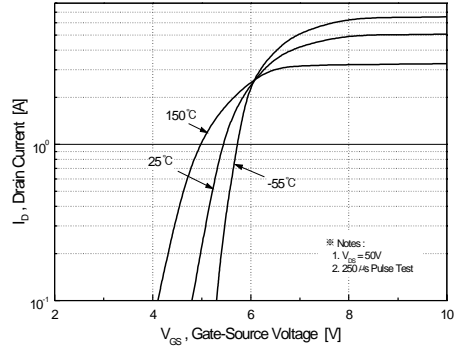


Figure 2. Transfer Characteristics

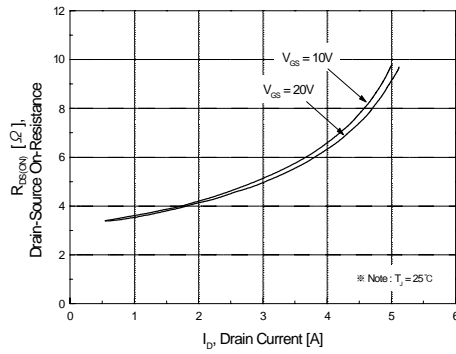


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

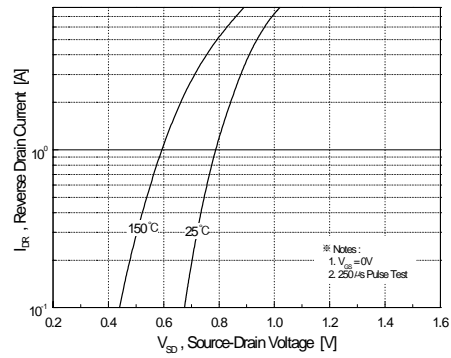


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

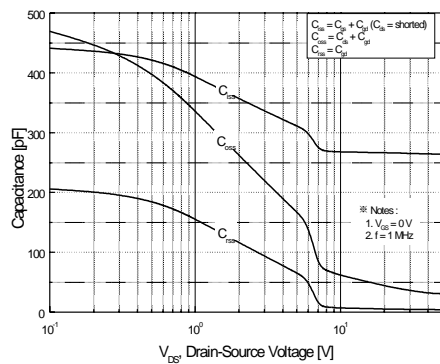


Figure 5. Capacitance Characteristics

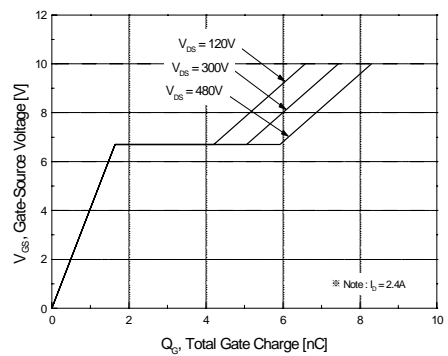
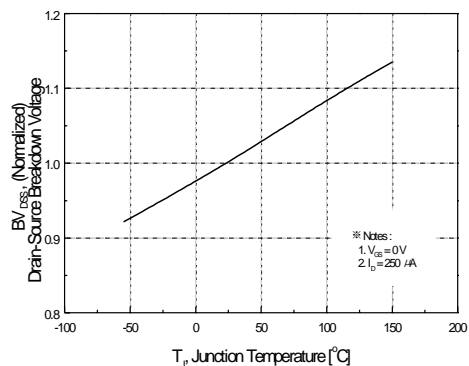
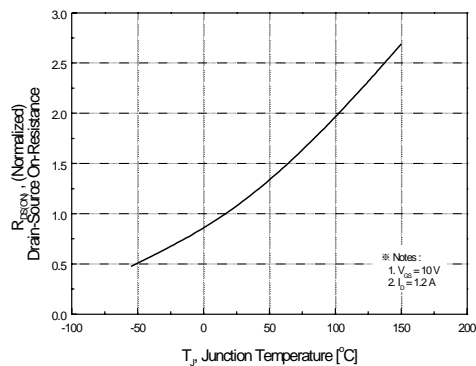


Figure 6. Gate Charge Characteristics

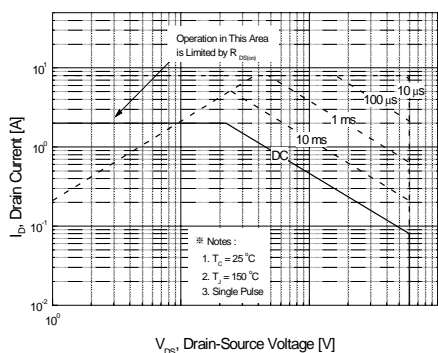
**Typical Characteristics** (Continued)



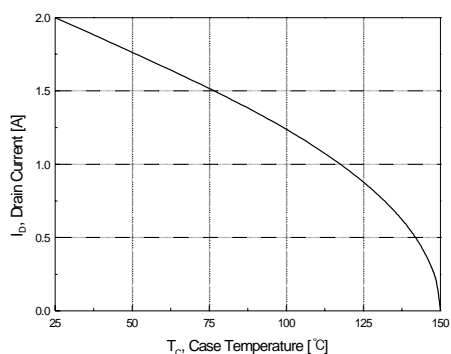
**Figure 7. Breakdown Voltage Variation vs. Temperature**



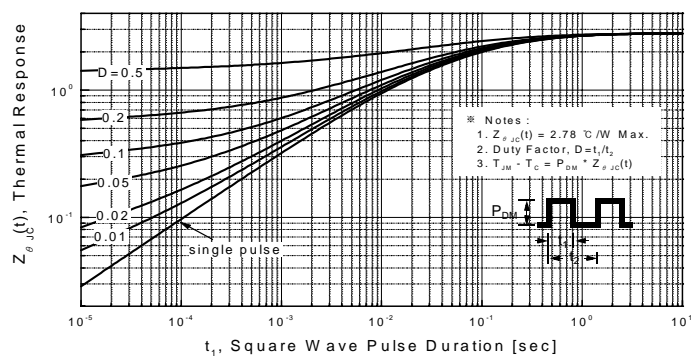
**Figure 8. On-Resistance Variation vs. Temperature**



**Figure 9. Maximum Safe Operating Area**

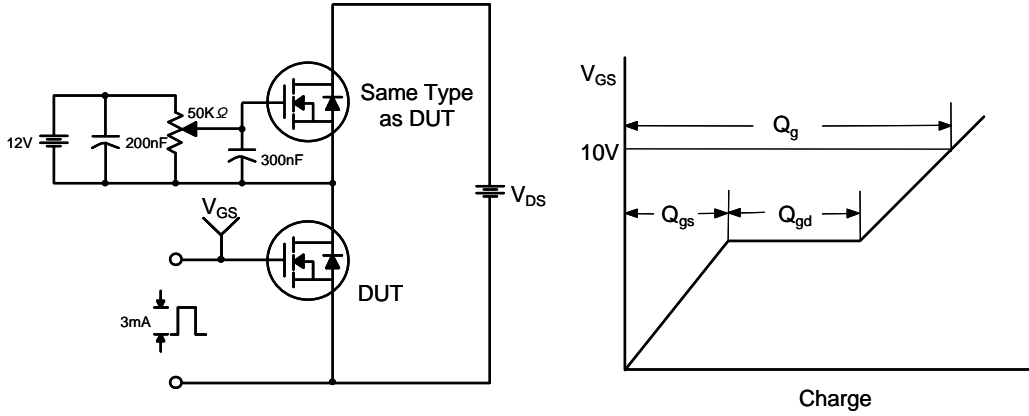


**Figure 10. Maximum Drain Current vs. Case Temperature**

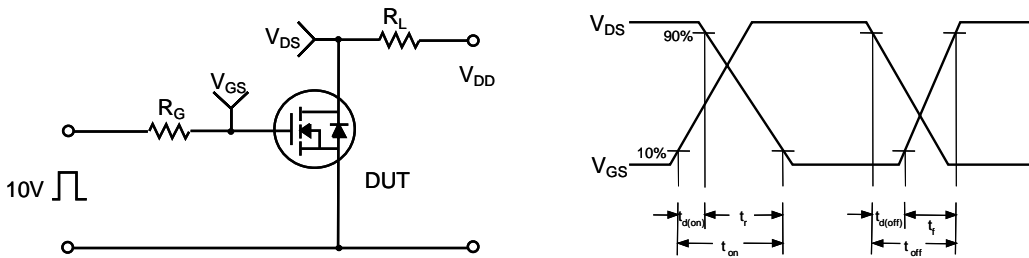


**Figure 11. Transient Thermal Response Curve**

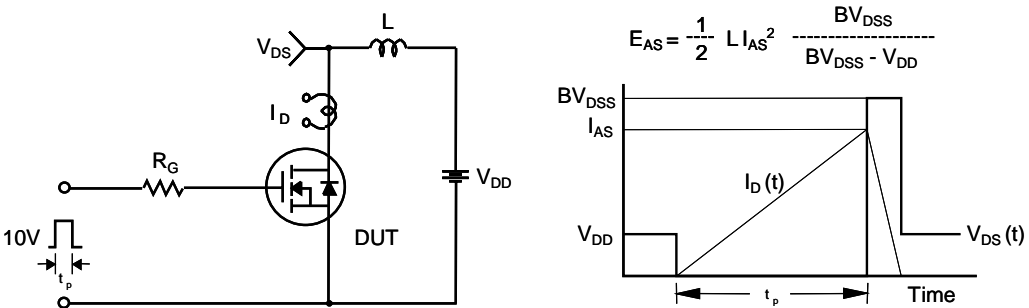
Gate Charge Test Circuit & Waveform



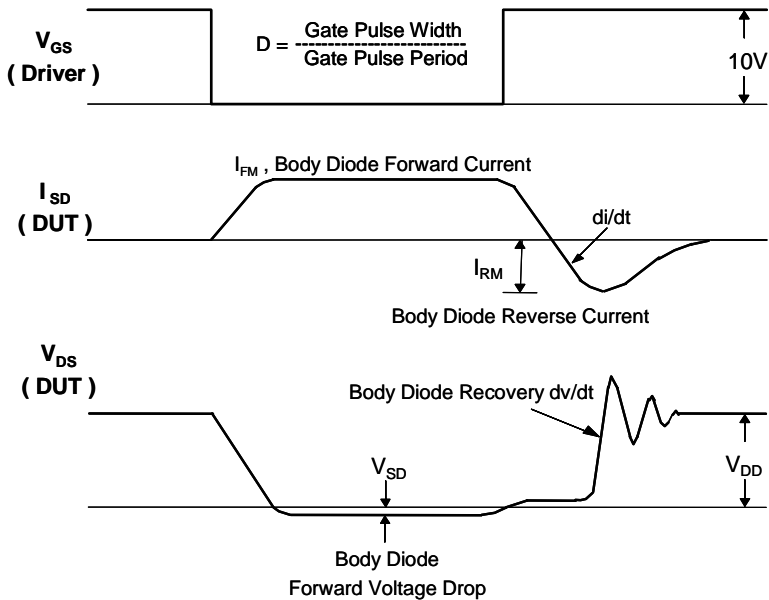
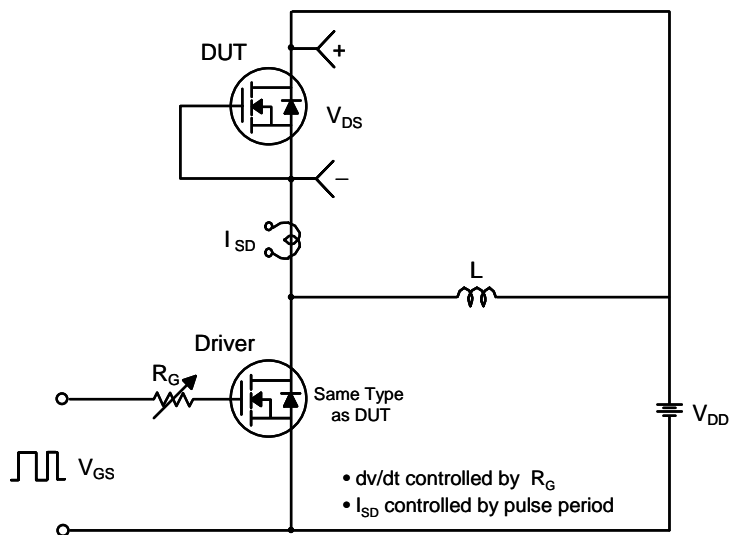
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

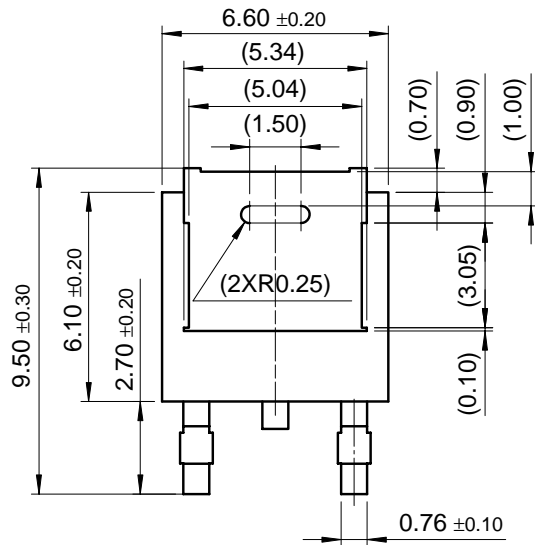
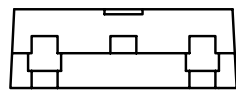
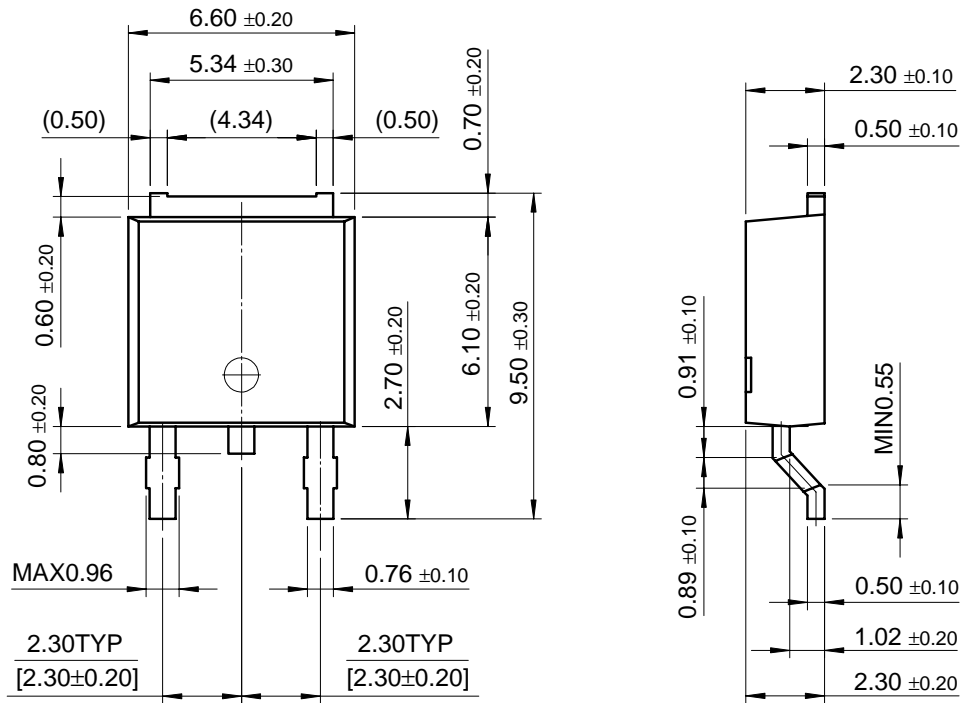


Peak Diode Recovery dv/dt Test Circuit & Waveforms



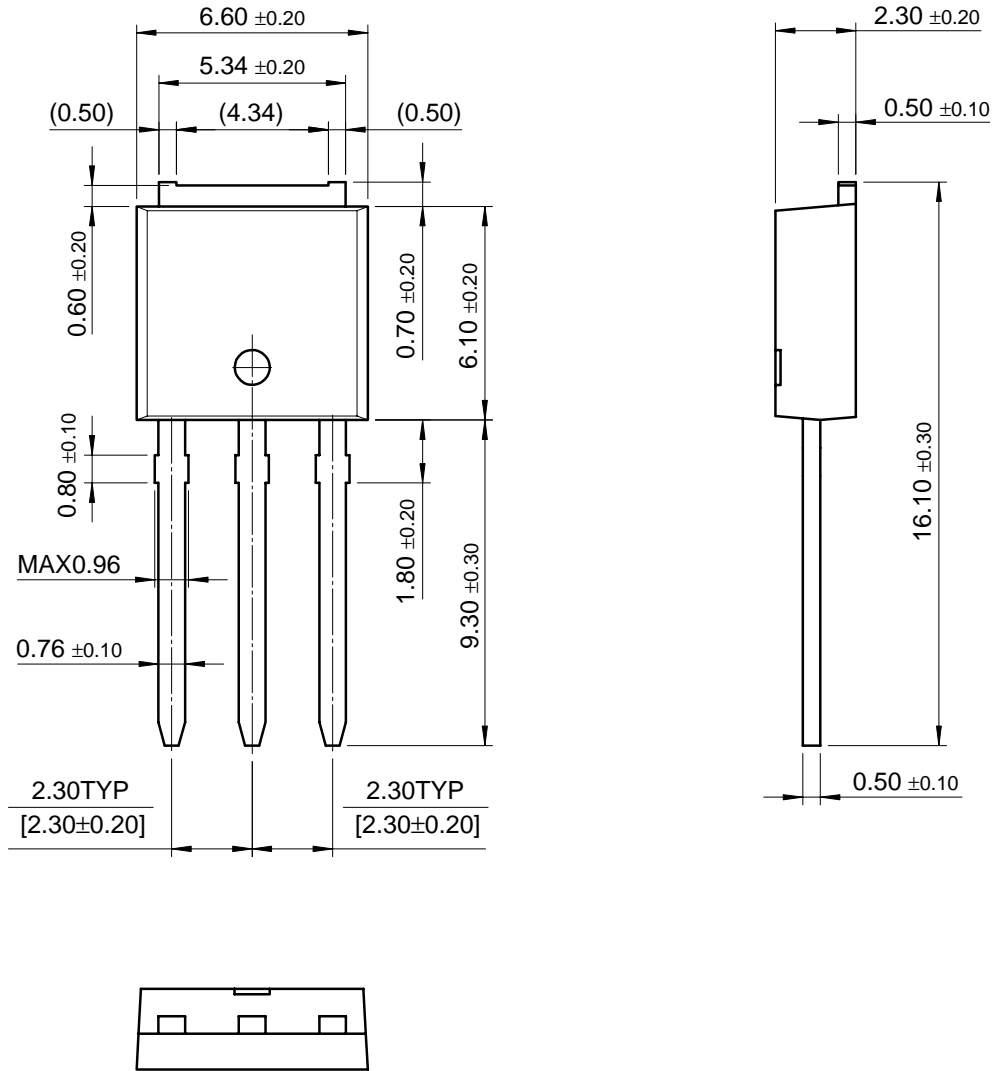
Package Dimensions

DPAK



Package Dimensions (Continued)

# IPAK



FQD2N60 / FQU2N60



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