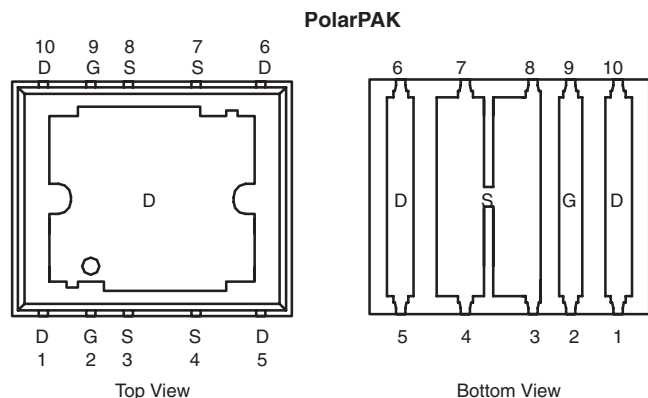


## N-Channel 200-V (D-S) MOSFET

PRODUCT SUMMARY			
V <sub>DS</sub> (V)	R <sub>DS(on)</sub> (Ω)	I <sub>D</sub> (A) <sup>a</sup>	Q <sub>g</sub> (Typ.)
200	0.130 at V <sub>GS</sub> = 10 V	18.3	27 nC

[Package Drawing](http://www.vishay.com/doc?68798)  
<http://www.vishay.com/doc?68798>



Top surface is connected to pins 1, 5, 6, and 10

Ordering Information: SiE836DF-T1-E3 (Lead (Pb)-free)

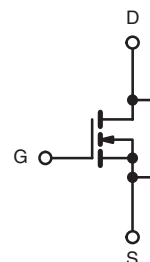
### FEATURES

- TrenchFET<sup>®</sup> Power MOSFET
- Ultra Low Thermal Resistance Using Top-Exposed PolarPAK<sup>®</sup> Package for Double-Sided Cooling
- Leadframe-Based New Encapsulated Package - Die Not Exposed
- Low Q<sub>gd</sub>/Q<sub>gs</sub> Ratio Helps Prevent Shoot-Through
- 100 % R<sub>g</sub> and UIS Tested



### APPLICATIONS

- Primary Side Switch



N-Channel MOSFET

[For Related Documents](http://www.vishay.com/doc?68742)  
<http://www.vishay.com/doc?68742>

ABSOLUTE MAXIMUM RATINGS T <sub>A</sub> = 25 °C, unless otherwise noted				
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V <sub>DS</sub>	200	V	
Gate-Source Voltage	V <sub>GS</sub>	± 30		
Continuous Drain Current (T <sub>J</sub> = 150 °C)	I <sub>D</sub>	T <sub>C</sub> = 25 °C	18.3	A
		T <sub>C</sub> = 70 °C	14.6	
		T <sub>A</sub> = 25 °C	4.1 <sup>b, c</sup>	
		T <sub>A</sub> = 70 °C	3.3 <sup>b, c</sup>	
Pulsed Drain Current	I <sub>DM</sub>	15		
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C	14.6 <sup>a</sup>	
		T <sub>A</sub> = 25 °C	4.3 <sup>b, c</sup>	
Single Pulse Avalanche Current	I <sub>AS</sub>	5		
Avalanche Energy	E <sub>AS</sub>	1.25	mJ	
Maximum Power Dissipation	P <sub>D</sub>	T <sub>C</sub> = 25 °C	104	W
		T <sub>C</sub> = 70 °C	66	
		T <sub>A</sub> = 25 °C	5.2 <sup>b, c</sup>	
		T <sub>A</sub> = 70 °C	3.3 <sup>b, c</sup>	
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150		
Soldering Recommendations (Peak Temperature) <sup>d, e</sup>		260	°C	

Notes:

- T<sub>C</sub> = 25 °C.
- Surface Mounted on 1" x 1" FR4 board.
- t = 10 s.
- See Solder Profile (<http://www.vishay.com/doc?73257>). The PolarPAK is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

**THERMAL RESISTANCE RATINGS**

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>a, b</sup>	$t \leq 10$ s	$R_{thJA}$	20	24	°C/W
Maximum Junction-to-Case (Drain Top) <sup>a</sup>	Steady State	$R_{thJC}$ (Drain)	1	1.2	
Maximum Junction-to-Case (Source) <sup>a, c</sup>		$R_{thJC}$ (Source)	2.8	3.4	

Notes:

- a. Surface Mounted on 1" x 1" FR4 board.  
b. Maximum under Steady State conditions is 68 °C/W.  
c. Measured at source pin (on the side of the package).

**SPECIFICATIONS**  $T_J = 25$  °C, unless otherwise noted

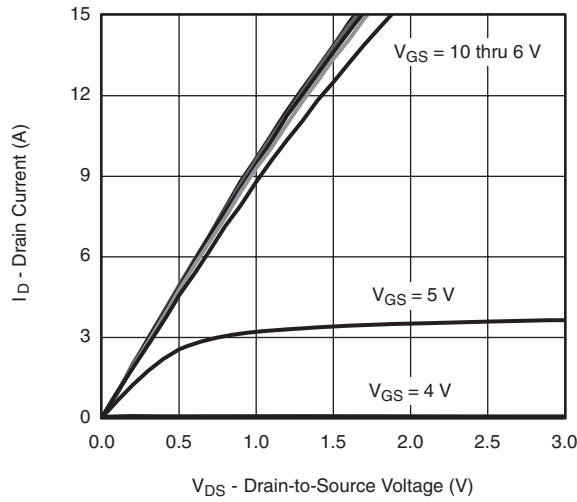
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0$ V, $I_D = 250$ $\mu$ A	200			V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250$ $\mu$ A		7		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			- 10		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 250$ $\mu$ A	2.5		4.5	V
Gate-Source Leakage	$I_{GSS}$	$V_{DS} = 0$ V, $V_{GS} = \pm 30$ V			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 200$ V, $V_{GS} = 0$ V			1	$\mu$ A
		$V_{DS} = 200$ V, $V_{GS} = 0$ V, $T_J = 55$ °C			10	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \geq 5$ V, $V_{GS} = 10$ V	15			A
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = 10$ V, $I_D = 4.1$ A		0.105	0.130	$\Omega$
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 15$ V, $I_D = 4.1$ A		14		S
<b>Dynamic<sup>b</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = 100$ V, $V_{GS} = 0$ V, $f = 1$ MHz		1200		pF
Output Capacitance	$C_{oss}$			70		
Reverse Transfer Capacitance	$C_{rss}$			35		
Total Gate Charge	$Q_g$	$V_{DS} = 100$ V, $V_{GS} = 10$ V, $I_D = 4.1$ A		27	41	nC
Gate-Source Charge	$Q_{gs}$			7		
Gate-Drain Charge	$Q_{gd}$			10		
Gate Resistance	$R_g$	$f = 1$ MHz		1.0	2	$\Omega$
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 100$ V, $R_L = 30$ $\Omega$ $I_D \cong 3.3$ A, $V_{GEN} = 10$ V, $R_g = 1$ $\Omega$		15	25	ns
Rise Time	$t_r$			10	15	
Turn-Off Delay Time	$t_{d(off)}$			20	30	
Fall Time	$t_f$			10	15	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	$I_S$	$T_C = 25$ °C			18.3	A
Pulse Diode Forward Current <sup>a</sup>	$I_{SM}$				15	
Body Diode Voltage	$V_{SD}$	$I_S = 3.3$ A		0.8	1.2	V
Body Diode Reverse Recovery Time	$t_{rr}$	$I_F = 3.3$ A, $di/dt = 100$ A/ $\mu$ s, $T_J = 25$ °C		90	135	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			270	405	nC
Reverse Recovery Fall Time	$t_a$			53		ns
Reverse Recovery Rise Time	$t_b$			37		

Notes:

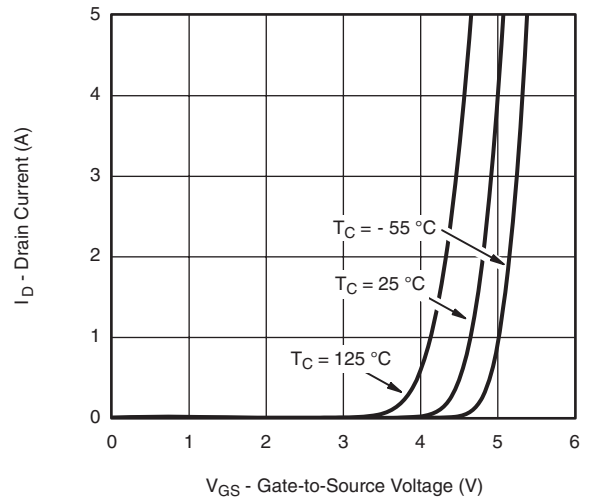
- a. Pulse test; pulse width  $\leq 300$   $\mu$ s, duty cycle  $\leq 2$  %  
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

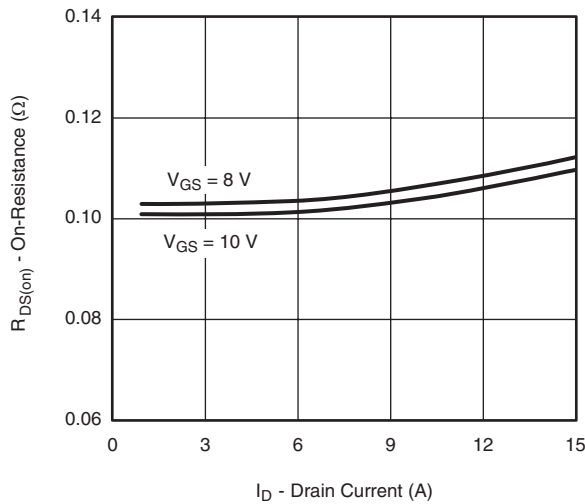
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



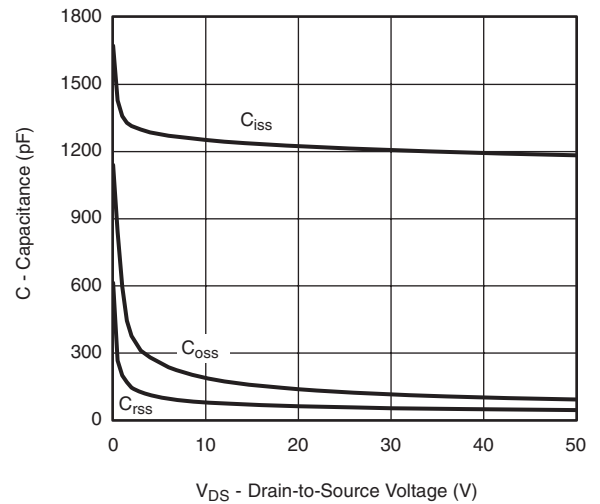
**Output Characteristics**



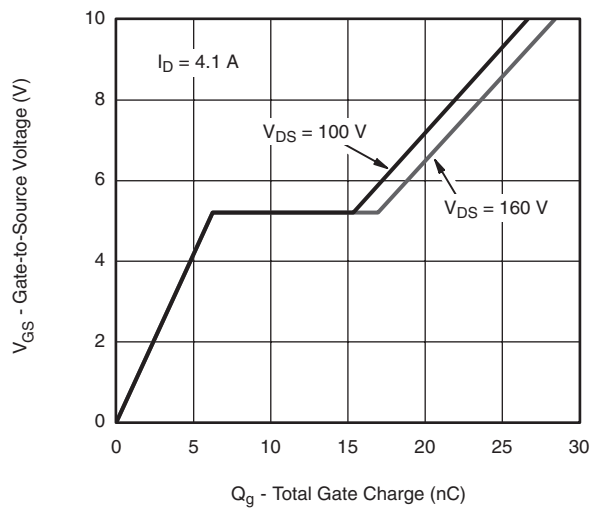
**Transfer Characteristics**



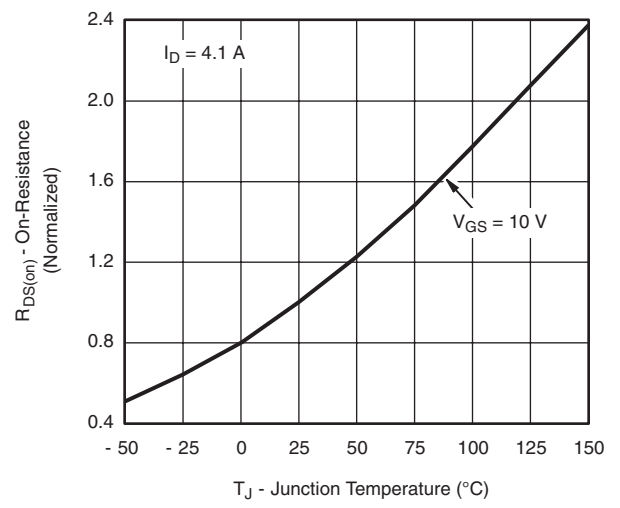
**On-Resistance vs. Drain Current**



**Capacitance**

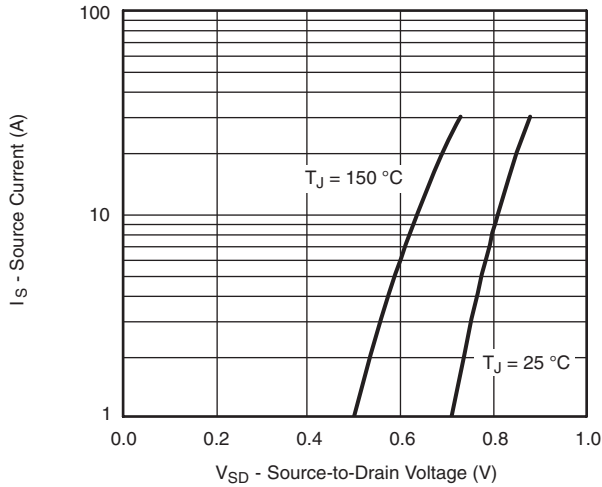


**Gate Charge**

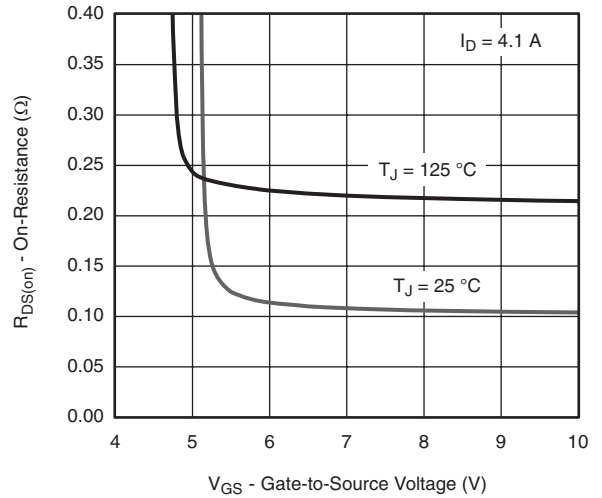


**On-Resistance vs. Junction Temperature**

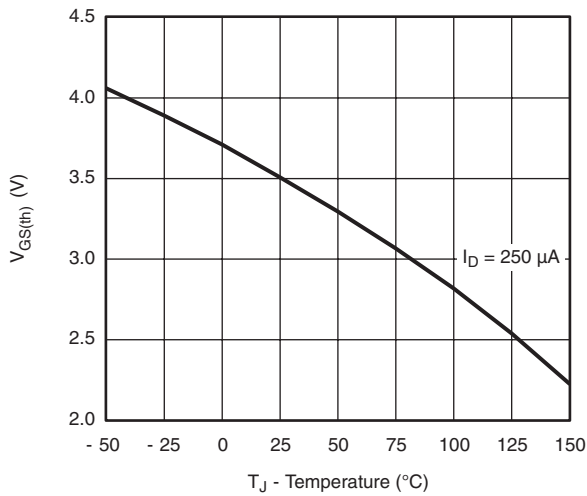
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



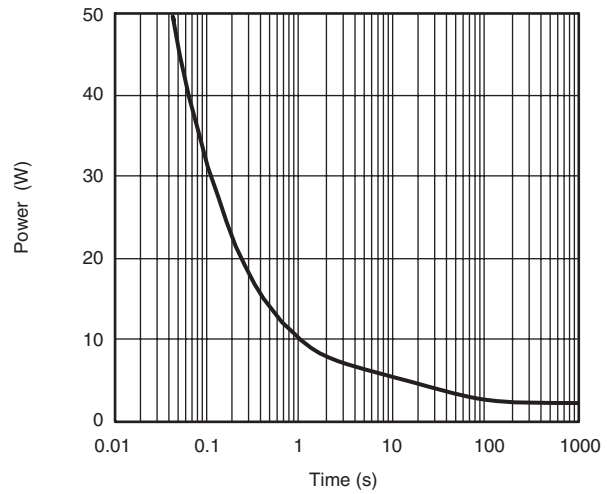
Source-Drain Diode Forward Voltage



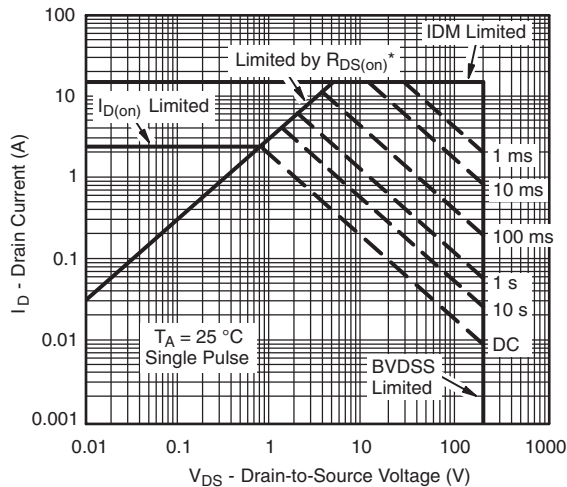
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



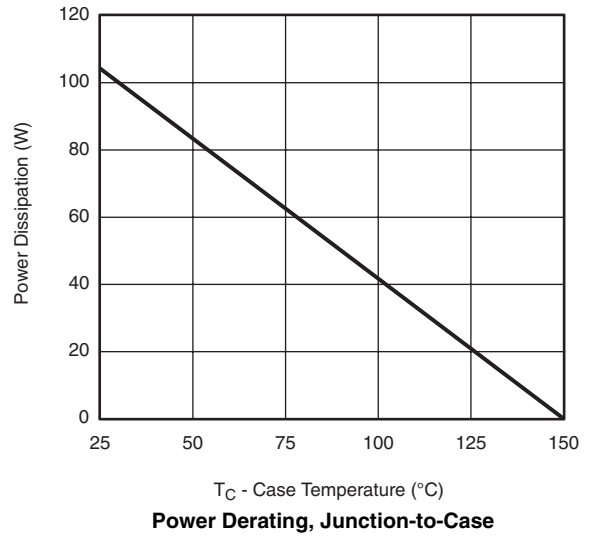
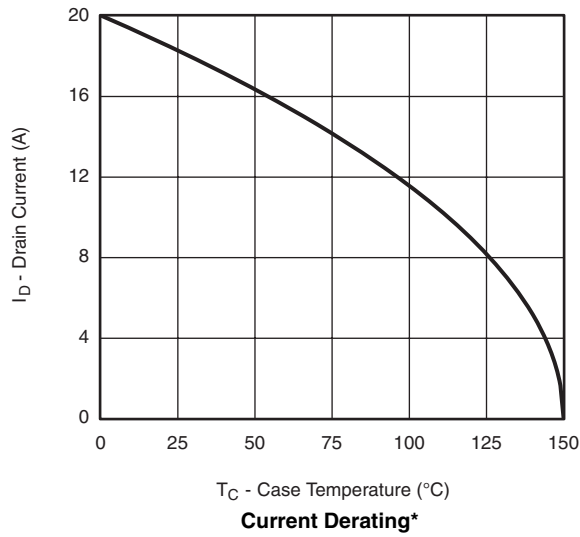
Single Pulse Power, Junction-to-Ambient



\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

Safe Operating Area, Junction-to-Ambient

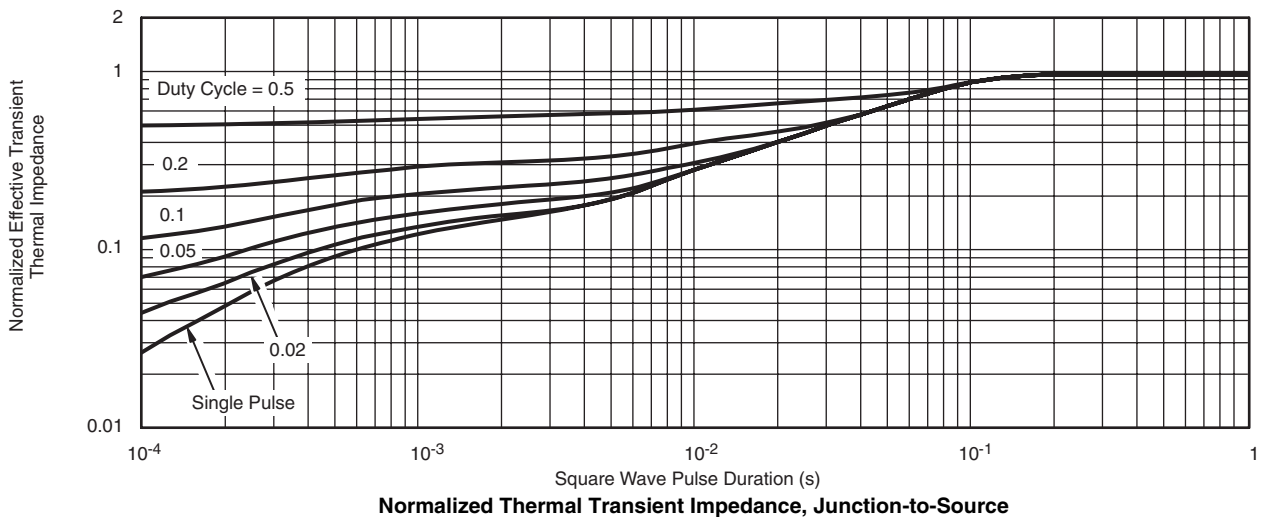
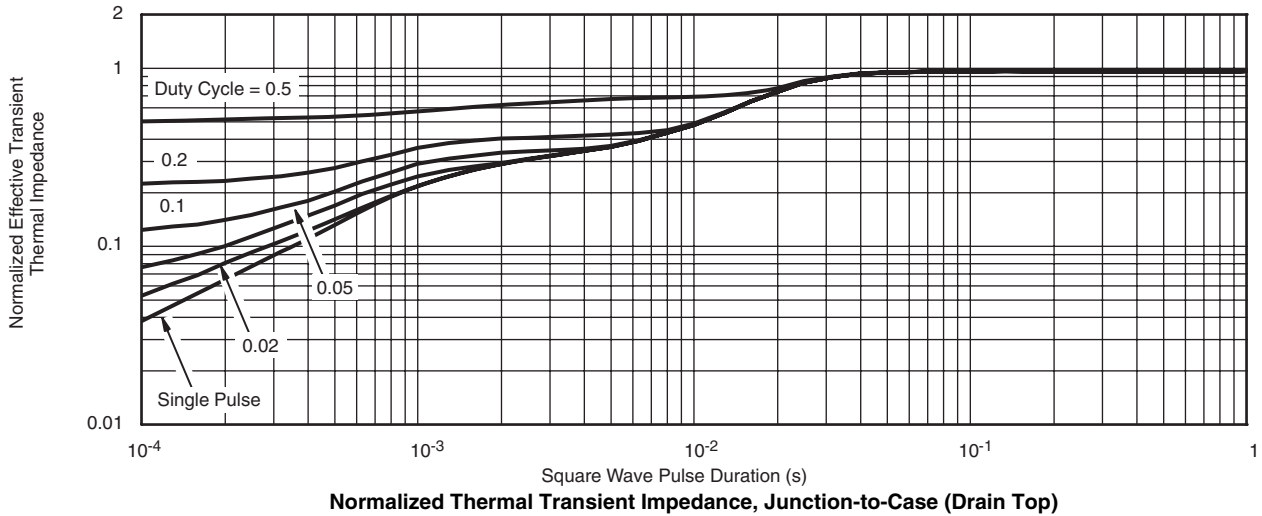
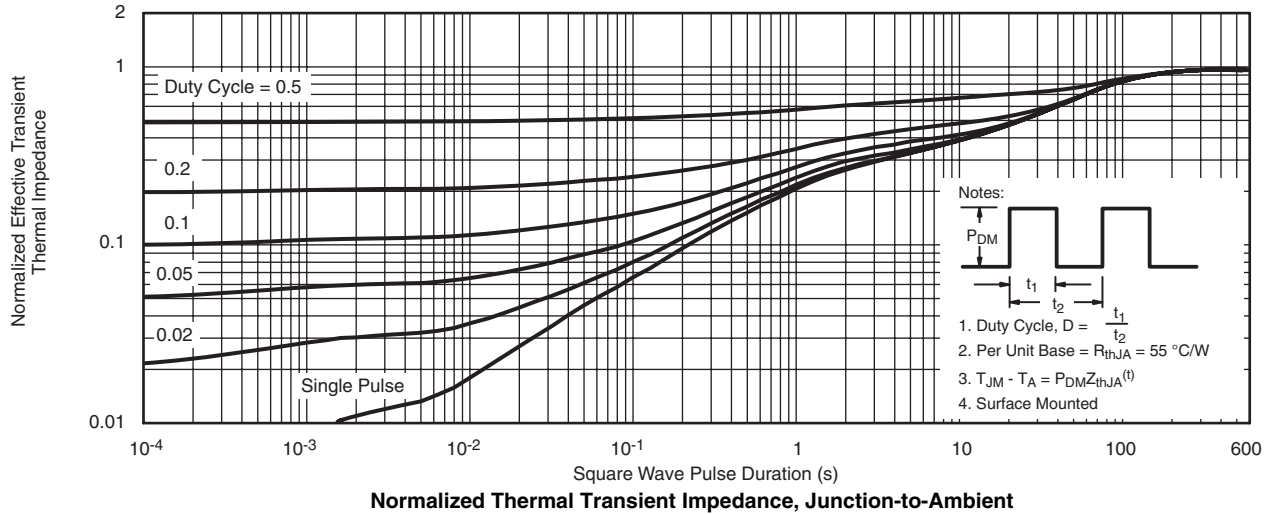
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



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