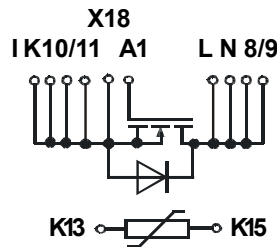


Power MOSFET in ECO-PAC 2

Single MOSFET Die

PSMG 150/01*



$V_{DSS} = 100 \text{ V}$
 $I_{D25} = 165 \text{ A}$
 $R_{DS(on)} = 8 \text{ m}\Omega$
 $t_{rr} < 250 \text{ ns}$

Preliminary Data Sheet

*NTC optional

MOSFET

Symbol	Test Conditions	Maximum Ratings
V_{DSS}	$T_J = 25^\circ\text{C}$ to 150°C	100 V
V_{DGR}	$T_J = 25^\circ\text{C}$ to 150°C ; $R_{GS} = 1 \text{ M}\Omega$	100 V
V_{GS}	Continuous	± 20 V
V_{GSM}	Transient	± 30 V
I_{D25}	$T_C = 25^\circ\text{C}$ (MOSFET chip capability)	165 A
$I_{D(RMS)}$	External lead (current limit)	76 A
I_{DM}	$T_C = 25^\circ\text{C}$ ¹⁾	720 A
I_{AR}	$T_C = 25^\circ\text{C}$	180 A
E_{AR}	$T_C = 25^\circ\text{C}$	60 mJ
E_{AS}	$T_C = 25^\circ\text{C}$	3 J
dv/dt	$I_S \leq I_{DM}$, $di/dt \leq 100 \text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DSS}$ $T_J \leq 150^\circ\text{C}$, $R_G = 2 \Omega$	5 V/ns
P_D	$T_C = 25^\circ\text{C}$	400 W

Symbol	Test Conditions	Characteristic Values ($T_J = 25^\circ\text{C}$, unless otherwise specified)		
		min.	typ.	max.
V_{DSS}	$V_{GS} = 0 \text{ V}$, $I_D = 3 \text{ mA}$	100		V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 8 \text{ mA}$	2.0		V
I_{GSS}	$V_{GS} = \pm 20 \text{ V}$, $V_{DS} = 0$			± 100 nA
I_{DSS}	$V_{DS} = V_{DSS}$; $T_J = 25^\circ\text{C}$ $V_{GS} = 0 \text{ V}$; $T_J = 125^\circ\text{C}$			100 μA 2 mA
$R_{DS(on)}$	$V_{GS} = 10 \text{ V}$, $I_D = 90 \text{ A}$ ¹⁾			8 m Ω
g_{fs}	$V_{DS} = 10 \text{ V}$, $I_D = 90 \text{ A}$ ²⁾	60	90	S
C_{iss} C_{oss} C_{rss}	$V_{GS} = 0 \text{ V}$, $V_{DS} = 25 \text{ V}$, $f = 1 \text{ MHz}$		9400	pF
			3200	pF
			1660	pF
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	$V_{GS} = 10 \text{ V}$, $V_{DS} = 0.5 \cdot V_{DSS}$, $I_D = 90 \text{ A}$ $R_G = 1 \Omega$ (External)		50	ns
			90	ns
			140	ns
			65	ns
$Q_{g(on)}$ Q_{gs} Q_{gd}	$V_{GS} = 10 \text{ V}$, $V_{DS} = 0.5 \cdot V_{DSS}$, $I_D = 90 \text{ A}$		400	nC
			65	nC
			220	nC
R_{thJC} R_{thCK}	with heatsink compound (0.42 K/m.K; 50 μm)		0.2	0.30 K/W K/W



Features

- Silicon chip on Direct-Copper-Bond substrate
- High power dissipation
- Isolated mounting surface
- 3000V electrical isolation
- Low drain to tab capacitance (< 25pF)
- Low $R_{DS(on)}$ HDMOS™ process
- Rugged polysilicon gate cell structure
- Unclamped Inductive Switching (UIS) rated
- Fast intrinsic Rectifier
- UL certified, E 148688

Applications

- DC-DC converters
- Battery chargers
- Switched-mode and resonant-mode power supplies
- DC choppers
- AC motor control

Advantages

- Easy assembly
- Space savings
- High power density

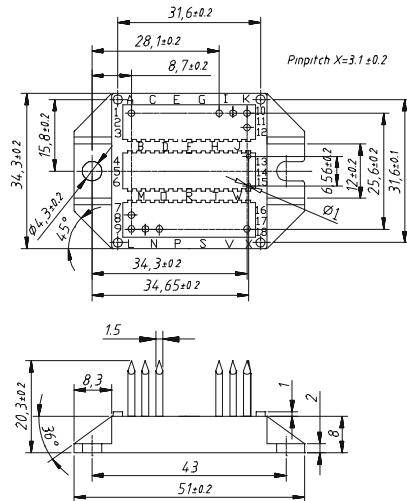
Caution: These Devices are sensitive to electrostatic discharge. Users should observe proper ESD handling precautions.

Source-Drain Diode

Symbol	Test Conditions	Characteristic Values ($T_J = 25^\circ\text{C}$, unless otherwise specified)		
		min.	typ.	max.
I_S	$V_{GS} = 0\text{ V}$			180 A
I_{SM}	Repetitive; pulse width limited by T_{JM}			720 A
V_{SD}	$I_F = 100\text{ A}$, $V_{GS} = 0\text{ V}$, ¹⁾			1.5 V
t_{rr}	$I_F = 50\text{ A}$, $-di/dt = 100\text{ A}/\mu\text{s}$, $V_R = 100\text{ V}$			250 ns
Q_{RM}		1.1		μC
I_{RM}		13		A

Note: ¹⁾ Pulse width limited by T_{JM}
²⁾ Pulse test, $t \leq 300\ \mu\text{s}$, duty cycle $d \leq 2\%$

Package style and outline Dimensions in mm (1mm = 0.0394")



Temperature Sensor NTC

Symbol	Conditions	Characteristic Values		
		min.	typ.	max.
R_{25}	$T = 25^\circ\text{C}$	4.75	5.0	5.25 k Ω
$B_{25/50}$			3375	K

Module

Symbol	Conditions	Maximum Ratings	
T_{VJ}		-40...+150	$^\circ\text{C}$
T_{stg}		-40...+125	$^\circ\text{C}$
V_{ISOL}	$I_{ISOL} \leq 1\text{ mA}$; 50/60 Hz; $t = 1\text{ s}$	3600	V~
M_d	Mounting torque (M4)	1.5 - 2.0	Nm
		14 - 18	lb.in.
a	Max. allowable acceleration	50	m/s^2

Symbol	Conditions	Characteristic Values		
		min.	typ.	max.
d_s	Creepage distance on surface (Pin to heatsink)	11.2		mm
d_A	Strike distance in air (Pin to heatsink)	11.2		mm
Weight		24		g

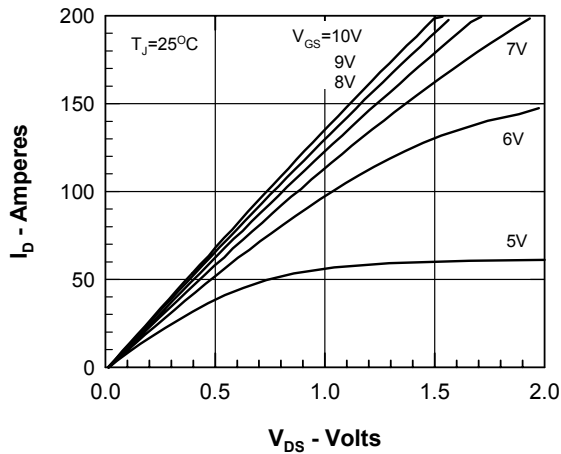


Figure 1. Output Characteristics at 25°C

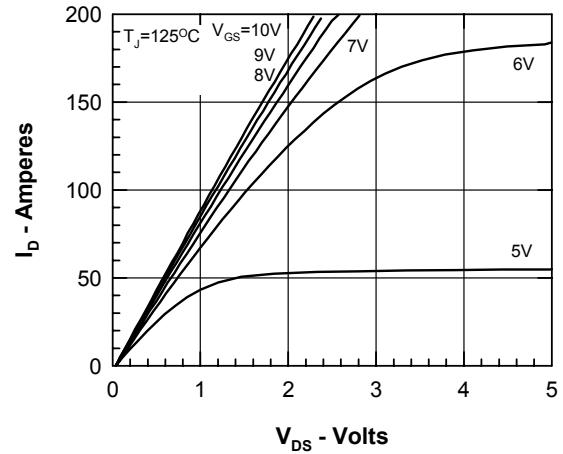


Figure 2. Output Characteristics at 125°C

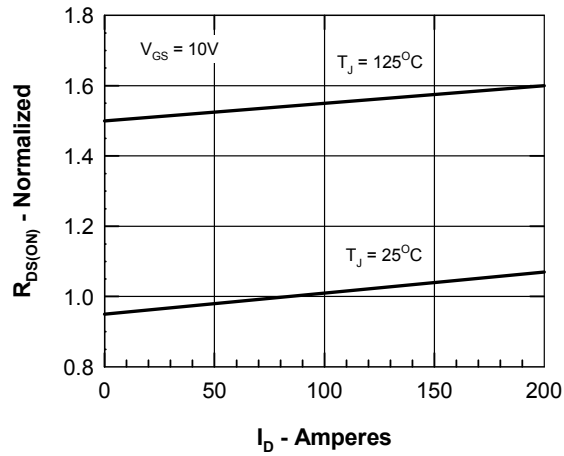


Figure 3. $R_{DS(on)}$ normalized to 15A/25°C vs. I_D

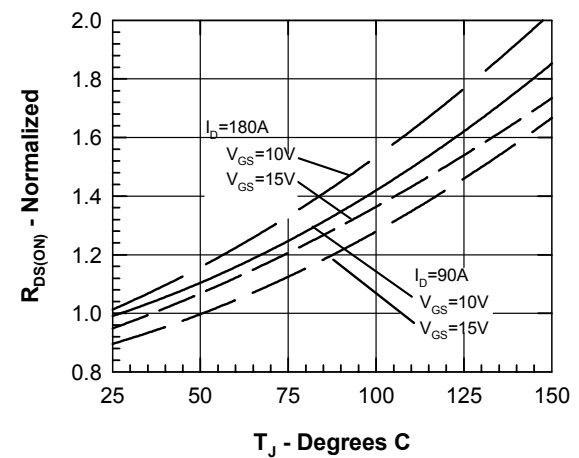


Figure 4. $R_{DS(on)}$ normalized to 15A/25°C vs. T_J

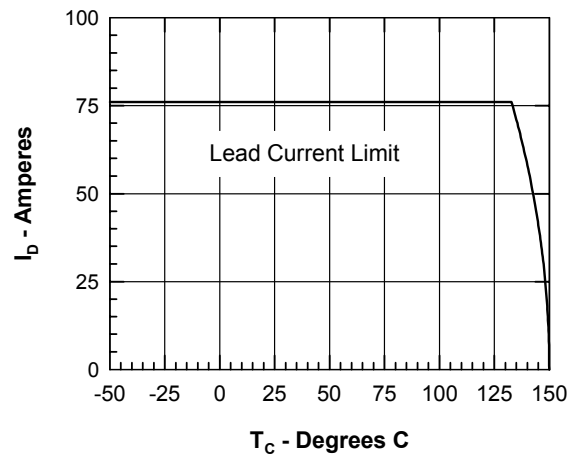


Figure 5. Drain Current vs. Case Temperature

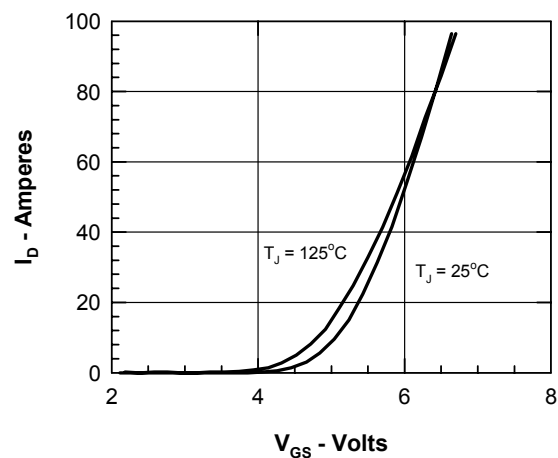


Figure 6. Admittance Curves

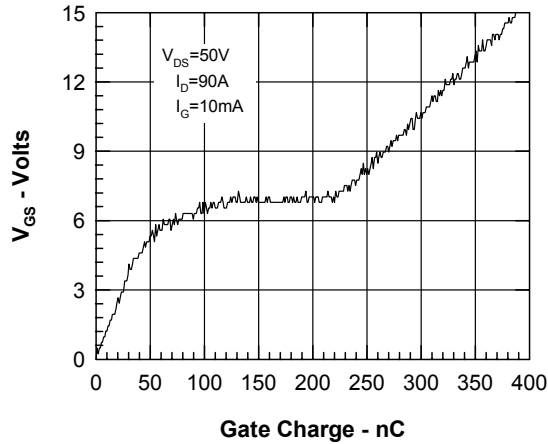


Figure 7. Gate Charge

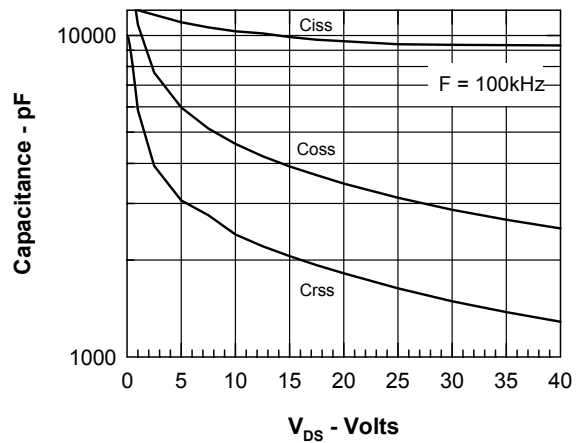


Figure 8. Capacitance Curves

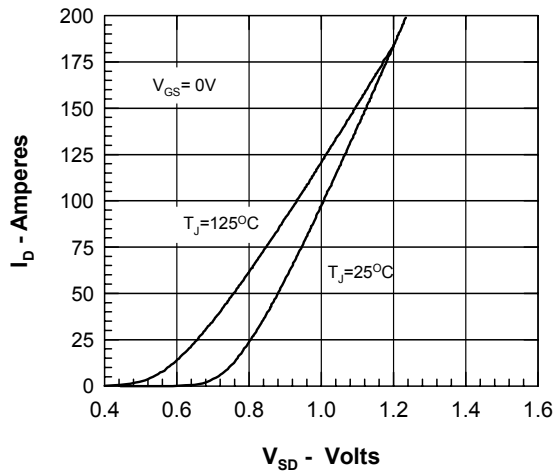


Figure 9. Forward Voltage Drop of the Intrinsic Diode

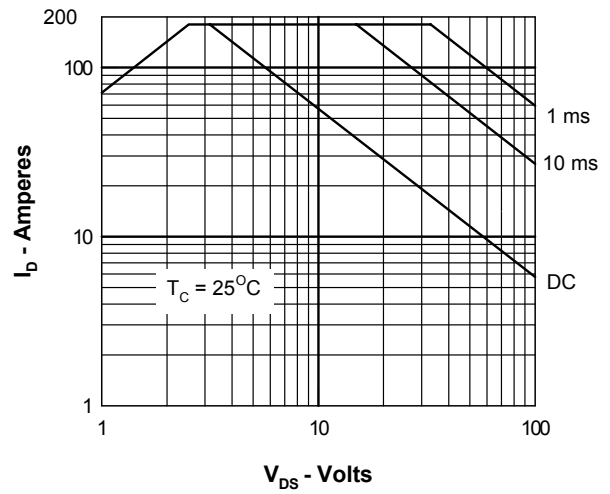


Figure 10. Forward Bias Safe Operating Area

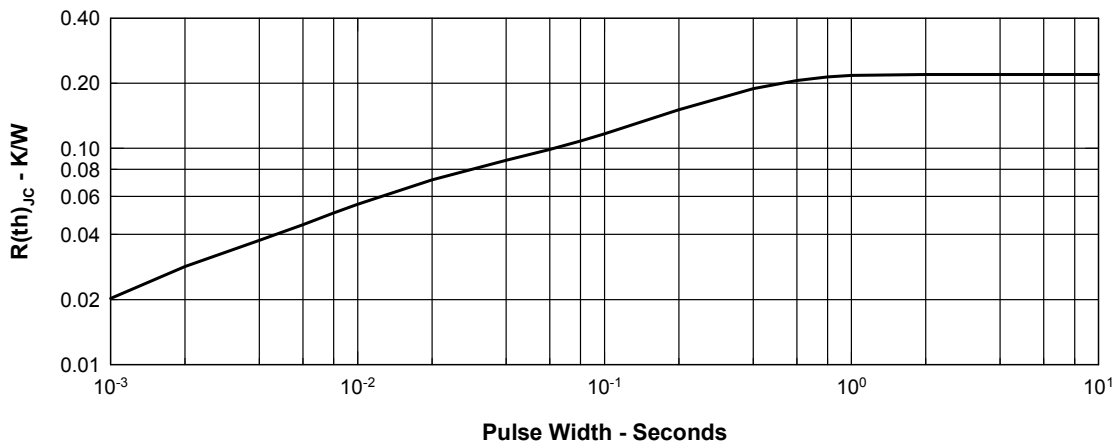


Figure 11. Typical Transient Thermal Resistance