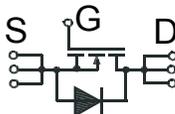


MOSFET Module

PSMG 60/08

$$\begin{aligned}
 V_{DSS} &= 800 \text{ V} \\
 I_{D25} &= 60 \text{ A} \\
 R_{DS(on)} &= 0.12 \Omega \\
 t_{rr} &\leq 250 \text{ ns}
 \end{aligned}$$

Preliminary Data Sheet



MOSFET (data related to single chip)

Symbol	Test Conditions	Maximum Ratings
V_{DSS}	$T_J = 25 \text{ }^\circ\text{C}$ to $150 \text{ }^\circ\text{C}$	800 V
V_{DGR}	$T_J = 25 \text{ }^\circ\text{C}$ to $150 \text{ }^\circ\text{C}$, $R_{GS} = 1 \text{ M}\Omega$	800 V
V_{GS}	continuous	± 20 V
V_{GSM}	transient	± 30 V
I_{D25}	$T_{Case} = 25 \text{ }^\circ\text{C}$	60 A
I_{DM}	$T_{Case} = 25 \text{ }^\circ\text{C}$, pulse width limited by T_{JM}	240 A
I_{AR}		60 A
E_{AR}	$T_C = 25 \text{ }^\circ\text{C}$	64 mJ
E_{AS}	$T_C = 25 \text{ }^\circ\text{C}$	3 J
dv/dt	$I_S \leq I_{DM}$, $di/dt \leq 100 \text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DSS}$, $T_J \leq 150 \text{ }^\circ\text{C}$, $R_G = 2 \Omega$	5 V/ns
P_D	$T_{Case} = 25 \text{ }^\circ\text{C}$	1200 W
T_J		$-55 \dots +150 \text{ }^\circ\text{C}$
T_{JM}		$+150 \text{ }^\circ\text{C}$
T_{stg}		$-55 \dots +150 \text{ }^\circ\text{C}$
V_{ISOL}	50/60 Hz, RMS $t = 1 \text{ min.}$	2500 V~
V_{ISOL}	$I_{ISOL} \leq 1 \text{ mA}$ $t = 1 \text{ s}$	3000 V~
M_d	Mounting torque (M4)	1.5 Nm 14 lb.in.
a	max. allowed acceleration	50 m/s^2
Weight		26 g

Symbol	Test Conditions	Characteristic Values
$(T_J = 25 \text{ }^\circ\text{C}$, unless otherwise specified)		
V_{DSS}	$V_{GS} = 0 \text{ V}$, $I_D = 3 \text{ mA}$	min. 800 V
	V_{DSS} temperature coefficient	typ. 0.096 %/K
$V_{GS(th)}$	$V_{GS} = V_{DS}$, $I_D = 8 \text{ mA}$	min. 3.0 V
		max. 5.0 V
	$V_{GS(th)}$ temperature coefficient	typ. -0.214 %/K
I_{GSS}	$V_{DS} = 0 \text{ V}$, $V_{GS} = \pm 20 \text{ V}$	max. $\pm 200 \text{ nA}$
I_{DSS}	$V_{DS} = V_{DSS}$, $T_J = 25 \text{ }^\circ\text{C}$	max. 100 μA
	$V_{GS} = 0 \text{ V}$, $T_J = 125 \text{ }^\circ\text{C}$	max. 2 mA
$R_{DS(on)}$	$V_{GS} = 10 \text{ V}$, $I_D = 0.5 \cdot I_{D25}$ pulse test, $t \leq 300 \mu\text{s}$, duty cycle $d \leq 2 \%$	max. 0.12 Ω

ATTENTION: All given data are derived from similar modules or estimated from chip data.



Typical picture; changes of the pin configuration is reserved.

Features

- Package with DCB ceramic base plate
- Isolation voltage 3000 V~
- Planar glass passivated chips
- Low forward voltage drop
- Leads suitable for PC board soldering
- Low $R_{DS(on)}$ HDMOS™ process
- Fast intrinsic Rectifier
- UL registered, E 148688

Applications

- DC-DC converters
- Battery chargers
- Switched-mode and resonant-mode power supplies
- DC choppers
- Temperature and lighting controls

Advantages

- Easy to mount with two screws
- Space and weight savings
- Improved temperature and power cycling capability
- High power density
- Small and light weight

Caution: These devices are sensitive to electrostatic discharge. Users should observe proper ESD handling precautions.

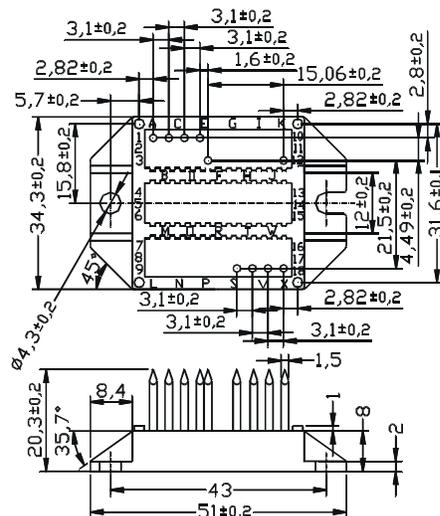
Symbol	Test Conditions	Characteristic Values		
($T_J = 25\text{ }^\circ\text{C}$, unless otherwise specified)				
C_{iss}	$V_{GS} = 0\text{ V}$,	typ.	15000	pF
C_{oss}	$V_{DS} = 25\text{ V}$,	typ.	1840	pF
C_{rss}	$f = 1\text{ MHz}$	typ.	440	pF
$t_{d(on)}$	$V_{GS} = 10\text{ V}$,	typ.	45	ns
t_r	$V_{DS} = 0.5 \cdot V_{DSS}$,	typ.	45	ns
$t_{d(off)}$	$I_D = 0.5 \cdot I_{D25}$	typ.	100	ns
t_f	$R_G = 1\ \Omega$ (External)	typ.	40	ns
R_{thJC}			0.45	K/W
R_{thCK}			0.60	K/W

Source-Drain Diode

Symbol	Test Conditions	Characteristic Values		
($T_J = 25\text{ }^\circ\text{C}$, unless otherwise specified)				
I_S	$V_{GS} = 0\text{ V}$	max.	34	A
I_{SM}	repetitive pulse width limited by T_{JM}	max.	136	A
V_{SD}	$I_F = I_S$, $V_{GS} = 0\text{ V}$ pulse test, $t \leq 300\ \mu\text{s}$, duty cycle $d \leq 2\%$	max.	1.5	V
t_{rr}	$I_F = I_S$, $T_J = 25\text{ }^\circ\text{C}$ max.	max.	250	ns
	$T_J = 125\text{ }^\circ\text{C}$ max.	max.	400	ns
Q_{RM}	$-di/dt = 100\text{ A}/\mu\text{s}$, $T_J = 25\text{ }^\circ\text{C}$	typ.	1.4	μC
I_{RM}	$V_R = 100\text{ V}$	typ.	10	A

Package style and preliminary outline

Dimensions in mm (1mm = 0.0394")



Characteristic pin configuration; changes of the pin configuration is reserved.

ATTENTION: All given data are derived from similar modules or estimated from chip data.