

MITSUBISHI SEMICONDUCTOR &lt;TRANSISTOR ARRAY&gt;

**M63826P/FP/GP**

7-UNIT 500mA DARLINGTON TRANSISTOR-ARRAY WITH CLAMP DIODE

**DESCRIPTION**

M63826P, M63826FP and M63826GP are seven-circuit Darlington transistor arrays with clamping diodes. The circuits are made of NPN transistors. Both the semi-conductor integrated circuits perform high-current driving with extremely low input-current supply.

Production lineup has been newly expanded with the addition of 225mil (GP) package.

M63826P and M63826FP have the same pin connection as M54526P and M54526FP. (Compatible with M54526P and M54526FP) More over, the features of M63826P and M63826FP are equal or superior to those of M54526P and M54526FP.

**FEATURES**

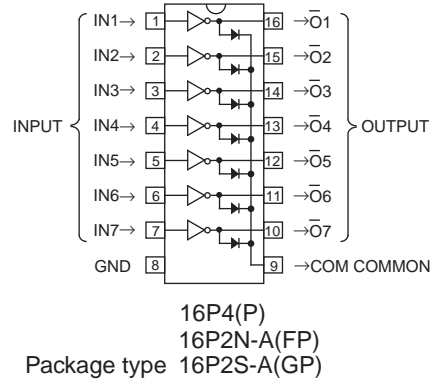
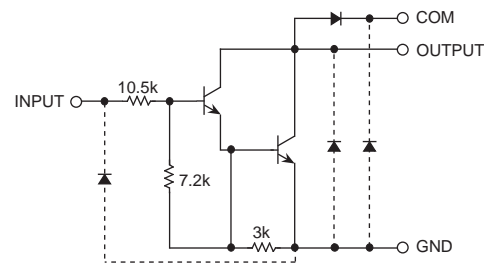
- Three package configurations (P, FP and GP)
- Pin connection Compatible with M54526P and M54526FP
- High breakdown voltage ( $BV_{CEO} \geq 50V$ )
- High-current driving ( $I_{C(max)} = 500mA$ )
- With clamping diodes
- Driving available with PMOS IC output of 8-18V
- Wide operating temperature range ( $T_a = -40$  to  $+85^\circ C$ )

**APPLICATION**

Drives of relays and printers, digit drives of indication elements (LEDs and lamps), and MOS-bipolar logic IC interfaces

**FUNCTION**

The M63826P, M63826FP and M63826GP each have seven circuits consisting of NPN Darlington transistors. These ICs have resistance of  $10.5k\Omega$  between input transistor bases and input pins. A spike-killer clamping diode is provided between each output pin (collector) and COM pin (pin 9). The output transistor emitters are all connected to the GND pin (pin 8). The collector current is 500mA maximum. Collector-emitter supply voltage is 50V maximum. The M63826FP and M63826GP is enclosed in molded small flat package, enabling space-saving design.

**PIN CONFIGURATION****CIRCUIT DIAGRAM**

The seven circuits share the COM and GND

The diode, indicated with the dotted line, is parasitic, and cannot be used.

Unit :  $\Omega$

**ABSOLUTE MAXIMUM RATINGS** (Unless otherwise noted,  $T_a = -40 \sim +85^\circ C$ )

Symbol	Parameter	Conditions	Ratings	Unit
$V_{CEO}$	Collector-emitter voltage	Output, H	-0.5 ~ +50	V
$I_C$	Collector current	Current per circuit output, L	500	mA
$V_i$	Input voltage		-0.5 ~ +30	V
$I_F$	Clamping diode forward current		500	mA
$V_R$	Clamping diode reverse voltage		50	V
$P_d$	Power dissipation	$T_a = 25^\circ C$ , when mounted on board	1.47(P)/1.00(FP)/0.80(GP)	W
$T_{opr}$	Operating temperature		-40 ~ +85	$^\circ C$
$T_{stg}$	Storage temperature		-55 ~ +125	$^\circ C$

Jan. 2000



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### RECOMMENDED OPERATING CONDITIONS (Unless otherwise noted, Ta = -40 ~ +85°C)

Symbol	Parameter	Limits			Unit	
		min	typ	max		
VO	Output voltage	0	—	50	V	
Ic	Collector current (Current per 1 circuit when 7 circuits are coming on simultaneously)	Duty Cycle P : no more than 8% FP : no more than 5% GP : no more than 4%	0	—	400	mA
		Duty Cycle P : no more than 30% FP : no more than 20% GP : no more than 15%	0	—	200	
VIH	"H" input voltage	5	—	25	V	
VIL	"L" input voltage	0	—	0.5	V	

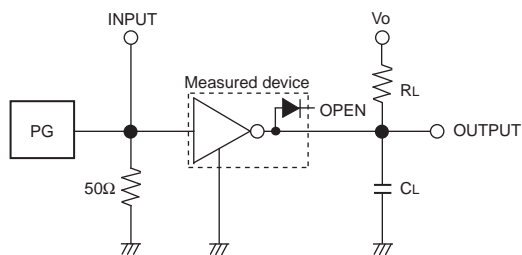
### ELECTRICAL CHARACTERISTICS (Unless otherwise noted, Ta = 25°C)

Symbol	Parameter	Test conditions	Limits			Unit
			min	typ	max	
V (BR) CEO	Collector-emitter breakdown voltage	ICEO = 100μA	50	—	—	V
VCE(sat)	Collector-emitter saturation voltage	II = 500μA, IC = 350mA	—	1.2	1.6	V
		II = 350μA, IC = 200mA	—	1.0	1.3	
		II = 250μA, IC = 100mA	—	0.9	1.1	
II	Input current	VI = 10V	—	0.9	1.4	mA
VF	Clamping diode forward voltage	IF = 350mA	—	1.4	2.0	V
IR	Clamping diode reverse current	VR = 50V	—	—	100	μA
hFE	DC amplification factor	VCE = 4V, IC = 350mA	1000	2500	—	—

### SWITCHING CHARACTERISTICS (Unless otherwise noted, Ta = 25°C)

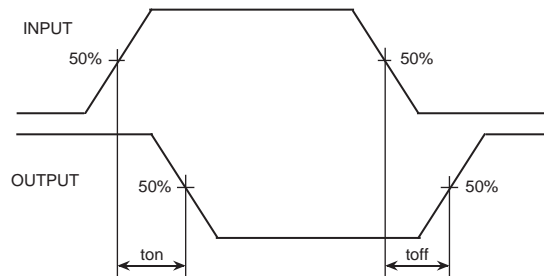
Symbol	Parameter	Test conditions	Limits			Unit
			min	typ	max	
ton	Turn-on time	CL = 15pF (note 1)	—	15	—	ns
toff	Turn-off time		—	350	—	ns

#### NOTE 1 TEST CIRCUIT



- (1) Pulse generator (PG) characteristics : PRR=1kHz,  
tw = 10μs, tr = 6ns, tf = 6ns, Zo = 50Ω  
VP = 8VP-P
- (2) Input-output conditions : RL = 25Ω, Vo = 10V
- (3) Electrostatic capacity CL includes floating capacitance at connections and input capacitance at probes

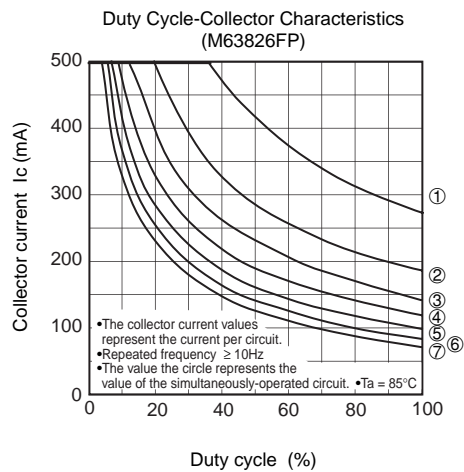
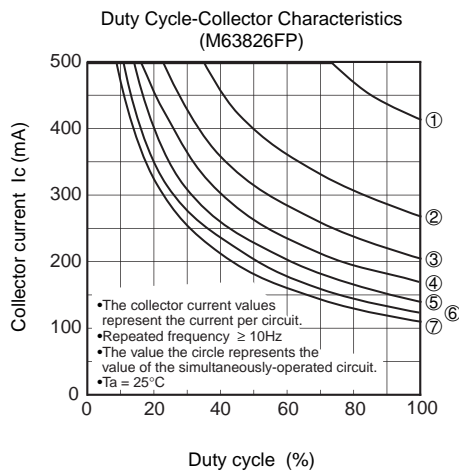
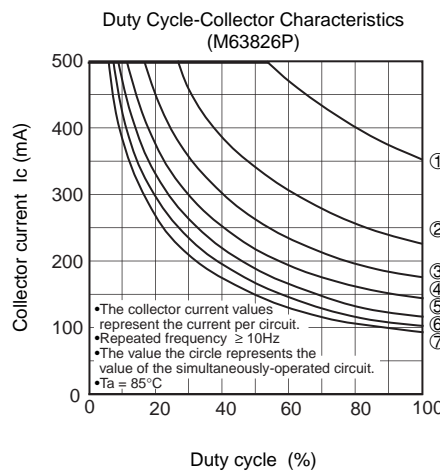
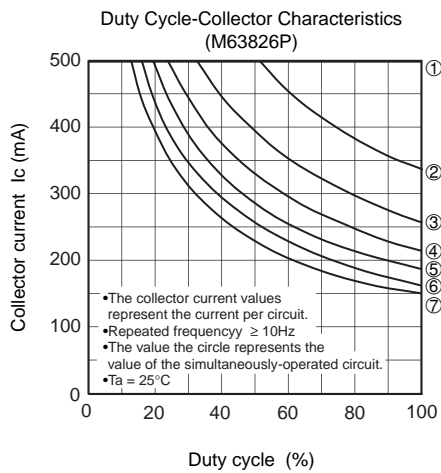
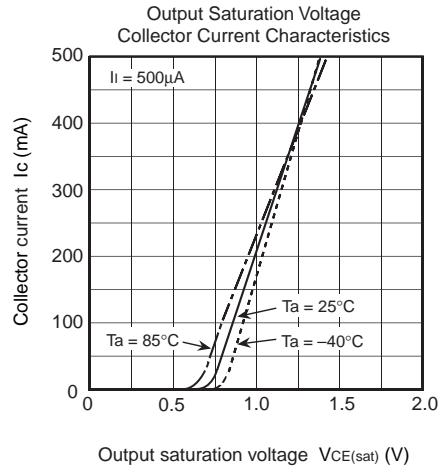
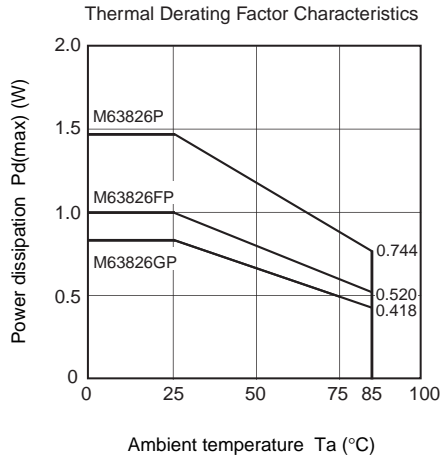
#### TIMING DIAGRAM



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### TYPICAL CHARACTERISTICS



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