OKI Semiconductor T-77-13

MSM6376

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ADPCM SPEECH SYNTHESIZER WITH EXTERNAL ROM

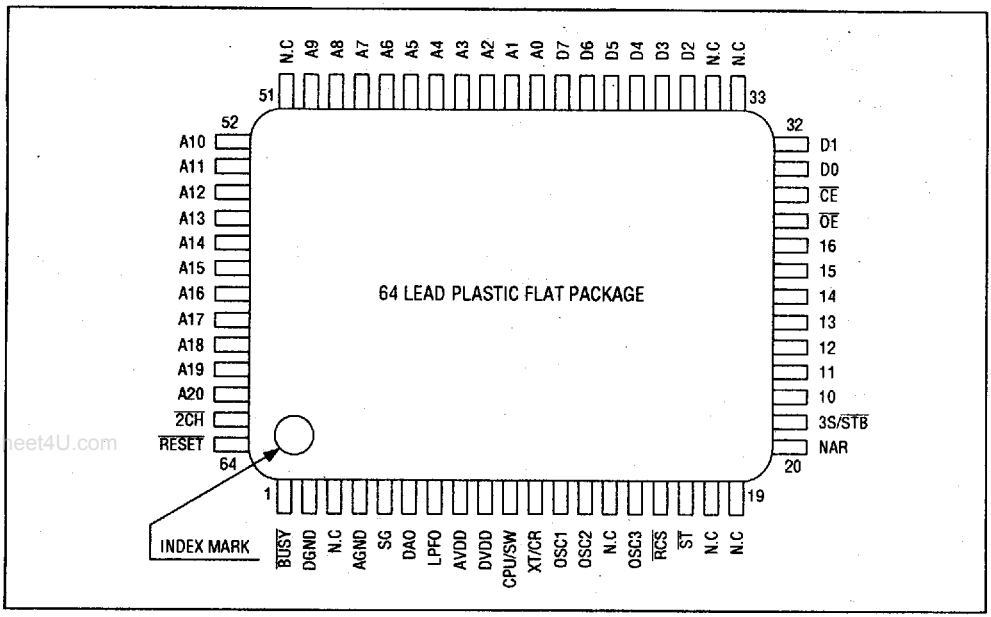
GENERAL DESCRIPTION

MSM6376 is a two-channel mixing ADPCM speech synthesizer LSI using up to 16 M-bit external speech data storage, such as ROM, and EPROM. Since it has a built-in 12-bit DA converter and low pass filter, a speech data output system can easily be configured by connecting an external power amplifier and speaker. MSM6376 is best suited to the evaluation of MSM6372, MSM6373, MSM6374, and MSM6375, which are used as speech synthesizer LSIs with built in ROM, because the MSM6376 has the same circuit configuration as those LSIs.

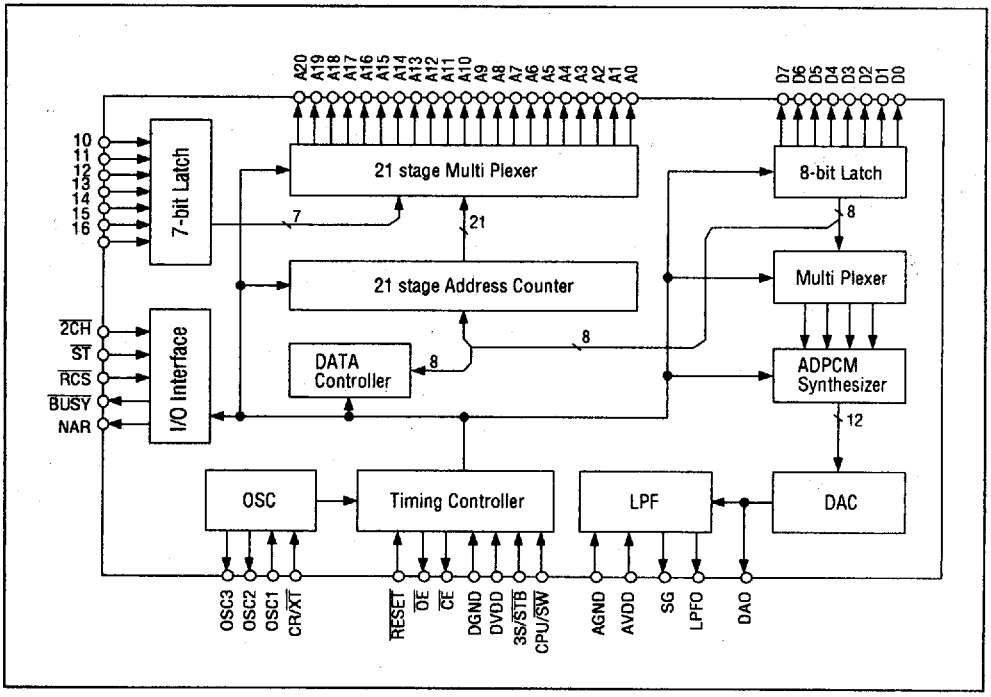
FEATURES

- External memory capacity 16 Mbits ROM
- 4-bit straight ADPCM method
- Echo reproduction and simultaneous output of two audible tones (sound volume variation for one tone in three stages)
- Output of either of two built-in BEEP tones (1 Hz and 2 Hz) by designation code (when oscillation is 64 kHz)
- Sampling frequency 4.0, 6.4 and 8.0 kHz (at oscillation of 64 kHz) up to 32 kHz is possible.
- Maximum speech period of 10.9 minutes (at sampling frequency of 6.4 kHz) with 16 Mbits ROM
- Maximum number of words:
  111 words
- Built-in 12-bit D/A converter of class A voltage type (with built-in pop noise suppression circuit)
- Built-in LPF with attenuation factor of – 24 dB/oct (fcut to 3 x fcut)
  Note) fcut=cutoff frequency
- Standby function to stop oscillation and all functions during the standby state
- Oscillation selectable between CR oscillation and crystal oscillation
- Master oscillation frequency:
  64 to 128 kHz (LPF output)
  64 to 256 kHz (DAC output)
- Supply voltage:
  4.5 to 5.5V
- 64 pin-V1 plastic QFP
  (QFP64-P-1420-V1K)

PIN CONFIGURATION (Top View)



BLOCK DIAGRAM



• Absolute Maximum Ratings

(DGND = AGND = 0V)

Parameter	Symbol	Conditions	Rating	Unit
Power supply voltage	V_{DD}	Ta = 25°C	−0.3 ~ +7.0	V
Input voltage	V_I		−0.3 ~ V_{DD} +0.3	V
Storage temperature	T_{stg}	—	−55 ~ +150	°C

• Operating Ranges

(DGND = AGND = 0V)

Parameter	Symbol	Conditions	Range	Unit
Power supply voltage	V_{DD}	–	4.5 ~ +5.5	V
Operating temperature	T_{opr}	–	−40 ~ +85	°C
DAO output level	V_{DD}	No load	0 ~ V_{DD}	V

• DC Characteristics

(DV_{DD} = AV_{DD} = 5V, DGND = AGND = 0V, Ta=−40~85°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
"H" input voltage	V_{IH}	—	4.2	—	—	V
"L" input voltage	V_{IL}	—	—	—	0.8	V
"H" output voltage	V_{OH}	I_{OH} = −40 µA	4.6	—	—	V
"L" output voltage	V_{OL}	I_{OL} = 40 µA	—	—	0.4	V
"H" input current	I_{IH}	V_{IH} = V_{DD}	—	—	10	µA
"L" input current	I_{IL}	V_{IL} = 0V	−10	—	—	µA
Operating current consumption	I_{DD1}	—	—	4	10	mA
Output leak current	I_{LO}	$0 \leqq V_{OUT} \leqq V_{DD}$	−10	—	10	µA
Standby current consumption	I_{DD2}	—	—	—	10	µA
Relative precision of DA output	V_{DAE}	no load	—	—	40	mV
DA output impedance	R_{OR}	—	15	25	35	kΩ
LPF load impedance	R_{AOUT}	—	50	—	—	kΩ

- **AC Characteristics (V_{DD} = 5V, Ta = –40 ~ 85°C, f_{OSC1} = 64 kHz)**

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Master oscillation frequency	$f_{(osc1)}$	—	40	–	256	kHz
Master oscillation duty cycle	f_{duty}	—	40	50	60	%
$\overline{RESET}$ input pulse width	$t_{W(\overline{RST})}$	—	10	–	–	µS
$\overline{ST}$ input pulse width (Note 1)	$t_{W(\overline{ST})}$	CPU interface	0.35	–	350	µS
$\overline{2CH}$ input pulse width	$t_{W(\overline{2CH})}$	—	0.35	–	–	µS
$\overline{ST}$–$\overline{ST}$ pulse interval	t_{SS}	—	0.35	–	–	µS
$\overline{2CH}$ setup time	t_{CHS}	—	0.35	–	–	µS
$\overline{2CH}$ hold time	t_{SCH}	—	0.35	–	–	µS
Data set time	t_{DW}	—	10	–	–	µS
Data hold time	t_{WD}	—	10	–	–	µS
$\overline{RCS}$ setup time	t_{CS}	—	10	–	–	µS
$\overline{RCS}$ hold time	t_{BC}	—	10	–	–	µS
Selectable sampling frequency	f_{S1}	$f_{(osc1)}/8$	–	8.0	–	kHz
	f_{S2}	$f_{(osc1)}/10$	–	6.4	–	kHz
	f_{S3}	$f_{(osc1)}/16$	–	4.0	–	kHz
$\overline{BUSY}$ output time (1)	t_{SBS}	—	–	–	10	µS
$\overline{BUSY}$ output time (2) (Note 2)	t_{BN}	At f_s = 8 kHz	350	375	400	µS
$\overline{BUSY}$ output time (3) (Note 5)	t_{BF}	At master frequency=64 kHz	–	–	64	mS
NAR output time (1)	t_{SNS}		–	–	10	µS
NAR output time (2) (Note 2)	t_{NAA}	At f_S=8 kHz	350	375	400	µS
NAR output time (3) (Note 2)	t_{NAB}	At f_S=8 kHz	350	375	400	µS
NAR output time (4) (Note 2)	t_{NAC}	At f_S=8 kHz	350	–	550	µS
D/A converter transition time (Note 3)	t_{DAR}, t_{DAF}	At master frequency=64 kHz	60	64	68	mS
LPF stabilizing time (Note 4)	t_L	At master frequency=64 kHz	12	16	20	mS
Standby transition time (Note 3) (at end of speech output)	t_{STB}	At master frequency=64 kHz	2.9	3.0	3.1	mS
$\overline{ST}$ - $\overline{2CH}$ pulse interval	t_{S2CH}	At master frequency=64 kHz	1.0	–	–	mS
$\overline{ST}$ input wait time	t_{NS}	—	10	–	–	µS

Note 1: The MAX value is proportional to f_S.
Note 2: The duration is proportional to f_S.
Note 3: The duration is proportional to f_{OSC}.
Note 4: Applicable at the start of oscillation.
Note 5: When playback occurs during the standby transition period (t_{DAF}).

- **AC Characteristics (V_{DD} = 5V, Ta = –40 ~ 85°C, f_{OSC1} = 40 - 256 kHz)**

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Master oscillation frequency	$f_{(osc1)}$	—	40	–	256	kHz
Master oscillation duty cycle	f_{duty}	—	40	50	60	%
$\overline{RESET}$ input pulse width	$t_{W(\overline{RST})}$	—	10	–	–	µS
$\overline{ST}$ input pulse width	$t_{W(\overline{ST})}$	CPU interface	0.35	–	a	µS
$\overline{2CH}$ input pulse width	$t_{W(\overline{2CH})}$	—	0.35	–	–	µS
$\overline{ST}$–$\overline{ST}$ pulse interval	t_{SS}	—	0.35	–	–	µS
$\overline{2CH}$ setup time	t_{CHS}	—	0.35	–	–	µS
$\overline{2CH}$ hold time	t_{SCH}	—	0.35	–	–	µS
Data set time	t_{DW}	—	10	–	–	µS
Data hold time	t_{WD}	—	10	–	–	µS
$\overline{RCS}$ setup time	t_{CS}	—	10	–	–	µS
$\overline{RCS}$ hold time	t_{BC}	—	10	–	–	µS
Selectable sampling frequency	f_{S1}	—	–	$f_{(osc)}/8$	–	kHz
	f_{S2}	—	–	$f_{(osc)}/10$	–	kHz
	f_{S3}	—	–	$f_{(osc)}/16$	–	kHz
$\overline{BUSY}$ output time (1)	t_{SBS}	—	–	–	10	µS
$\overline{BUSY}$ output time (2)	t_{BN}	—	a	b	c	µS
$\overline{BUSY}$ output time (3) (Notes 2)	t_{BF}	—	–	–	e	mS
NAR output time (1)	t_{SNS}	—	–	–	10	µS
NAR output time (2)	t_{NAA}	—	a	b	c	µS
NAR output time (3)	t_{NAB}	—	a	b	c	µS
NAR output time (4)	t_{NAC}	—	a	–	d	µS
D/A converter transition time	t_{DAR}, t_{DAF}	—	e-4	e	e+4	mS
LPF stabilizing time (Note 1)	t_L	—	f-4	f	f+4	mS
Standby transition time (at end of speech output)	t_{ST8}	—	g-0.1	g	g+0.1	mS
$\overline{ST}$–$\overline{2CH}$ pulse interval	t_{S2CH}	—	h	–	–	mS
$\overline{ST}$ input wait time	t_{NS}	—	10	–	–	µS

$$a = 350 \times \frac{8\ (kHz)}{f_S\ (kHz)} \quad b = 375 \times \frac{8\ (kHz)}{f_S\ (kHz)} \quad c = 400 \times \frac{8\ (kHz)}{f_S\ (kHz)} \quad d = 550 \times \frac{8\ (kHz)}{f_S\ (kHz)}$$

$$e = 64 \times \frac{64\ (kHz)}{f_{OSC}\ (kHz)} \quad f = 16 \times \frac{64\ (kHz)}{f_{OSC}\ (kHz)} \quad g = 3.0 \times \frac{64\ (kHz)}{f_{OSC}\ (kHz)} \quad h = 1.0 \times \frac{64\ (kHz)}{f_{OSC}\ (kHz)}$$

Note 1: Applicable at the start of oscillation.
Note 2: When playback occurs during the standby transition period (t_{DAF}).

TIMING DIAGRAMS

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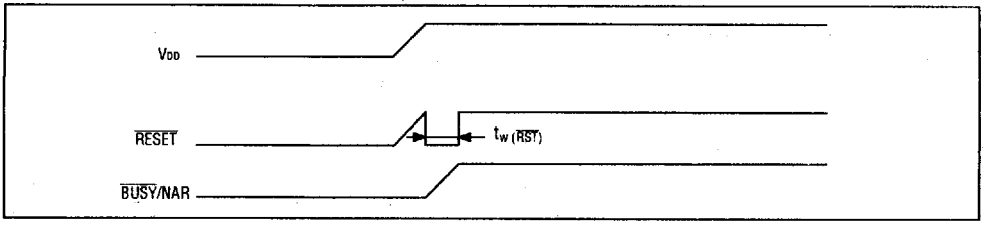
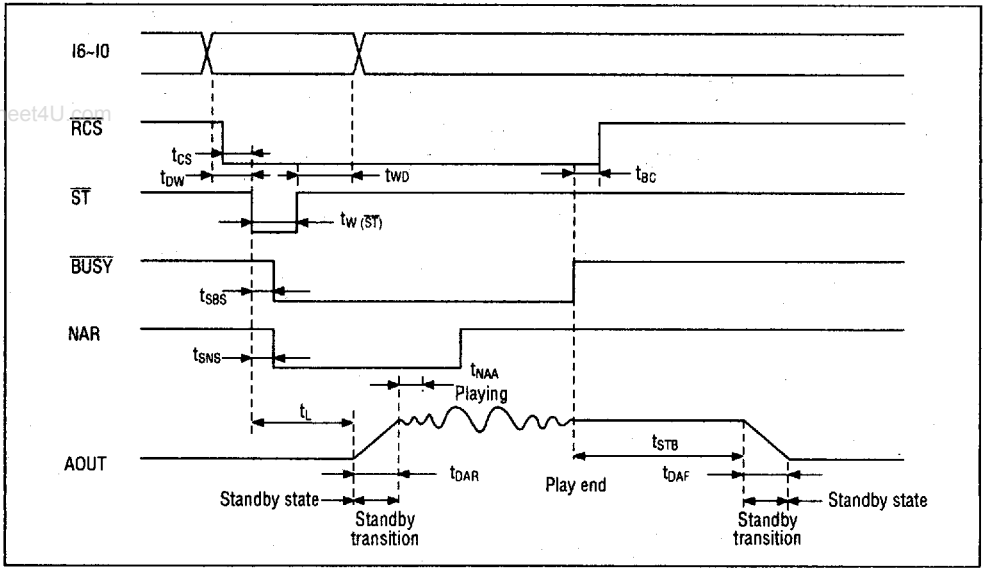
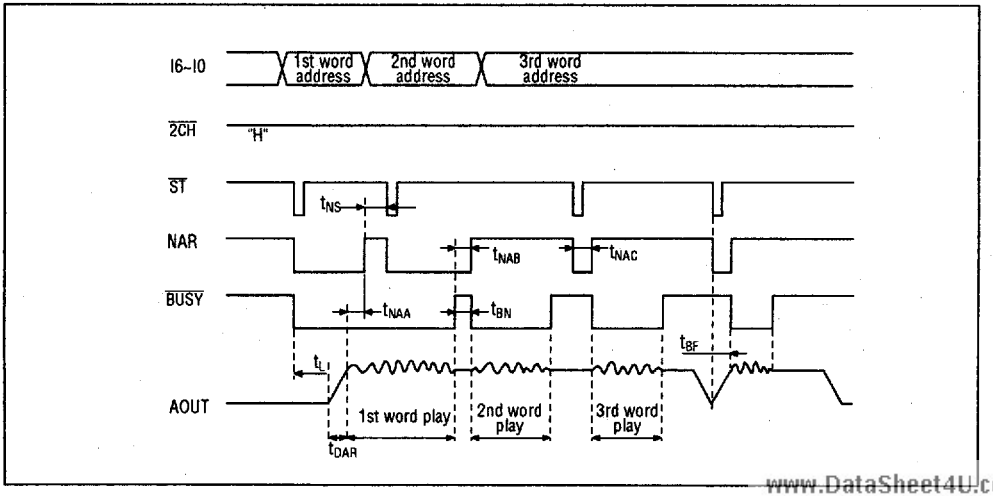
1. At power-on



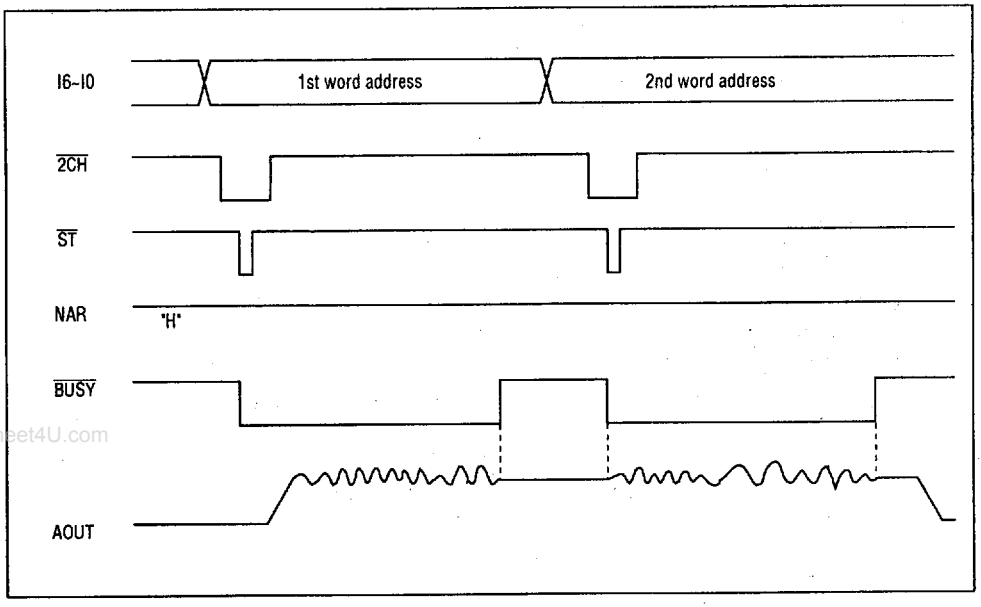
2. At LSI startup and in standby state



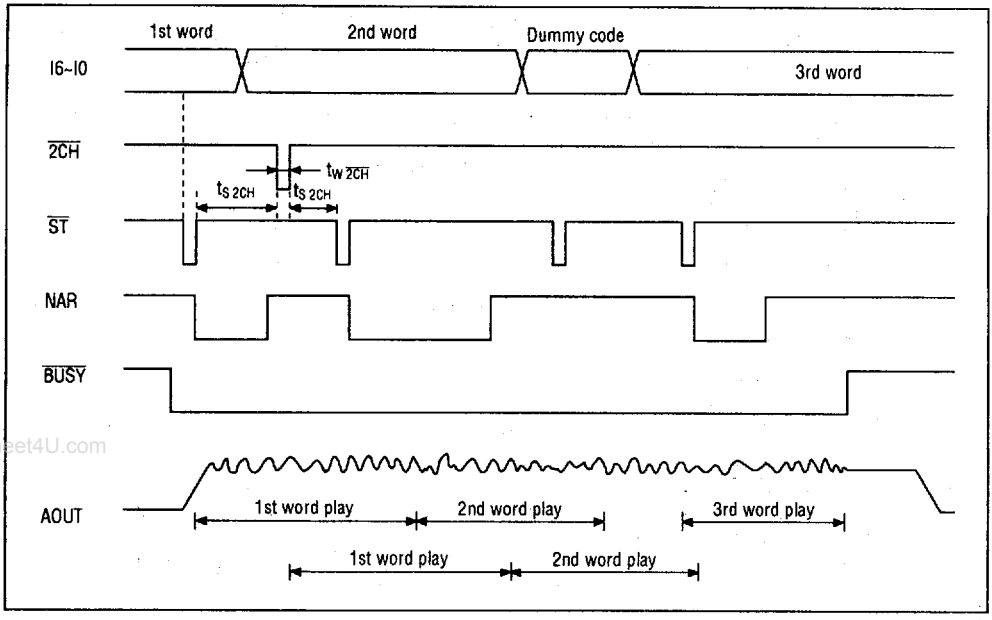
3. Operation in channel 1 only (CPU input interface)



4. Operation in channel 2 only (CPU input interface)



5. Timing Diagram of Echo Playback in Channel 1



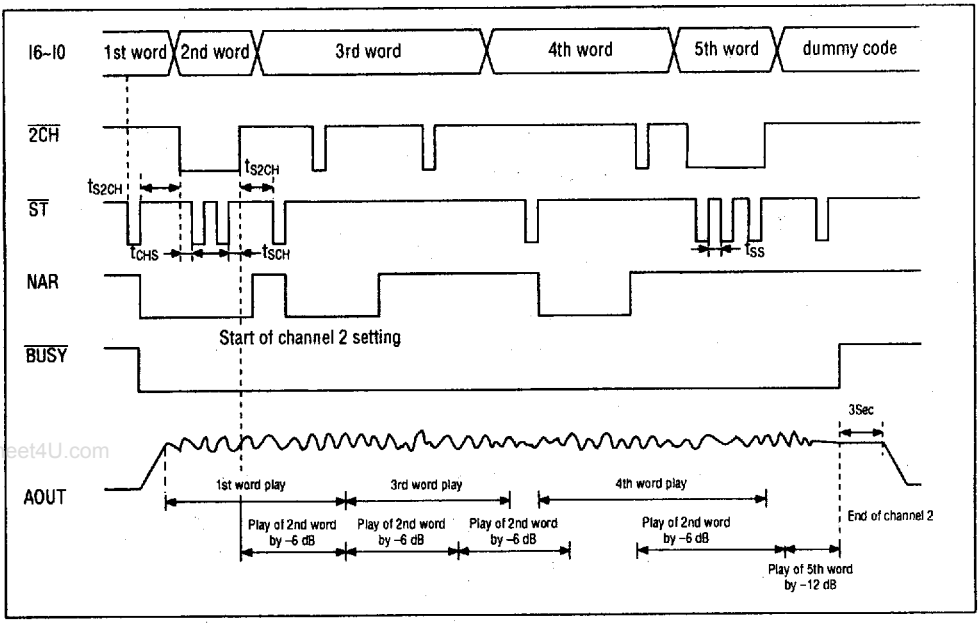
1. Input of the $\overline{2CH}$ pulse without lowering $\overline{ST}$ starts echo playback. Echo playback is canceled unless play is continuous.

2. At echo playback, the waveform is a combination of the playback of channel 1 by the $\overline{ST}$ pulse and a-6 DB playback of channel 2 by the $\overline{2CH}$ pulse.

3. In continuous play, the echo is applied to the next word (continuous play means playback of another word during a single word vocalization.)

4. Input unused code as a dummy code from the user selectable code at the end of echo playback. Without this input, the LSI may enter the standby mode without waiting for the 3 seconds after the end of playback when the standby option is selected.

6. Timing Diagram of Simultaneous Playback in Channel 1 and Channel 2



1. Channel 2 starts playing when the $\overline{ST}$ pulse is input and $\overline{2CH}$="L". The sounds volume can be changed by the number of the $\overline{ST}$ pulses using the table below.

2 Channel 2 plays a pre-set word each time the $\overline{2CH}$ pulse is input with the same sound volume until the LSI goes to the standby state or until channel 2 is reset.

3 Please input an unused code as a dummy code from the user selectable codes at the end of playback of channel 2. Without this input, the LSI may enter the standby mode without waiting for the 3 seconds after the end of play when the standby option is selected.

Number of $\overline{ST}$ pulses	Attenuation
1	No attenuation
2	-6dB attenuation
3	-12dB attenuation

PIN FUNCTIONS

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Pin name	Input/output	Function
I6-I0	Input	Selects and enters a user-specified word corresponding to the vocalized word. The code when the level of the $\overline{ST}$ pulse goes low is read, and latched as the level rises.
A0-A20	Output	These are the address terminals for the external connection of memory. The data is output when $\overline{RCS}$ is "L".
D0-D7	Input	These are the terminals to input the data from external memory. The data is input when $\overline{RCS}$ is "L".
$\overline{2CH}$	Input	Reproduces echo, or reproduces two different tones simultaneously. If $\overline{2CH}$ pulse is entered during operation in channel 1, echo is reproduced. Delay time for the echo can be changed according to the time of input of $\overline{2CH}$ pulse. If $\overline{ST}$ pulse is entered when the level for CH2 is low, reproduction is performed in channel 2.
$\overline{ST}$	Input	Activated at the fall of $\overline{ST}$. Data on I6 through I0 is read when their level is "L", and latched at the rise of $\overline{ST}$. Enter an address for channel 1 when the level of NAR is "H". For reproduction in channel 2, sound volume can be changed according to the number of $\overline{ST}$ pulses when the level of $\overline{2CH}$ is "L". In the case of SW input interface, synthesis is repeated while the level of $\overline{ST}$ is set to "L".
$\overline{RCS}$	Input	When the level is "L", this terminal enables $\overline{ST}$ pulse to be input and the address from A0-A20, $\overline{OE}$ and $\overline{CE}$ are output. When the level is "H", the address terminals of A0-A20, and $\overline{CE}$ and $\overline{OE}$ become high impedance.
$\overline{BUSY}$	Output	During playback, "L" level is output.
NAR	Output	When the level is "H", the next channel address can be input.
CR/$\overline{XT}$	Input	Selects CR oscillation or crystal oscillation. If the level of CR/$\overline{XT}$ is set to "H", OSC1, OSC2, and OSC3 work as CR oscillation terminals; if the level of CR/$\overline{XT}$ is set to "L", OSC1 and OSC2 work as crystal oscillation terminals, and a resistor with a resistance of about 2 M-ohms is inserted between OSC1 and OSC2.

Pin name	Input/output	Function
OSC1 OSC2 OSC3	Input Output Output	Crystal oscillation and CR oscillaito terminals. To use them for crystal oscillation, leave the OSC3 terminal open. If an external clock signal is to be used, it should be connected to the OSC1 terminal with OSC2 and OSC3 left open.
CPU/$\overline{SW}$	Input	Terminal for selection between CPU interface and SW input interface. "H" level = CPU interface. "L" level = switch interface Note: If SW input interface is selected, echo reproduction, and 2-channel mixing reproduction cannot be performed.
3S/$\overline{STB}$	Input	If the level of the 3S terminals is "H", standby state is invoked three seconds after completion of speech synthesis. If the level of the 3S terminals is "L", the output from the DA converter remains at 1/2 VDD after completion of speech synthesis.
$\overline{RESET}$	Input	If the level of this terminals is set to "L", the LSI is put in standby state. Upon $\overline{RESET}$, oscillation is stopped, the output from the DA converter is grounded, and put to the initial state. The M6376 has a built-in power-on reset circuit. To make the power-on resetting function reliably, raise the power supply within 1msec. If this is impossible to do, enter the $\overline{RESET}$ pulse when the power is turned on.
$\overline{CE}$	Output	A timing output terminal that controls chip enable of external memory. The signal is output when the level of $\overline{RCS}$ is "L".
$\overline{OE}$	Output	A timing output terminal that controls reading from external memory. The signal is output when the level of $\overline{RCS}$ is "L".
DAO	Output	A terminal that outputs analog voice sent from the DA converter.
AOUT	Output	A terminal for output of analog voice sent from the LPF.
SG	Output	A terminal that improves SN ratio of LPF. To utilize the outpur from the LPF, connect a capacitor of about 1μF.
AVDD		An analog power supply terminal.
AGND		An analog grounding terminal.
DVDD		A digital power supply terminal.
DGND		A digital grounding terminal.

FUNCTION DESCRIPTION

1. Voice Code Selection

User selectable words (phrases) are maximum 111 words/phrases. The setting of I0-I6 is as follows:

Table 1 List of User Selected Words

I0-I6	Code explanation
0000000	STOP code
0000001 ↕ 1101111	User selectable code (111 words)
1110000 ↕ 1110111	BEEP code
1111000 ↕ 1111111	Test codes (do not use)

2. CPU Interface and Switch Input Interface

The CPU interface and the switch input interface can be selected by the CPU/$\overline{SW}$ pin. When the CPU pin is high, the CPU interface is on. When the CPU pin is low, the switch input interface is on.

2-1 CPU interface

If the CPU interface is selected, the $\overline{ST}$ pulse becomes valid when the NAR pin is "H". User selected words are then fetched internally and vocalized. This interface is effective for playback of several words continuously. Please note that when the $\overline{ST}$ pulse is

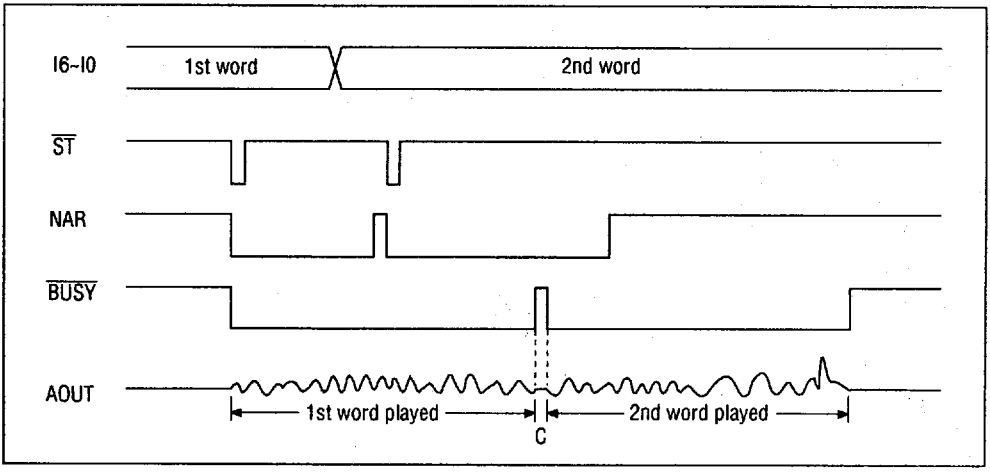


Figure 1 Timing of CPU Interface ($\overline{ST}$ ≤ 350 µS)

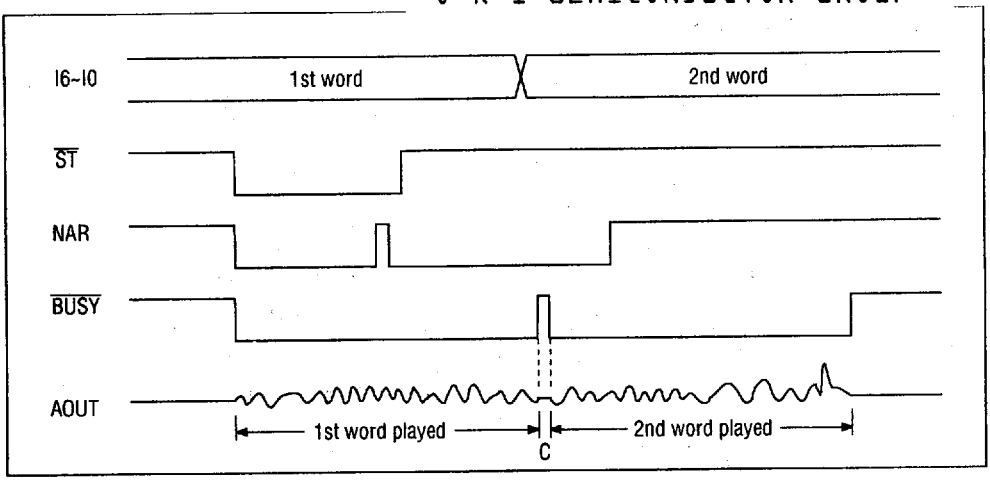


Figure 2 Timing of CPU Interface ($\overline{ST}$ > 800 µS)

kept at the "L" level for longer than 800 µS, one word is played twice (at 8 kHz sampling).

When the $\overline{ST}$ pulse width is between 350 µS and 800 µS, a single word is played once or twice. However, when the $\overline{ST}$ pulse is input from the standby state, a single word is played only once if within 80µS.

When a $\overline{ST}$ pulse width of longer than 350µS (master frequency is 64 kHz) is input and the $\overline{BUSY}$ option has been selected, make sure the $\overline{ST}$ pulse is within 800 µS after the rise of $\overline{BUSY}$ pin.

2-2 SW input interface

If the SW input interface is selected, the specified word is played repeatedly when $\overline{ST}$ is "L" at the end of play of the specified word and is finished when it is "H".

For example, when this LSI is operated using a push switch , the same word is played repeatedly as long as the switch is pressed

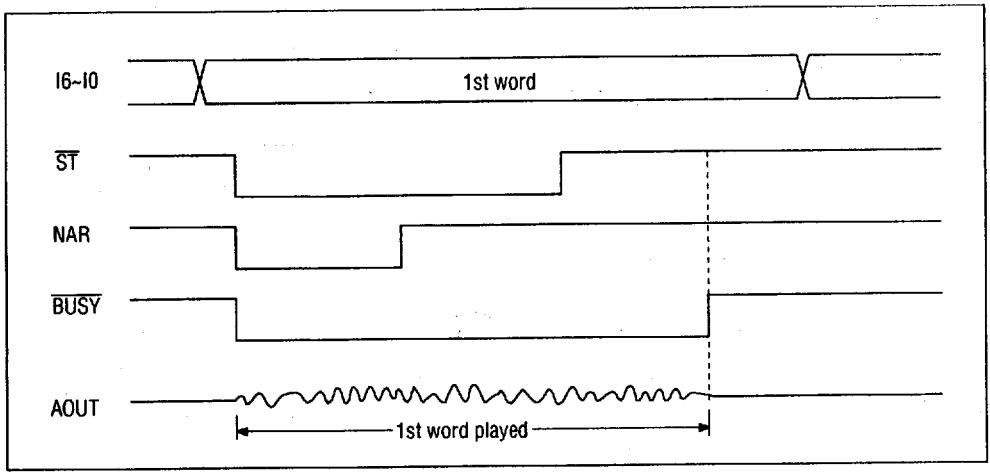


Figure 3 Timing of SW Input Interface (playing one word)

and when the switch is released, playback stops when the currently playing word is finished.

When playing different words continuously, change the code of I0-I6 and maintain $\overline{ST}$ at the "L" level before the play back is completed.

However, note that the playing interrupted if the input level of I6-I0 becomes "L" instantly when switching the address.

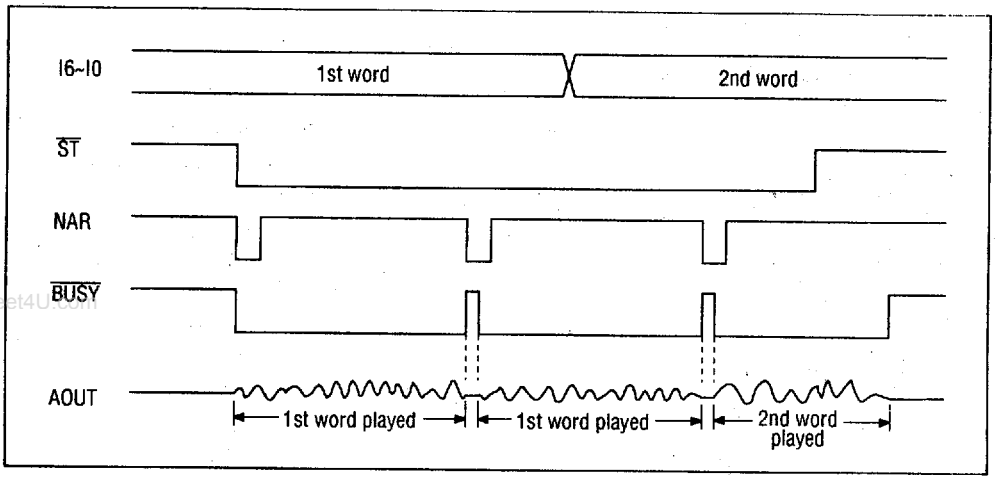


Figure 4 Timing of SW Input Interface (repeated play)

In SW input interface, playback of the 1st and 2nd channels simultaneously is not possible. Neither 2 channel mixing nor echo playback is possible in this interface.

3. BEEP Tone Generation

Since this LSI has an on-chip circuit to generate BEEP tones, the BEEP tones are selected using I6-I0. Depending on the word code, the frequency and duration can be changed. The amplitude is approximately $1/4\ V_{DD}$.

The NAR/$\overline{BUSY}$ pin outputs a "L" level during BEEP tone play regardless of either NAR or /BUSY is selected as the option. Figure 5 shows such timing.

Neither the STOP code (explained later) nor 2 channel playback is valid during the playback of BEEP tone, The following table shows the relationship between the BEEP tones and addresses when the oscillation frequency is 64 kHz.

Table 2 Relationship between BEEP Tones and Addresses

I6	I5	I4	I3	I2	I1	I0	BEEP tone frequency	Generating duration (sec)
1	1	1	0	0	0	0	2.0	0.064
					0	1		0.125
					1	0		0.250
					1	1		0.500
				1	0	0	1.0	0.064
					0	1		0.125
					1	0		0.250
					1	1		0.500

When the code for BEEP tone is input while playing either the 1st channel or the 2nd channel, the BEEP tone is generated after the completion of play. The reverse case also holds true.

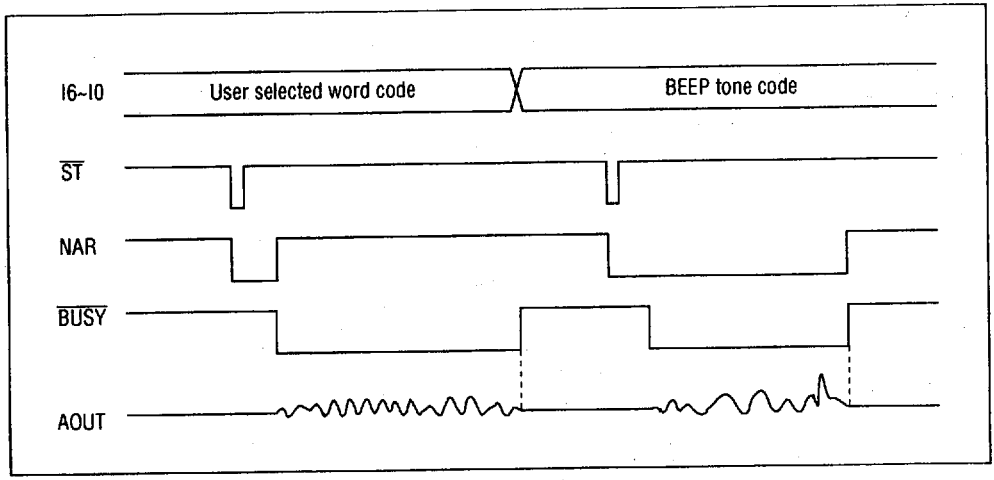


Figure 5 Timing at BEEP Tone Generation

4. Stop Code

Speech playing is finished when the $\overline{ST}$ pulse is input by setting I6-I7 to "0000000" during play. The DA converter becomes 1/2 V_{DD}.

The input method of the $\overline{ST}$ pulse is subject to the AC characteristics when the NAR output is "H". When the NAR output is at the "L" level, the STOP code is valid by setting the $\overline{ST}$ pulse to the "L" level longer than 1 msec (f_{OSC}=64 kHz) or by the timing shown in Figure 6.

The STOP code is not valid during the generation of BEEP tone. When the STOP code is input, only playback is stopped while the oscillation and the analog circuitry are still operating. When the $\overline{RESET}$ pulse is input, all operations are halted.

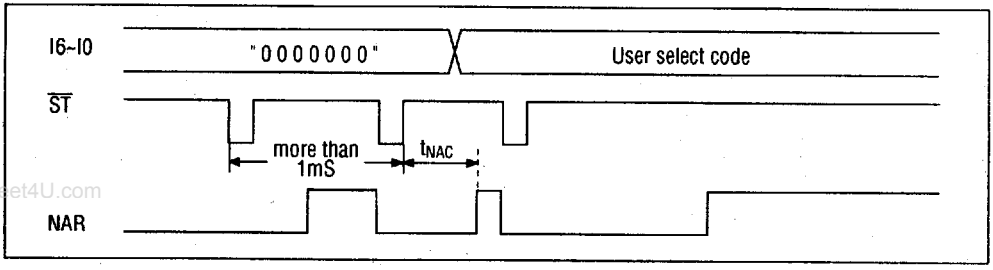


Figure 6 Example of STOP Code Input Timing

5. Sampling Frequencies

Sampling frequencies can be specified for each word in the speech data of the built-in ROM. When the 1st and the 2nd channels are simultaneously played back, the sampling frequency of the 1st channel has priority.

Three types of sampling frequencies can be selected during speech data analysis. The relationship between the master frequency, f_{OSC}, and the sampling frequency, f_S, is as follows:

Selection 1	f_{S1}=fose/8
Selection 2	f_{S2}=fose/10
Selection 3	f_{S3}=fose/16

6. Echo Playback and Channel 2 Playback

By using the $\overline{2CH}$ input, echo or 2 channel playback is possible. Because both echo and 2 channel playback use the $\overline{2CH}$ pin, switch between modes by returning the LSI to the standby state.

This function is not available in the SW input interface or during generation of BEEP tones.

6-1 Echo Playback

Echo playback is performed by combining a speech waveform of the 1st channel with a delayed speech waveform with -6 dB attenuation (half the amplitude of the channel 1 speech waveform).

The echo delay time is the time until the $\overline{2CH}$ pulse is input from the start of play of channel 1.

However, when starting this operation from the standby state, pop noise suppression time is not counted as delay time.

In echo playback, echo is applied to all the words during continuous play of channel 1 (continuous play means playback of the next word during playback.)

6-2 Channel Mixing Playback

Using 2 channel mixing playback, a different word can be played during the play of channel 1. This has a wide range of application such as BGM (back ground music) and combinations of instruments. Speech data on channel 2 can remain the same while the sound volume may be changed to 1, 1/2 and 1/4 according to channel 1. The change in

sound volume is determined by the number of $\overline{ST}$ pulses when starting the 2nd channel.

Table 3 Number of $\overline{ST}$ Pulses and Attenuation

Number of $\overline{ST}$ pulses	Attenuation
1	No attenuation (100% of speech data)
2	-6dB attenuation (1/2 of speech data)
3	-12dB attenuation (1/4 of speech data)

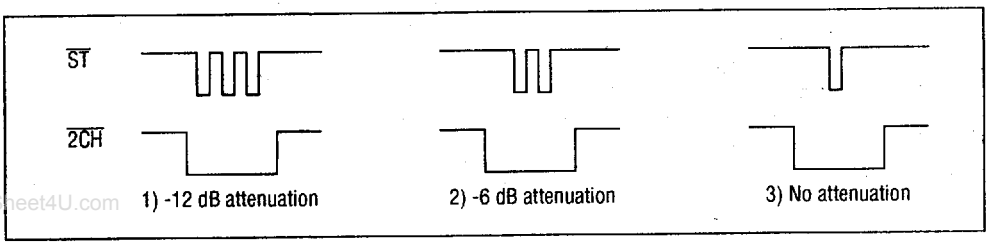


Figure 7 Input Timing of 2 Channel Mixing

Once 2 channel mixing is set, it is maintained until the standby state or until channel 2 is reset. Because of this, restart can be accomplished by the input of the $\overline{2CH}$ pulse only.

7. Standby Transition

When standby transition is enabled as an option, the LSI changes to the standby state and halts all operations unless another word is played within 3 seconds of the completion of playback of a single word. For this reason, it takes approximately 100 mS before the next playback is started as the LSI needs to activate the pop noise suppression circuitry.

When standby transition is disabled as an option, the LSI does not go into the standby mode even when playback is completed. At this time, the output from AOUT is approximately 1/2 V_{DD} and the LSI still draws current as oscillation is continued. When restarted, the next playback begins after approximately 350 µs.

If disabling standby transition as an option, the $\overline{RESET}$ pulse must be input to set to the standby state. Pop noise may be generated at the input of the $\overline{RESET}$ pulse as the output level from AOUT becomes GND level instantly.

8. Voice Input

The voice output pin can be selected by the output of the DA converter either directly or through the built-in low-pass filter.

8-1 Output Waveform of DA Converter

The output amplitude from the DA converter is maximum 4095/4096 x V_{DD} of a square wave that synchronizes with a sampling frequency. When selecting the DA output, addition of an external low-pass filter is highly recommended.

Because the output impedance of DAO varies between 15KΩ and 35KΩ, determine the filter constant so that the resistance variation does not influence the cut-off frequency of the low-pass filter.

Table 4 shows the output level from the AOUT pin when selecting an optional DA output.

Table 4 Output Level from DA Converter

Condition	Minimum level	Center level	Maximum level	Unit
1 channel playback	$\frac{1}{4}V_{DD}$	$\frac{1}{2}V_{DD}$	$\frac{3}{4}V_{DD}$	V
2 channel mixing	0.0	$\frac{1}{2}V_{DD}$	V_{DD}	V
BEEP tone playback	$\frac{3}{8}V_{DD}$	$\frac{1}{2}V_{DD}$	$\frac{3}{8}V_{DD}$	V

8-2 Low-pass filter output

Since the low-pass filter is composed of switch capacitors, the cut-off frequency varies proportional to the master clock frequency.

When the sampling frequency (f_s) is 1/8 and 1/10 of the master clock frequency, the cut-off frequency, f_{cut}, is $f_{cut}=3/64\ f_{osc}$ and is $f_{cut}=3/128$ when f_s is 1/16. Table 5 shows the relationship between the sampling frequencies and the cut-off frequencies.

Table 5 Cut-off Frequency of Low-pass Filter

Sampling frequency (f_s)	Master clock frequency (f_{osc})	Cut-off frequency (f_{cut})
4.0 kHz	64 kHz	1.5 kHz
6.4 kHz	64 kHz	3.0 kHz
8.0 kHz	64 kHz	3.0 kHz
12.8 kHz	128 kHz	6.0 kHz
16.0 kHz	128 kHz	6.0 kHz

The low-pass filter characteristics when the sampling frequency is 8 kHz are shown in figure 8. Table 6 shows the output level from AOUT when selecting the low-pass filter option.

Table 6 Output Level of Low-pass Filter

Condition	Minimum level	Center level	Maximum level	Unit
1 channel playback	$\frac{1}{4}V_{DD}$	$\frac{1}{2}V_{DD}$	$\frac{3}{4}V_{DD}$	V
2 channel mixing	0.7	$\frac{1}{2}V_{DD}$	$V_{DD}-0.7$	V
BEEP tone playback	$\frac{3}{8}V_{DD}$	$\frac{1}{2}V_{DD}$	$\frac{3}{8}V_{DD}$	V

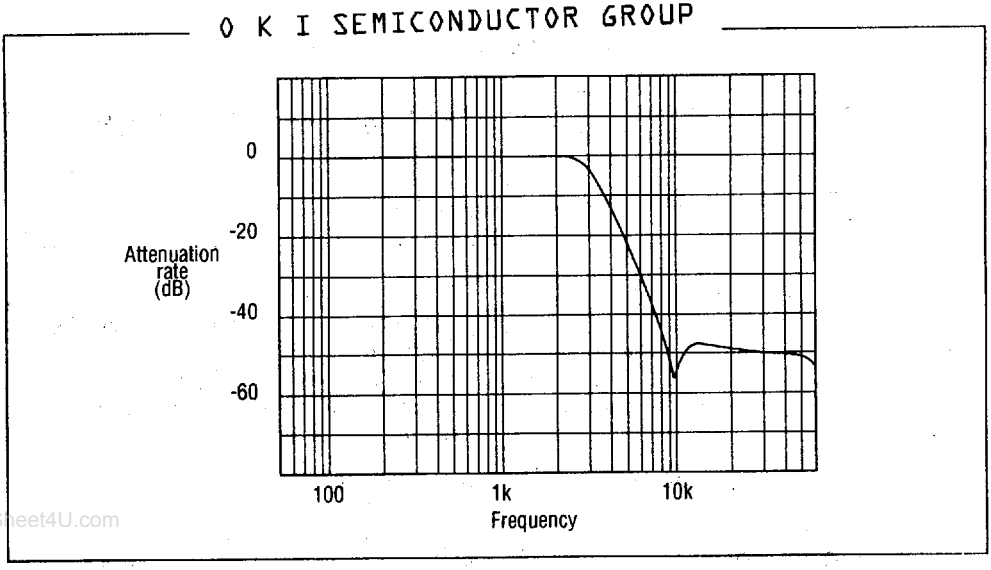


Figure 8 Low-pass Filter Characteristics (f_s=8 kHz)

8-3 Pop Noise of Low-Pass Filter Output

Although this LSI has a built-in pop noise suppression circuit, the voltage of the circled portion in the figure below may be changed abruptly by approximately 0.7V when selecting the low-pass filter output and may generate a "pop" sound.

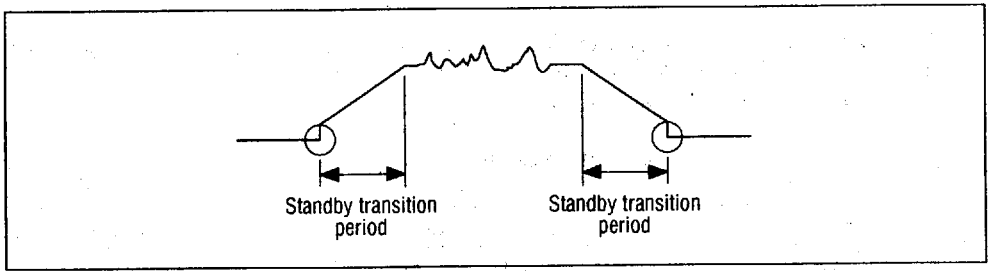


Figure 9 Pop Noise of Low-pass Filter Output

When connecting a diode at the output from AOUT, the "pop" sound can be reduced. Figure 10 shows the circuit.

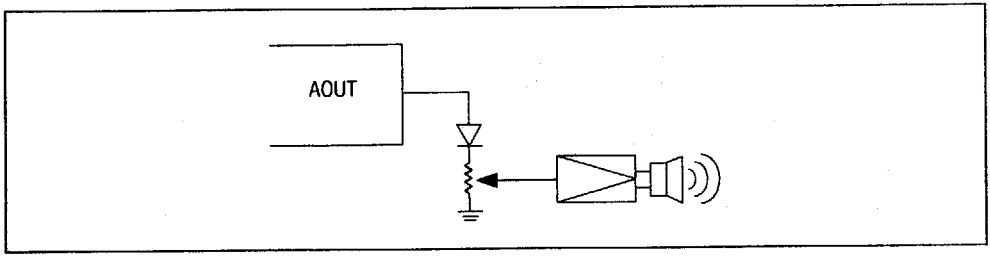


Figure 10 Pop Noise Suppression Circuit

9. RC Oscillation

The external circuit diagram for RC oscillation is shown below:

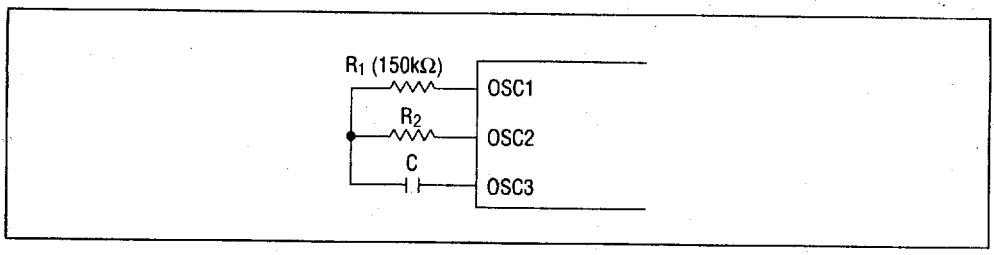


Figure 11 RC Oscillation Connection Circuit

9-1 Determination of RC Constant

The RC oscillation frequency characteristics are shown in Figure 12. If f_{OSC} is set to 64 kHz, choose the appropriate values for C and R_2 using the following as a reference:

C=100 pF, R_1=150kΩ, R_2=50kΩ.

9-2 Fluctuation of RC oscillation frequencies

When choosing RC oscillation, the RC oscillation frequencies are varied according to the fluctuation of the external C and R_2 as well as the process variations of LSI.

When using a 50kΩ R2, the error due to process variations of the LSI is maximum ±4% so that the fluctuation of the RC oscillation frequency when using a capacitance (C) of ±1% accuracy and a resistance (R_2) of ±2% accuracy is maximum ±7% approximately.

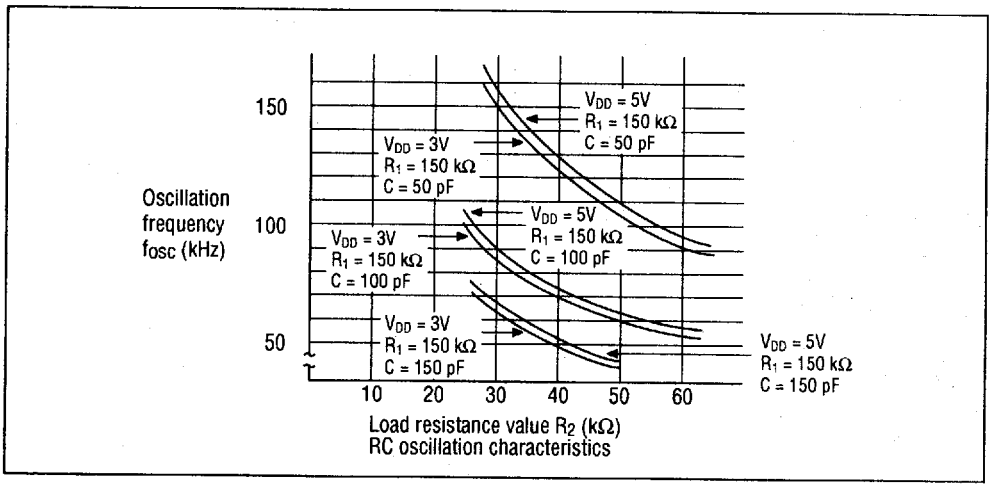


Figure 12 RC Oscillation Frequency

10. Crystal Oscillation

Figure 13 shows an external circuit using a crystal oscillator, KF-38S4-13PO102 (64 kHz), made by Kyocera.

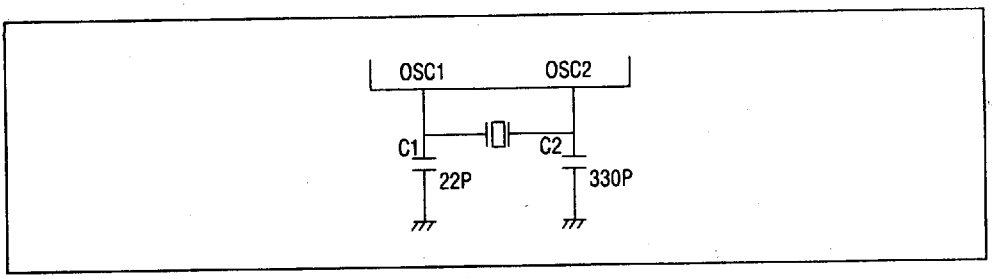


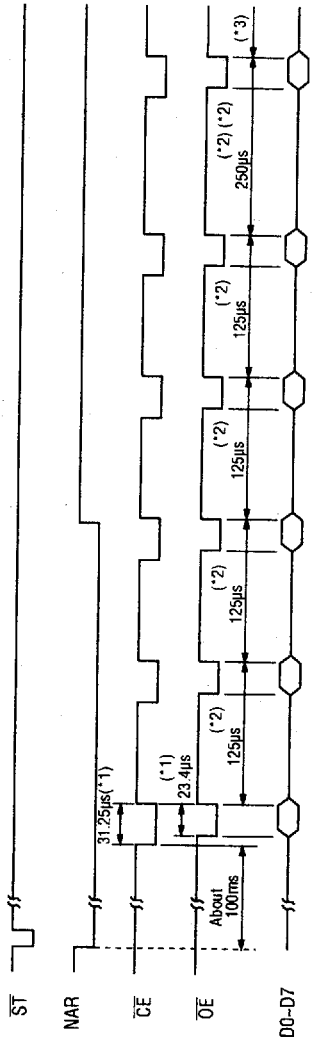
Figure 13 Circuit Diagram of Crystal Oscillator Connection

11. Connection with MSC 1191/1192

When using an MSC1191 and an MSC1192, connect the STBY pin to the OSC3/$\overline{CS}$ pin an the OSC2 pin, respectively. When connecting with an MSC1191/1192, set C and R after mounting it to the board as the oscillation characteristics may change.

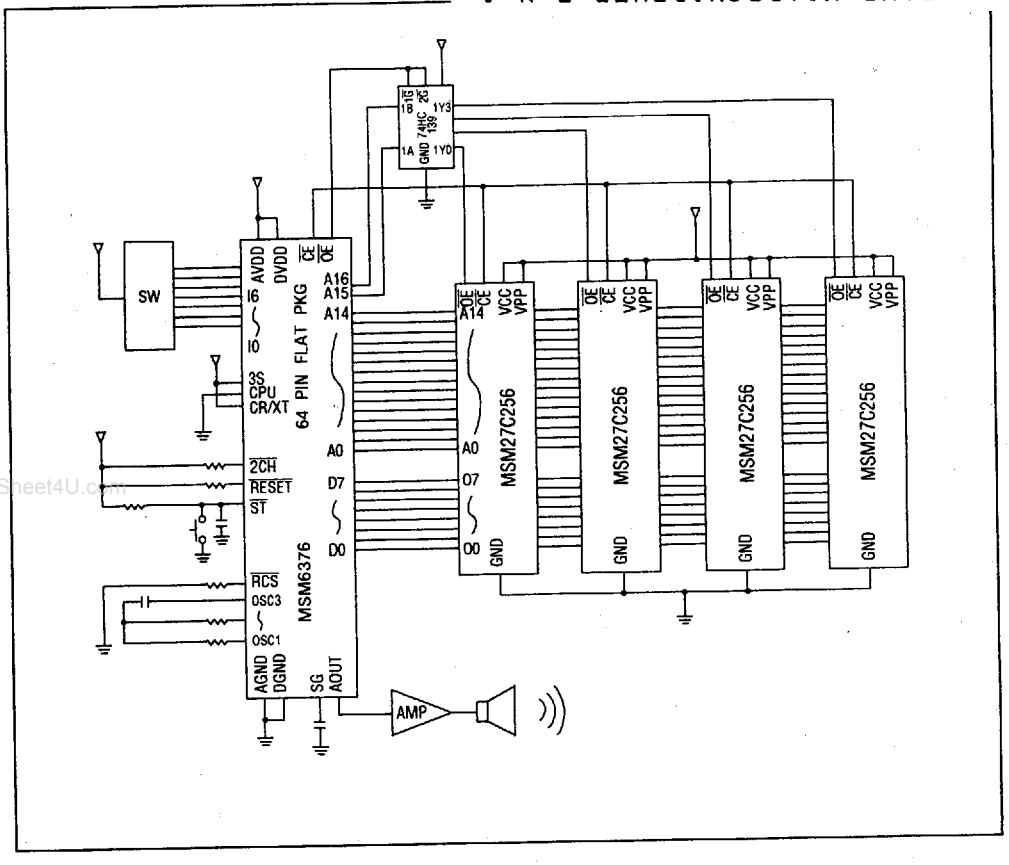
12. External ROM Timing

Figure 14 shows the external ROM driving timing under voice playback at f_{OSC} = 64kHz and f_S = 8.0kHz.



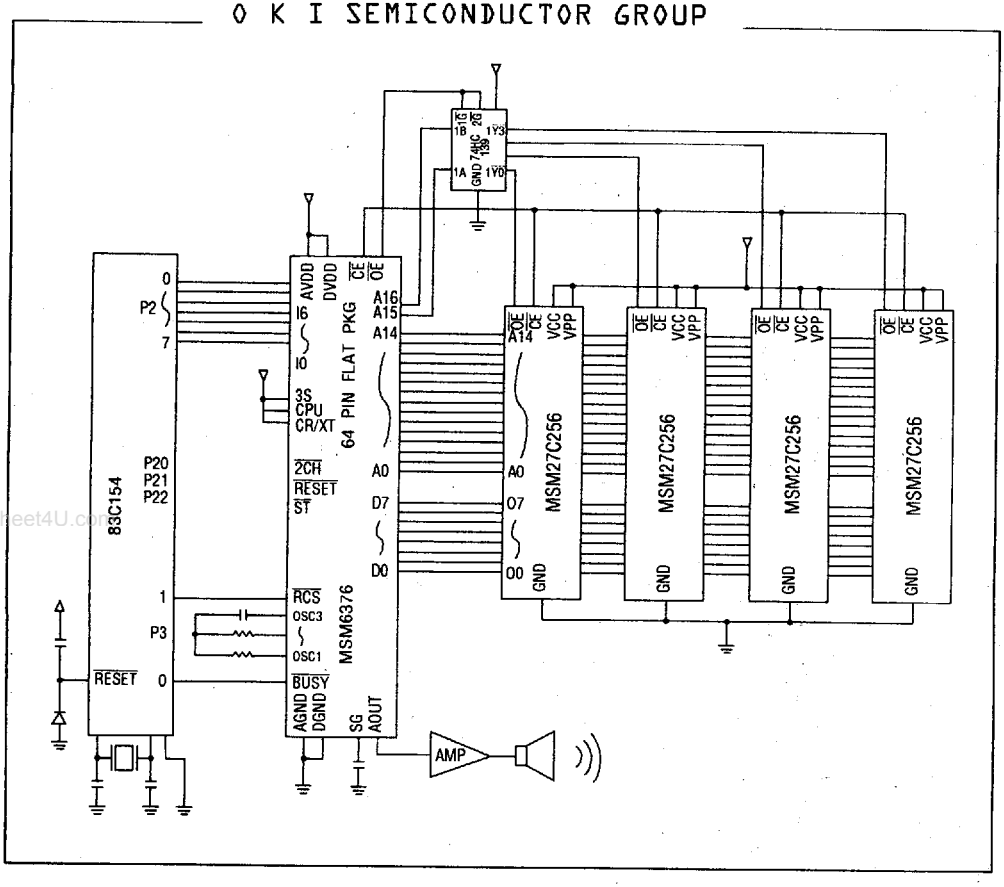
Note *1) This is proportional to f_{osc}
*2) This is proportional to f_S
*3) CE,OE and D0~D7 are input and output at the frequency of 250µs or 125µs hereafter.

Figure 14 External ROM Timing



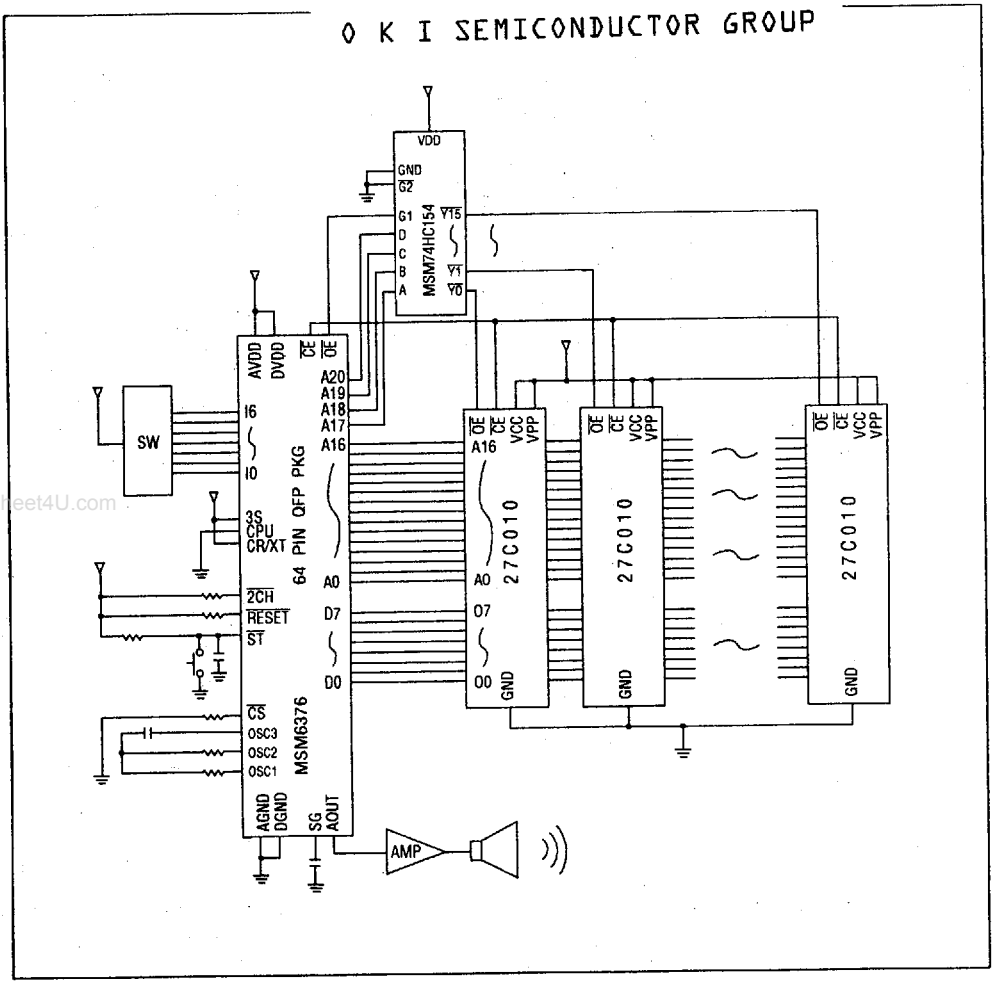
Note: Use a CMOS type 27C256 as an EPROM if possible. If an NMOS type 27256 is used, there are some cases where the power voltage variation of the EPROM becomes a source to generate noise.

Figure 15 Example of Interface Using Four 256K EPROMs



Note: Use a CMOS type 27C256 as an EPROM if possible. If an NMOS type 27256 is used, there are some cases where the power voltage variation of the EPROM becomes a source to generate noise.

Figure 16 Example of Applied CPU Interface Circuit



Note: Use a CMOS type 27C010 as an EPROM if possible. If an NMOS type EPPROM is used the power voltage variation of the EPROM becomes a source to generate noise.

Figure 17 Example of Interface Using 16-1Mbit EPROMs