



# PH3330L

## N-channel TrenchMOS logic level FET

Rev. 01 — 1 February 2006

Product data sheet

### 1. Product profile

#### 1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology.

#### 1.2 Features

- Optimized for use in DC-to-DC converters
- Logic level compatible
- Very low switching and conduction losses
- Lead-free package

#### 1.3 Applications

- DC-to-DC converters
- Voltage regulators
- Switched-mode power supplies
- Notebook computers

#### 1.4 Quick reference data

- $V_{DS} \leq 30\text{ V}$
- $R_{DS(on)} \leq 3.3\text{ m}\Omega$
- $I_D \leq 100\text{ A}$
- $Q_{GD} = 6.9\text{ nC (typ)}$

### 2. Pinning information

Table 1: Pinning

Pin	Description	Simplified outline	Symbol
1, 2, 3	source (S)		
4	gate (G)		
mb	mounting base; connected to drain (D)		

**SOT669 (LPAK)**

### 3. Ordering information

**Table 2: Ordering information**

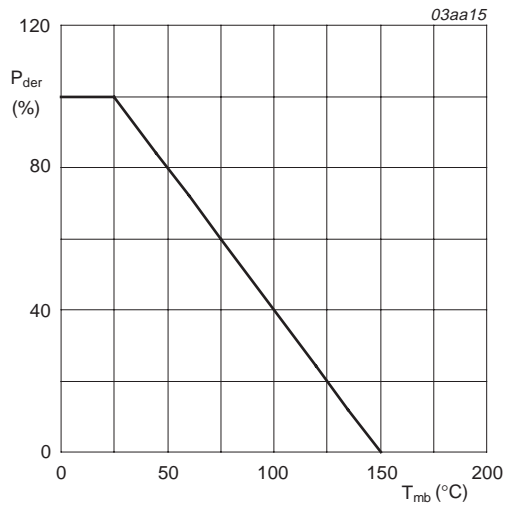
Type number	Package		Version
	Name	Description	
PH3330L	LFPAK	plastic single-ended surface mounted package (LFPAK); 4 leads	SOT669

### 4. Limiting values

**Table 3: Limiting values**

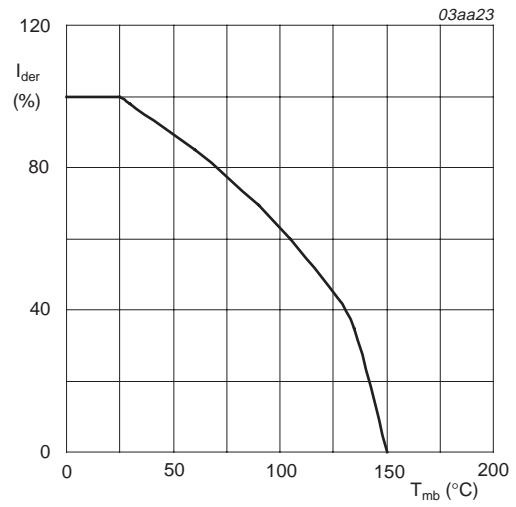
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	30	V
$V_{DGR}$	drain-gate voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$ ; $R_{GS} = 20\text{ k}\Omega$	-	30	V
$V_{GS}$	gate-source voltage		-	$\pm 20$	V
$I_D$	drain current	$T_{mb} = 25\text{ °C}$ ; $V_{GS} = 10\text{ V}$ ; see <a href="#">Figure 2</a> and <a href="#">3</a>	-	100	A
		$T_{mb} = 100\text{ °C}$ ; $V_{GS} = 10\text{ V}$ ; see <a href="#">Figure 2</a>	-	54.2	A
$I_{DM}$	peak drain current	$T_{mb} = 25\text{ °C}$ ; pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; see <a href="#">Figure 3</a>	-	300	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 1</a>	-	62.5	W
$T_{stg}$	storage temperature		-55	+150	°C
$T_j$	junction temperature		-55	+150	°C
<b>Source-drain diode</b>					
$I_S$	source current	$T_{mb} = 25\text{ °C}$	-	52	A
$I_{SM}$	peak source current	$T_{mb} = 25\text{ °C}$ ; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	208	A
<b>Avalanche ruggedness</b>					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; $I_D = 70\text{ A}$ ; $t_p = 0.15\text{ ms}$ ; $V_{DS} \leq 30\text{ V}$ ; $R_{GS} = 50\text{ }\Omega$ ; $V_{GS} = 10\text{ V}$ ; starting at $T_j = 25\text{ °C}$	-	245	mJ



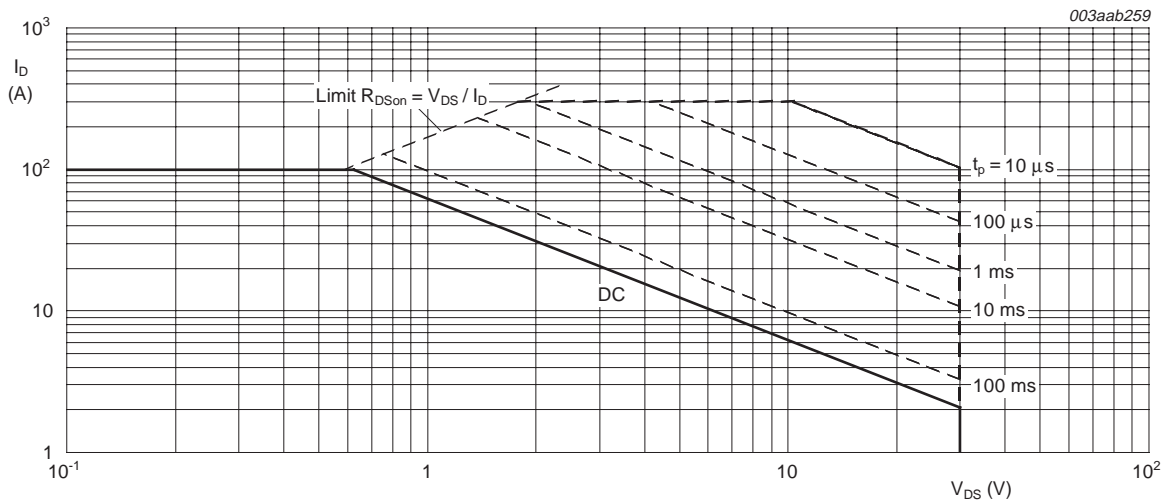
$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature



$$I_{der} = \frac{I_D}{I_{D(25^\circ C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature



$T_{mb} = 25^\circ C$ ;  $I_{DM}$  is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

## 5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see <a href="#">Figure 4</a>	-	-	2	K/W

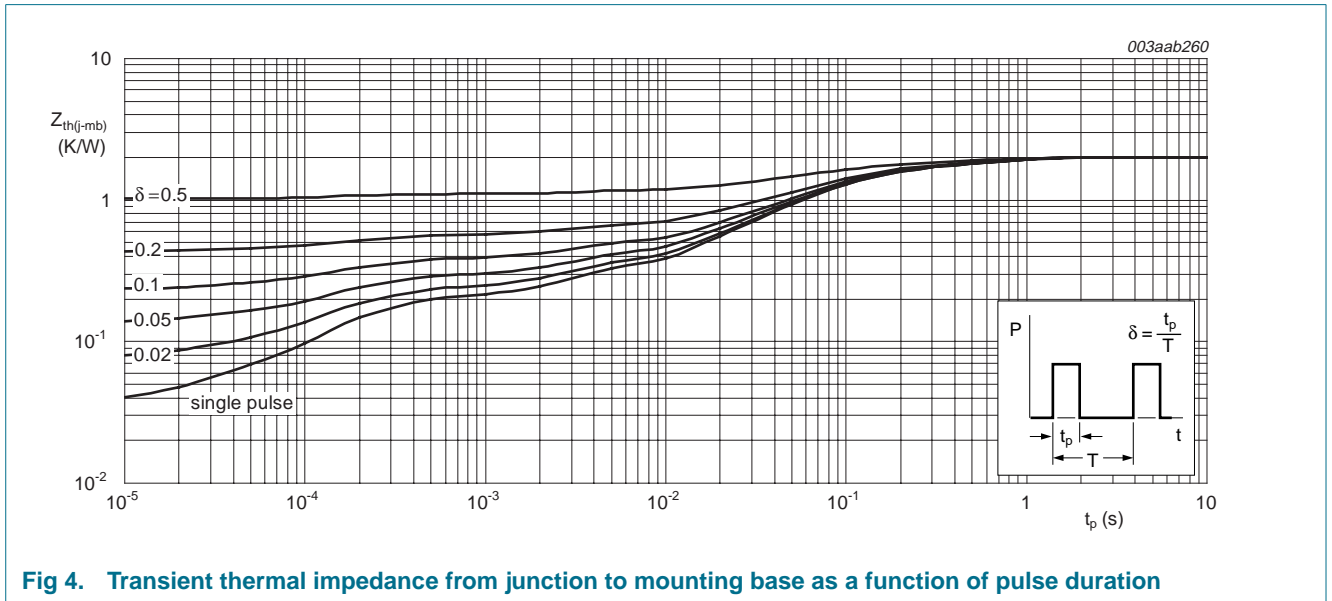
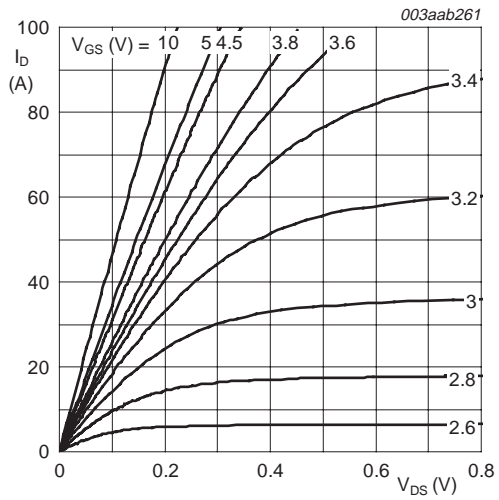


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

## 6. Characteristics

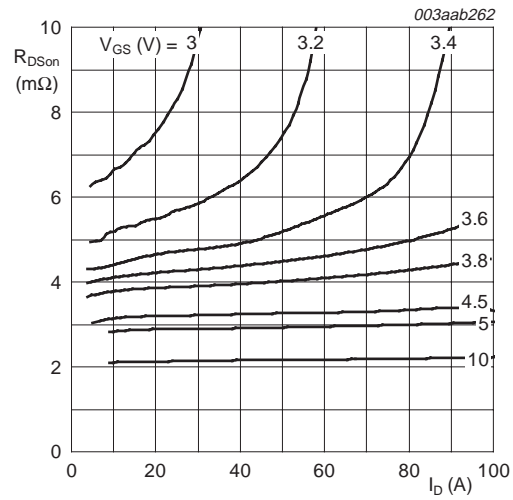
**Table 5: Characteristics**
*T<sub>j</sub> = 25 °C unless otherwise specified.*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
V <sub>(BR)DSS</sub>	drain-source breakdown voltage	I <sub>D</sub> = 250 μA; V <sub>GS</sub> = 0 V T <sub>j</sub> = 25 °C	30	-	-	V
		T <sub>j</sub> = -55 °C	27	-	-	V
V <sub>GS(th)</sub>	gate-source threshold voltage	I <sub>D</sub> = 1 mA; V <sub>DS</sub> = V <sub>GS</sub> ; see <a href="#">Figure 9</a> and <a href="#">10</a> T <sub>j</sub> = 25 °C	1.3	1.7	2.15	V
		T <sub>j</sub> = 150 °C	0.8	-	-	V
		T <sub>j</sub> = -55 °C	-	-	2.6	V
I <sub>DSS</sub>	drain leakage current	V <sub>DS</sub> = 30 V; V <sub>GS</sub> = 0 V T <sub>j</sub> = 25 °C	-	-	1	μA
		T <sub>j</sub> = 150 °C	-	-	100	μA
I <sub>GSS</sub>	gate leakage current	V <sub>GS</sub> = ±16 V; V <sub>DS</sub> = 0 V	-	-	100	nA
R <sub>G</sub>	gate resistance	f = 1 MHz	-	0.7	-	Ω
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; see <a href="#">Figure 6</a> and <a href="#">8</a> T <sub>j</sub> = 25 °C	-	2.3	3.3	mΩ
		T <sub>j</sub> = 150 °C	-	4.1	6	mΩ
		V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 25 A; see <a href="#">Figure 6</a> and <a href="#">8</a>	-	3.4	4.5	mΩ
<b>Dynamic characteristics</b>						
Q <sub>G(tot)</sub>	total gate charge	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 12 V; V <sub>GS</sub> = 4.5 V; see <a href="#">Figure 11</a> and <a href="#">12</a>	-	30.5	-	nC
Q <sub>GS</sub>	gate-source charge		-	15.4	-	nC
Q <sub>GS1</sub>	pre-V <sub>GS(th)</sub> gate-source charge		-	7.7	-	nC
Q <sub>GS2</sub>	post-V <sub>GS(th)</sub> gate-source charge		-	7.7	-	nC
Q <sub>GD</sub>	gate-drain charge		-	6.9	-	nC
V <sub>GS(pl)</sub>	gate-source plateau voltage		-	3.4	-	V
Q <sub>G(tot)</sub>	total gate charge	I <sub>D</sub> = 0 A; V <sub>DS</sub> = 0 V; V <sub>GS</sub> = 4.5 V	-	28.5	-	nC
C <sub>iss</sub>	input capacitance	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 12 V; f = 1 MHz; see <a href="#">Figure 14</a>	-	4840	-	pF
C <sub>oss</sub>	output capacitance		-	960	-	pF
C <sub>rss</sub>	reverse transfer capacitance		-	410	-	pF
C <sub>iss</sub>	input capacitance	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 0 V; f = 1 MHz	-	5380	-	pF
t <sub>d(on)</sub>	turn-on delay time	V <sub>DS</sub> = 12 V; R <sub>L</sub> = 0.5 Ω; V <sub>GS</sub> = 4.5 V; R <sub>G</sub> = 5.6 Ω	-	41	-	ns
t <sub>r</sub>	rise time		-	75	-	ns
t <sub>d(off)</sub>	turn-off delay time		-	52	-	ns
t <sub>f</sub>	fall time		-	27	-	ns
<b>Source-drain diode</b>						
V <sub>SD</sub>	source-drain voltage	I <sub>S</sub> = 25 A; V <sub>GS</sub> = 0 V; see <a href="#">Figure 13</a>	-	0.82	1.2	V
t <sub>rr</sub>	reverse recovery time	I <sub>S</sub> = 20 A; dI <sub>S</sub> /dt = -100 A/μs; V <sub>GS</sub> = 0 V	-	52	-	ns
Q <sub>r</sub>	recovered charge		-	23	-	nC



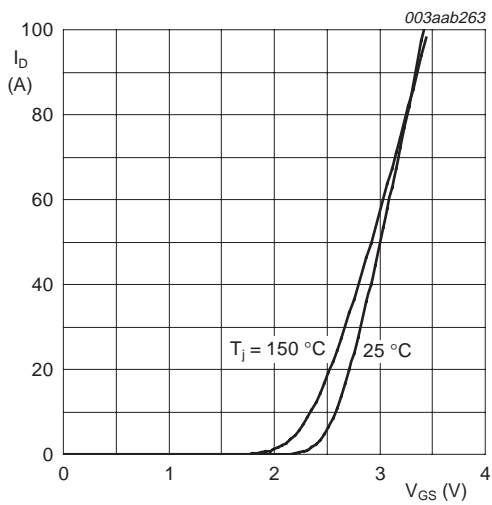
T<sub>j</sub> = 25 °C

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



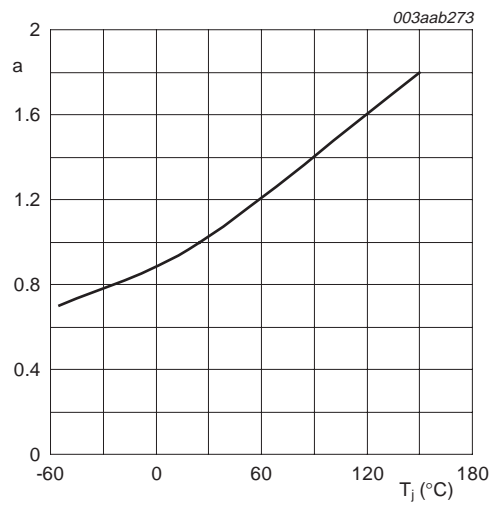
T<sub>j</sub> = 25 °C

Fig 6. Drain-source on-state resistance as a function of drain current; typical values



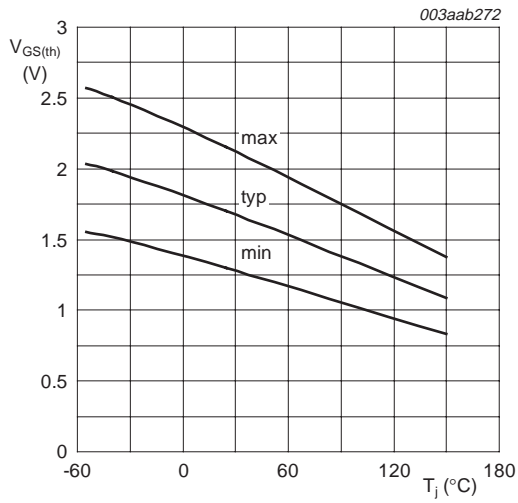
T<sub>j</sub> = 25 °C and 150 °C; V<sub>DS</sub> > I<sub>D</sub> × R<sub>DSon</sub>

Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values



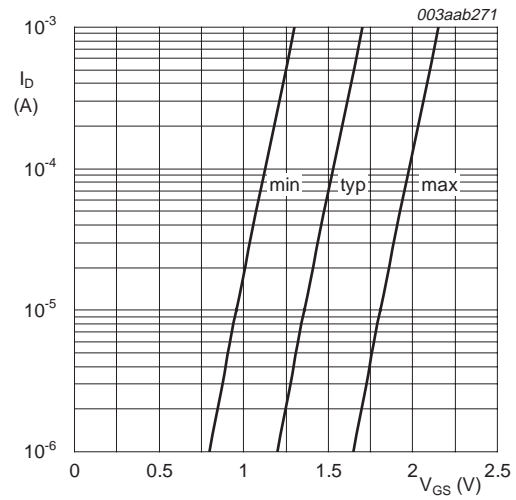
$$a = \frac{R_{DSon}}{R_{DSon(25\text{ }^\circ\text{C})}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature



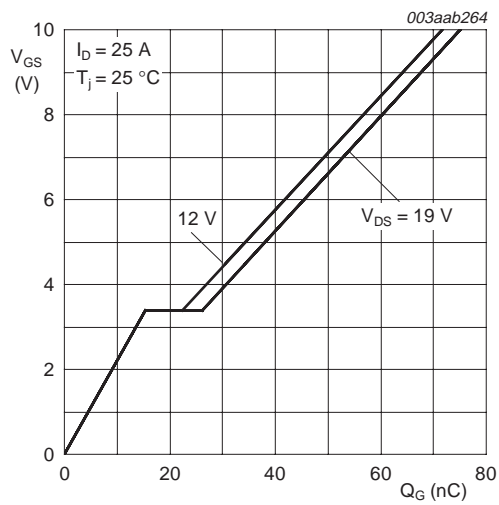
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature



$T_j = 25 \text{ }^{\circ}C; V_{DS} = 5 \text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage



$I_D = 25 \text{ A}; V_{DS} = 12 \text{ V and } 19 \text{ V}$

Fig 11. Gate-source voltage as a function of gate charge; typical values

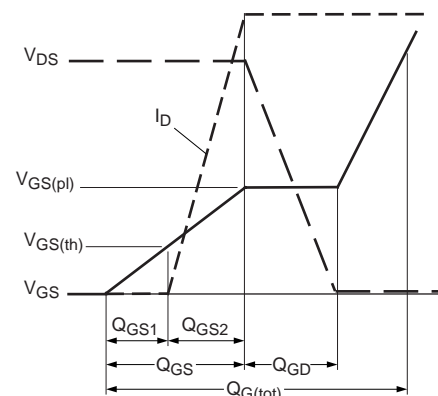
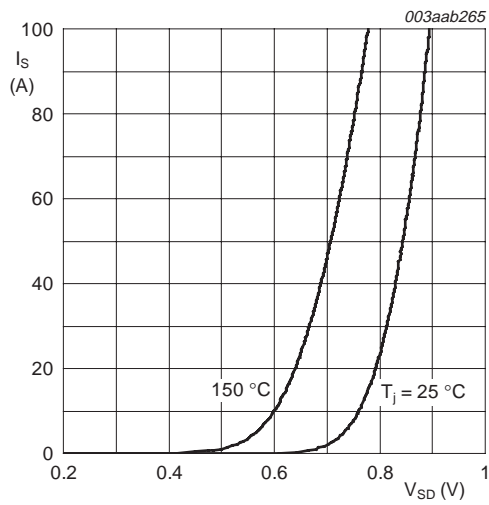
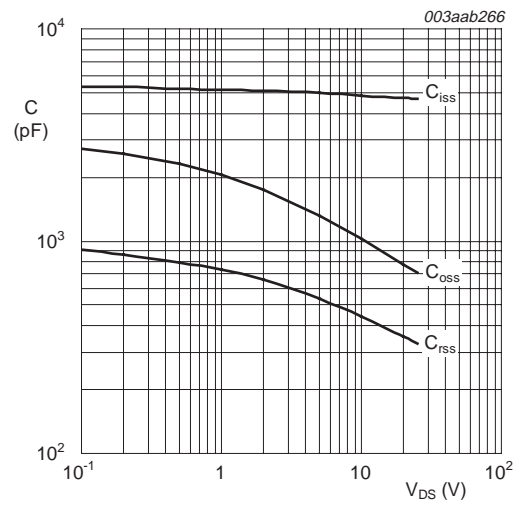


Fig 12. Gate charge waveform definitions



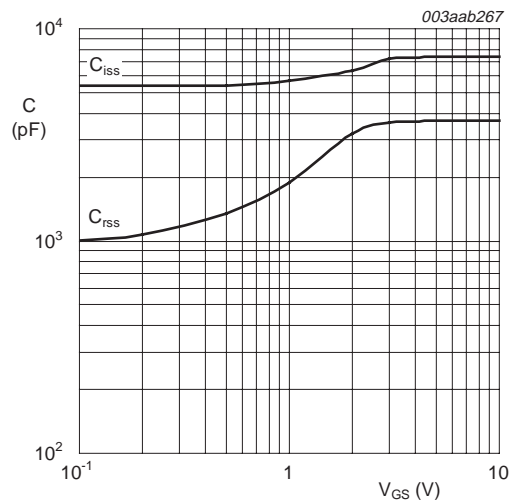
$T_j = 25\text{ }^\circ\text{C}$  and  $150\text{ }^\circ\text{C}$ ;  $V_{GS} = 0\text{ V}$

Fig 13. Source current as a function of source-drain voltage; typical values



$V_{GS} = 0\text{ V}$ ;  $f = 1\text{ MHz}$

Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{DS} = 0\text{ V}$ ;  $f = 1\text{ MHz}$

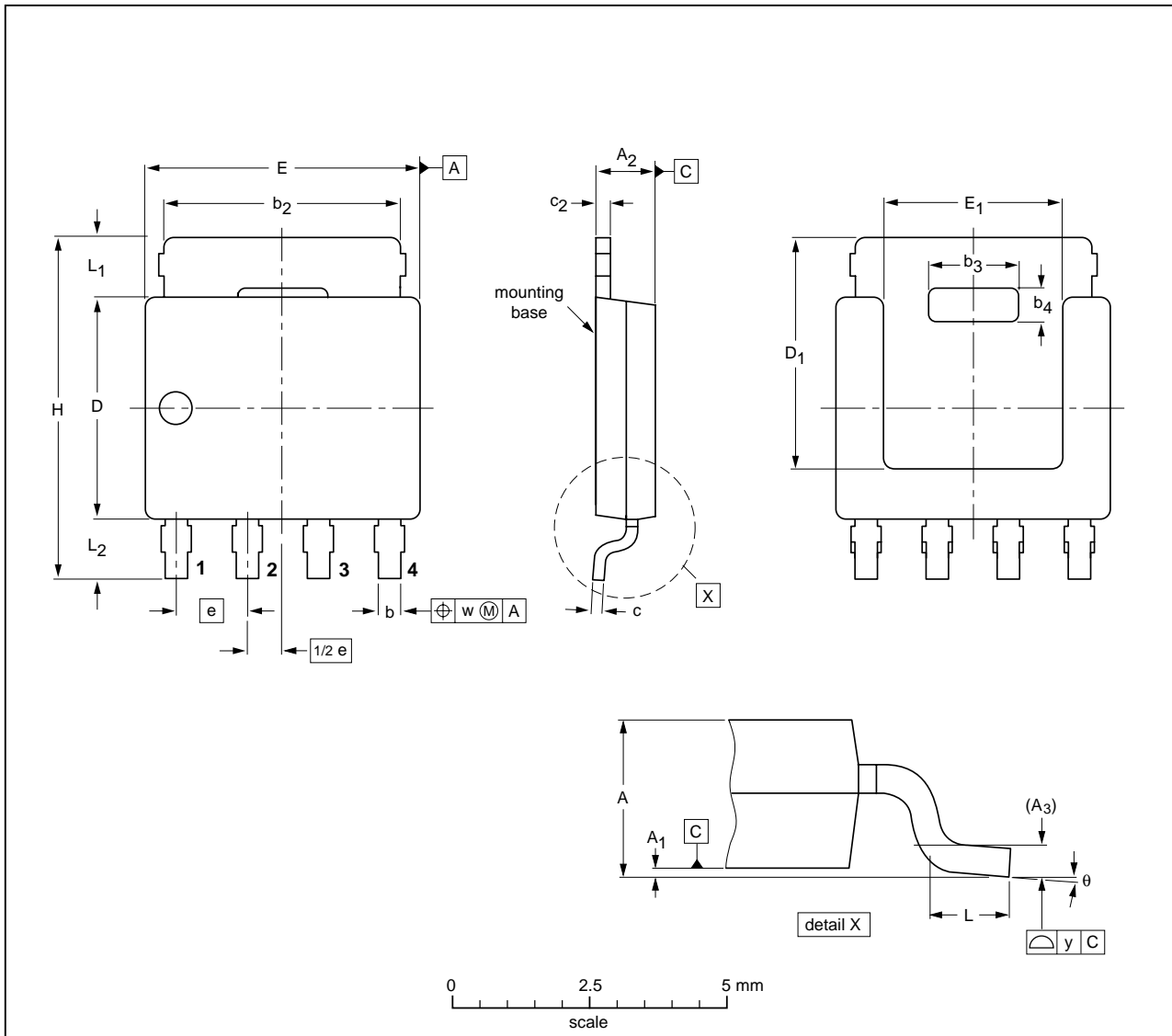
Fig 15. Input and reverse transfer capacitances as a function of gate-source voltage; typical values



7. Package outline

Plastic single-ended surface mounted package (LPAK); 4 leads

SOT669



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b	b <sub>2</sub>	b <sub>3</sub>	b <sub>4</sub>	c	c <sub>2</sub>	D <sup>(1)</sup>	D <sub>1</sub> <sup>(1)</sup> max	E <sup>(1)</sup>	E <sub>1</sub> <sup>(1)</sup>	e	H	L	L <sub>1</sub>	L <sub>2</sub>	w	y	θ
mm	1.20 1.01	0.15 0.00	1.10 0.95	0.25	0.50 0.35	4.41 3.62	2.2 2.0	0.9 0.7	0.25 0.19	0.30 0.24	4.10 3.80	4.20	5.0 4.8	3.3 3.1	1.27	6.2 5.8	0.85 0.40	1.3 0.8	1.3 0.8	0.25	0.1	8° 0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT669		MO-235				03-09-15 04-10-13

Fig 16. Package outline SOT669 (LPAK)

## 8. Revision history

Table 6: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
PH3330L_1	20060201	Product data sheet	-	-	-

## 9. Data sheet status

Level	Data sheet status <sup>[1]</sup>	Product status <sup>[2]</sup> <sup>[3]</sup>	Definition
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Date of release: 1 February 2006  
Document number: PH3330L\_1

Published in The Netherlands