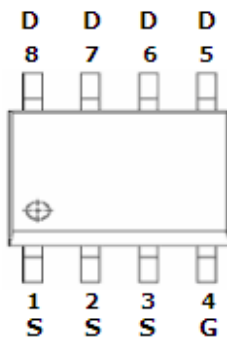
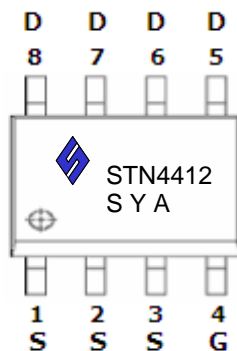
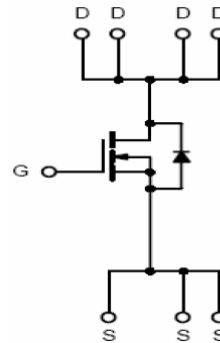


**DESCRIPTION**

STN4412 is the N-Channel logic enhancement mode power field effect transistor which is produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as power management and other battery powered circuits where high-side switching.

**PIN CONFIGURATION**
**SOP-8**

**PART MARKING**
**SOP-8**

**FEATURE**

- 30V/6.8A,  $R_{DS(ON)} = 28m\Omega$   
@ $V_{GS} = 10V$
- 30V/5.6A,  $R_{DS(ON)} = 36m\Omega$   
@ $V_{GS} = 4.5V$
- Super high density cell design for extremely low  $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOP-8 package design


**ORDERING INFORMATION**

Part Number	Package	Part Marking
STN4412S8RG	SOP-8P	STN4412
STN4412S8TG	SOP-8P	STN4412

※ Process Code : A ~ Z ; a ~ z

※ STN4412S8RG S8 : SOP-8 ; R : Tape Reel ; G : Pb - Free

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**STN4412** 

N Channel Enhancement Mode MOSFET

6.8A

※ STN4412S8TG S8 : SOP-8 ; T : Tube ; G : Pb – Free

**ABSOLUTE MAXIMUM RATINGS** (Ta = 25°C Unless otherwise noted )

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	VDSS	30	V
Gate-Source Voltage	VGSS	±20	V
Continuous Drain Current (TJ=150°C)	ID	TA=25°C 6.8	A
		TA=70°C 5.6	
Pulsed Drain Current	IDM	30	A
Continuous Source Current (Diode Conduction)	IS	2.3	A
Power Dissipation	PD	TA=25°C 2.8	W
		TA=70°C 1.6	
Operation Junction Temperature	TJ	150	°C
Storage Temperature Range	TSTG	-55/150	°C
Thermal Resistance-Junction to Ambient	RθJA	80	°C/W

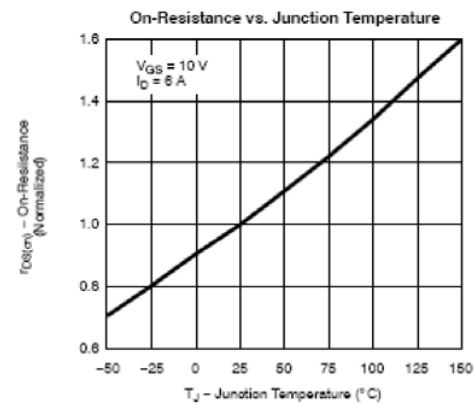
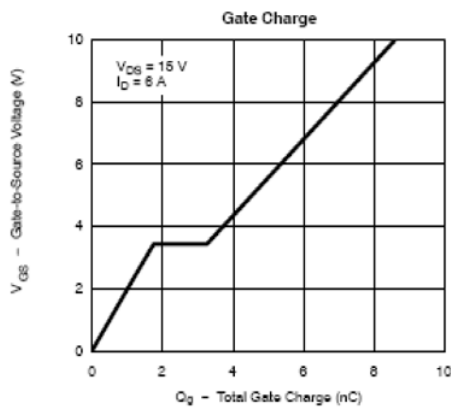
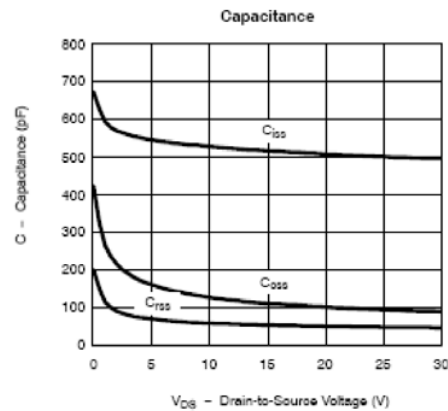
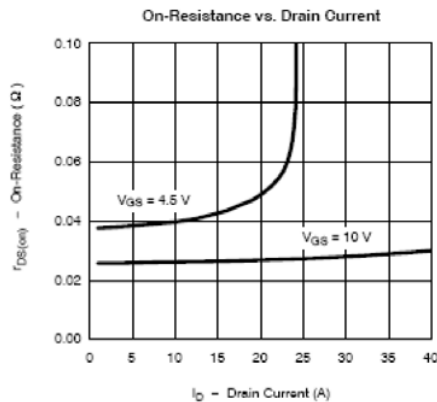
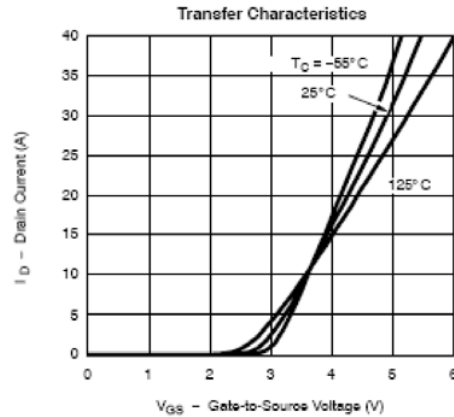
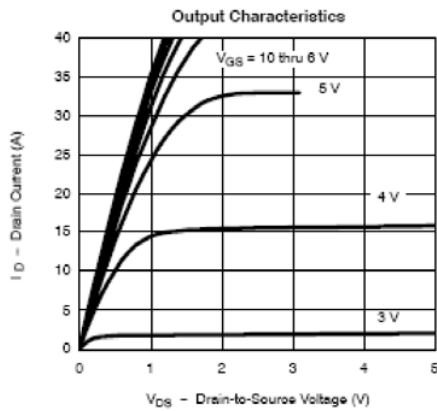
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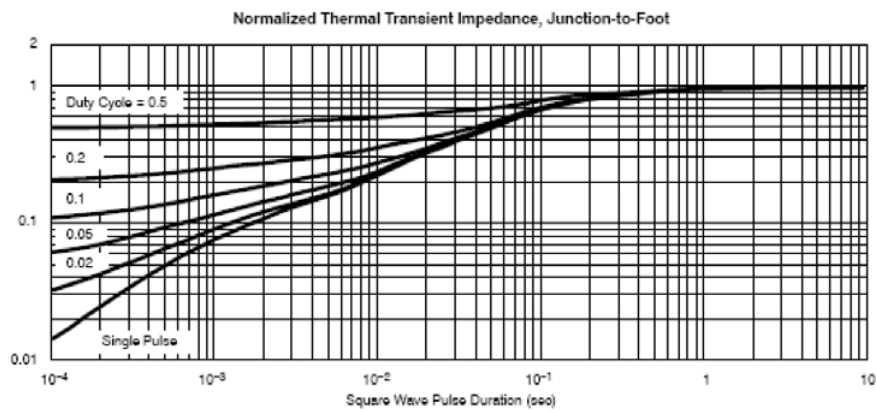
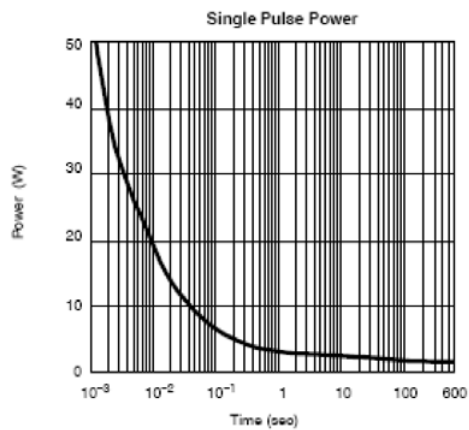
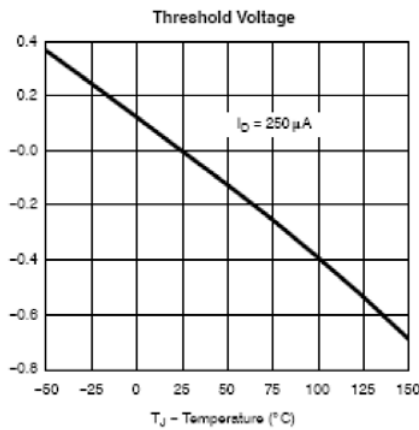
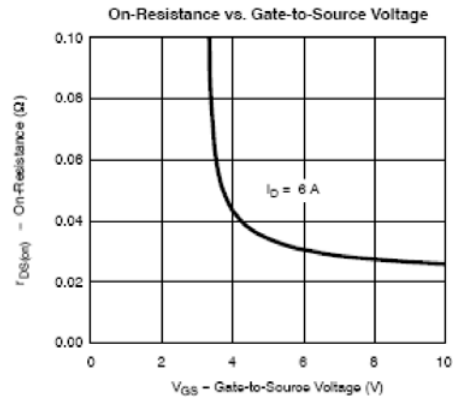
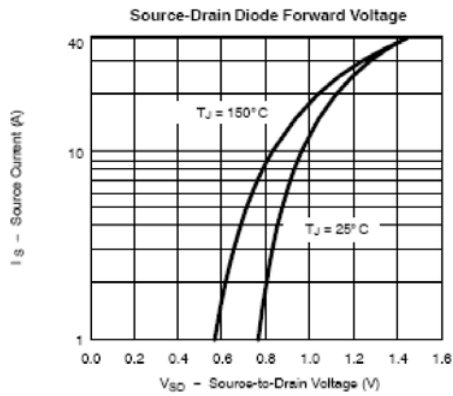
**ELECTRICAL CHARACTERISTICS** ( Ta = 25°C Unless otherwise noted )

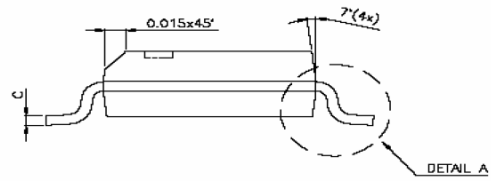
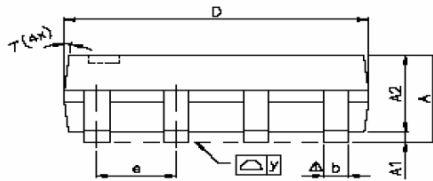
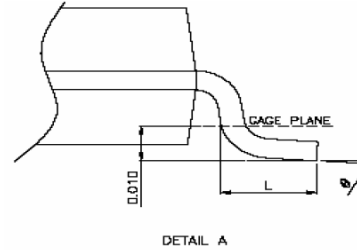
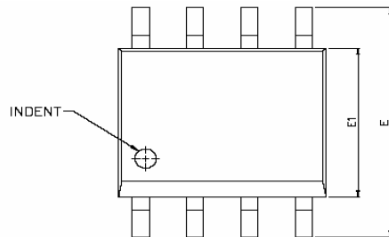
Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	30			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0		3.0	V
Gate Leakage Current	$I_{GSS}$	$V_{DS}=0V, V_{GS}=\pm 20V$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=24V, V_{GS}=0V$			1	uA
		$V_{DS}=24V, V_{GS}=0V$ $T_J=85^\circ C$			5	
On-State Drain Current	$I_{D(on)}$	$V_{DS} \geq 5V, V_{GS}=10V$	25			A
Drain-source On-Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=6.8A$ $V_{GS}=6.0V, I_D=5.6A$		22 30	28 36	mΩ
Forward Transconductance	$g_{fs}$	$V_{DS}=15V, I_D=6.2A$		13		S
Diode Forward Voltage	$V_{SD}$	$I_S=2.3A, V_{GS}=0V$		0.8	1.2	V
<b>Dynamic</b>						
Total Gate Charge	$Q_g$	$V_{DS}=15V, V_{GS}=10V$ $I_D=2A$		16	24	nC
Gate-Source Charge	$Q_{gs}$			3		
Gate-Drain Charge	$Q_{gd}$			2.5		
Input Capacitance	$C_{iss}$	$V_{DS} = 15V, V_{GS}=0V$ $F=1MHz$		450		pF
Output Capacitance	$C_{oss}$			240		
Reverse Transfer Capacitance	$C_{rss}$			38		
Turn-On Time	$t_{d(on)}$	$V_{DD}=15V, R_L=15\Omega$ $I_D=1A, V_{GEN}=-10V$ $R_G=6\Omega$		15	20	nS
	$t_r$			6	12	
Turn-Off Time	$t_{d(off)}$			10	20	
	$t_f$			40	80	

**TYPICAL CHARACTERISTICS**



**TYPICAL CHARACTERISTICS**



**PACKAGE OUTLINE SOP-8P**


SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.47	1.60	1.73	0.058	0.063	0.068
A1	0.10	—	0.25	0.004	—	0.010
A2	—	1.45	—	—	0.057	—
b	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.0098
D	4.80	4.85	4.95	0.189	0.191	0.195
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e	—	1.27	—	—	0.050	—
L	0.38	0.71	1.27	0.015	0.028	0.050
$\Delta$ y	—	—	0.076	—	—	0.003
$\theta$	0°	—	8°	0°	—	8°