CPC7220/CPC7221
Low Charge Injection 8-Channel High Voltage Analog Switch

Features
- Processed with BCDMOS on SOI (Silicon On Insulator)
- DC to 10MHz analog signal frequency
- Surface mount package available
- Low quiescent power dissipation (< 1µA typical)
- Output on-resistance typically 20Ω
- TTL I/O's for 3.3V interface
- Adjustable high voltage supplies

Applications
- Ultrasound imaging
- Printers
- Industrial controls and measurement

Description
The CPC7220 and CPC7221, with alternate pinout, are low charge injection 8-channel high-voltage analog switch integrated circuits (IC) for use in applications requiring high voltage switching. Control of the high voltage switching is via low voltage TTL logic level compatible inputs for direct connectivity to the system controller.

Switch manipulation is managed by an 8-bit serial to parallel shift register whose outputs are buffered and stored by an 8-bit transparent latch. Level shifters buffer the latch outputs and operate the high voltage switches.

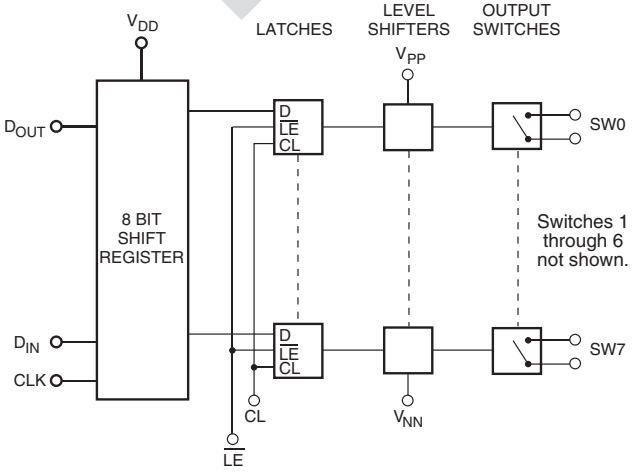
Because the CPC7220 and CPC7221 are capable of switching large load voltages and have a flexible load voltage range, e.g. V_{PP}/V_{NN} : +40V/-160V or +100V/-100V, they are well suited for many medical and industrial applications such as medical ultrasound imaging, printers and industrial measurement equipment.

Construction of the high voltage switches using Clare's reliable BCDMOS process technology on SOI (Silicon On Insulator) allow the switches to be organized as solid state switches with direct gate drive.

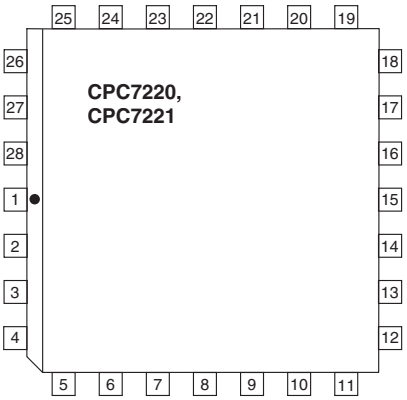
Ordering Information

Part Number	Description
CPC7220W	28-Pin PLCC
CPC7221W	28-Pin PLCC, Alternate pin out

Block Diagram



Package Pinout



top view

28-pin J-Lead Package

Pinout

CPC7220	CPC7221	Name	Description
1	1	SW3	SW3 output
2	2	SW3	SW3 output
3	3	SW2	SW2 output
4	4	SW2	SW2 output
5	5	SW1	SW1 output
6	6	SW1	SW1 output
7	7	SW0	SW0 output
8	8	SW0	SW0 output
10	9	V_{PP}	Switch positive high voltage supply
12	10	V_{NN}	Switch negative high voltage supply
13	12	GND	Ground
14	13	V_{DD}	Logic positive voltage supply
16	16	D_{IN}	Serial data input, LSB input first
17	17	CLK	Clock input, positive edge trigger
18	18	$\overline{LE}$	Latch enable, active low
19	19	CL	Latch clear, active high clears latches and opens switches
20	20	D_{OUT}	Serial data output, LSB output first
21	21	SW7	SW7 output
22	22	SW7	SW7 output
23	23	SW6	SW6 output
24	24	SW6	SW6 output
25	25	SW5	SW5 output
26	26	SW5	SW5 output
27	27	SW4	SW4 output
28	28	SW4	SW4 output
9, 11, 15	11, 14, 15	N/C	No Connects

Absolute Maximum Ratings (@ 25˚ C)

Parameter	Ratings	Units
V_{DD} logic power supply voltage	-0.5 to +6	V
V_{PP} - V_{NN} supply voltage	220	V
V_{PP} positive high voltage supply	-0.5 to V_{NN} +200	V
V_{NN} negative high voltage supply	+0.5 to V_{PP} -200	V
Logic input voltages	-0.5 to V_{DD} +0.3	V
Analog signal range	V_{NN} to V_{PP}	-
Peak analog signal current/channel	1	A
Power dissipation	1.2	W
Storage Temperature	-60 to +150	°C

Absolute Maximum Ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at conditions beyond those indicated in the operational sections of this data sheet is not implied.

Operating Conditions

Parameter	Symbol	Value
Logic power supply voltage [1,3]	V_{DD}	4.5V to 6V
Positive high voltage supply [1,3]	V_{PP}	40V to V_{NN} + 200V
Negative high voltage supply [1,3]	V_{NN}	-40V to -160V
Analog signal voltage peak to peak [2]	V_{SIG}	V_{NN} + 10V to V_{PP} -10V
Operating temperature	T_A	0ºC to 70ºC

NOTES:

1 Power up/down sequence is arbitrary except GND must be powered-up first and powered-down last.
2 V_{SIG} must be $V_{NN} \leq V_{SIG} \leq V_{PP}$ or floating durring power up/down transistion.
3 Rise and fall times of power supplies V_{DD}, V_{PP}, and V_{NN} should not be less than 1msec.

Electrical Characteristcs

DC Characteristics (over recommended operating conditions unless otherwise noted)

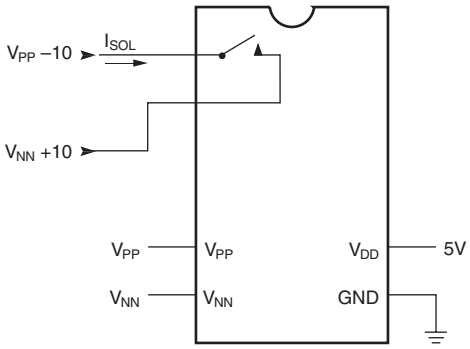
Parameter	Symbol	Test Conditions		0ºC		+25ºC			+70ºC		Units
				min	max	min	typ	max	min	max	
Small Signal Switch On-resistance	R_{ONS}	V_{PP} = 40V, V_{NN} = -160V	I_{SIG} = 5mA	-	30	-	26	38	-	48	Ω
			I_{SIG} = 200mA	-	25	-	22	27	-	32	
		V_{PP} = 100V, V_{NN} = -100V	I_{SIG} = 5mA	-	25	-	22	27	-	30	
			I_{SIG} = 200mA	-	18	-	18	24	-	27	
		V_{PP} = 160V, V_{NN} = -40V	I_{SIG} = 5mA	-	23	-	20	25	-	30	
			I_{SIG} = 200mA	-	22	-	16	25	-	27	
Small Signal Switch On-resistance Matching	ΔR_{ONS}	I_{SW} = 5mA, V_{PP} = 100V, V_{NN} = -100V		-	10	-	5	10	-	10	%
Large Signal Switch On-resistance	R_{ONL}	V_{SIG} = V_{PP} - 10V, I_{SIG} = 0.8A		-	-	-	15	-	-	-	Ω
Switch Off Leakage Per Switch	I_{SOL}	V_{SIG} = V_{PP} - 10V and V_{NN} + 10V		-	5	-	0.4	10	-	15	µA
DC Offset Switch Off	-	R_L = 100KΩ		-	100	-	0	100	-	100	mV
DC Offset Switch On	-	R_L = 100KΩ		-	100	-	0	100	-	100	mV
V_{PP} Quiescent Supply Current	I_{PPQ}	ALL SWs OFF		-	-	-	0.1	10	-	-	µA
		ALL SWs ON I_{SW} = 5mA									
V_{NN} Quiescent Supply Current	I_{NNQ}	ALL SWs OFF		-	-	-	-0.1	-10	-	-	µA
		ALL SWs ON I_{SW} = 5mA									
Switch Output Peak Current	-	V_{SIG} duty cycle ≤ 0.1%		-	-	-	-	0.8	-	-	A
Output Switch Frequency	f_{SW}	Duty Cycle = 50%		-	-	-	-	50	-	-	KHz
V_{PP} Operating Supply Current	I_{PP}	V_{PP} = 40V, V_{NN} = -160V	50KHz Output Switching Frequency with no load	-	6.5	-	-	7	-	8	mA
		V_{PP} = 100V, V_{NN} = -100V		-	5	-	-	5.5	-	5.5	
V_{NN} Operating Supply Current	I_{NN}	V_{PP} = 160V, V_{NN} = -40V		-	5	-	-	5	-	5.5	
V_{DD} Average Supply Current	I_{DD}	f_{CLK} = 5MHz, V_{DD} = 5V		-	4	-	-	4	-	4	mA
V_{DD} Quiescent Supply Current	I_{DDQ}	-		-	10	-	1	10	-	10	µA
D_{OUT} Source Capability	V_{OH}	I_{OUT} = -400µA		-	-	-	-	V_{DD} -0.7	-	-	V
D_{OUT} Sink Capability	V_{OL}	I_{OUT} = +400µA		-	-	-	-	0.7	-	-	V
Logic Input Capacitance	C_{IN}			-	10	-	-	10	-	10	pF
Logic Input High	V_{IH}	4.75V < V_{DD} < 5.25V		2	-	2	-	-	2	-	V
Logic Input Low	V_{IL}	4.75V < V_{DD} < 5.25V		-	0.8	-	-	0.8	-	0.8	V

Electrical Characteristcs

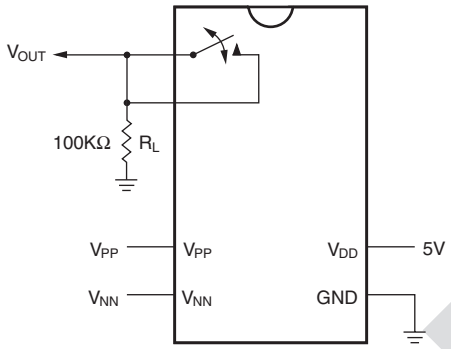
AC Characteristics (over recommended operating conditions unless otherwise noted)

Parameter	Symbol	Test Conditions	0ºC		+25ºC			+70ºC		Units
			min	max	min	typ	max	min	max	
Set Up Time before $\overline{LE}$ rises	t_{SD}		150	-	150	-	-	150	-	ns
Time Width of $\overline{LE}$	t_{WLE}		150	-	150	-	-	150	-	ns
Clock Delay time to Data Out	t_{DO}		-	150	-	-	150	-	150	ns
Time Width of CL	t_{WCL}		150	-	150	-	-	150	-	ns
Set Up Time Data to Clock	t_{SU}		15	-	15	8	-	20	-	ns
Hold Time Data from Clock	t_H		35	-	35	-	-	35	-	ns
Clock Freq	f_{CLK}	50% duty cycle $f_{DATA} = f_{CLK}/2$	-	5	-	-	5	-	5	MHz
Clock Rise and Fall Times	t_r, t_f		-	50	-	-	50	-	50	ns
Turn On Time	t_{ON}	$V_{SIG} = V_{PP}$ -10V, R_L = 10KΩ	-	5	-	-	5	-	5	µs
Turn Off Time	t_{OFF}									
Maximum V_{SIG} Slew Rate	dv/dt	V_{PP} = 160V, V_{NN} = -40V	-	20	-	-	20	-	20	V/ns
		V_{PP} = 100V, V_{NN} = -100V								
		V_{PP} = 40V, V_{NN} = -160V								
Off Isolation	KO	f = 5MHz, 1KΩ/15pF load	-30	-	-30	-33	-	-30	-	dB
		f = 5MHz, 50Ω load	-50	-	-50	-	-	-50	-	
Switch Crosstalk	K_{CR}	f = 5MHz, 50Ω load	-60	-	-60	-	-	-60	-	dB
Off Capacitance SW to GND	$C_{SG(OFF)}$	0V, 1MHz	5	17	5	21	25	5	20	pF
On Capacitance SW to GND	$C_{SG(ON)}$	0V, 1MHz	25	40	20	30	40	25	50	pF
Output Voltage Spike	$+V_{SPK}$	V_{PP} = 40V, V_{NN} = -160V, R_L = 50Ω	-	-	-	-	150	-	-	mV
	$-V_{SPK}$									
	$+V_{SPK}$	V_{PP} = 100V, V_{NN} = -100V, R_L = 50Ω								
	$-V_{SPK}$									
	$+V_{SPK}$	V_{PP} = 160V, V_{NN} = -40V, R_L = 50Ω								
	$-V_{SPK}$									
Charge Injection	Q	V_{PP} = 100V, V_{NN} = -100V, V_{SIG} = 0V			-	880	-			pC

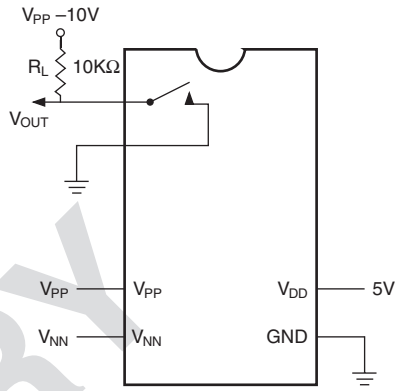
Test Circuits



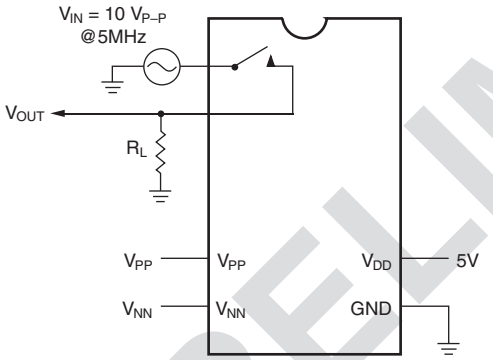
Switch OFF Leakage



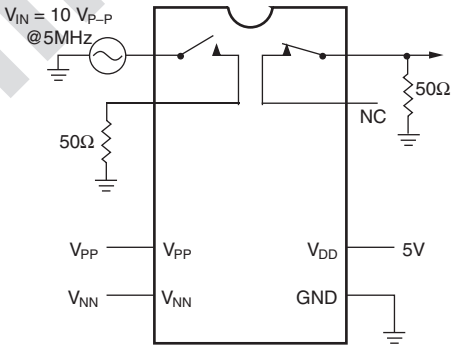
DC Offset ON/OFF



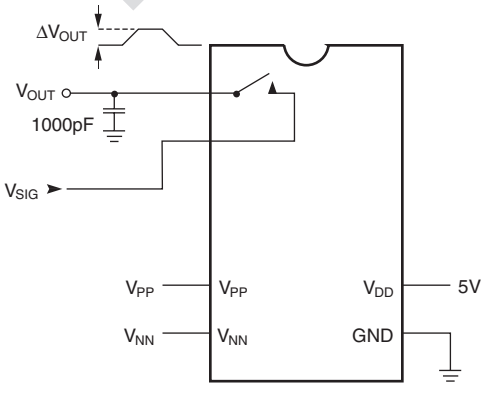
T_{ON}/T_{OFF} Test Circuit



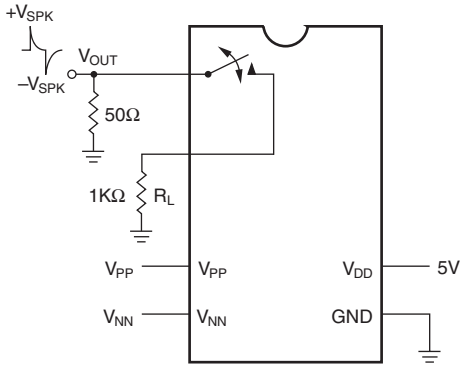
OFF Isolation



Crosstalk

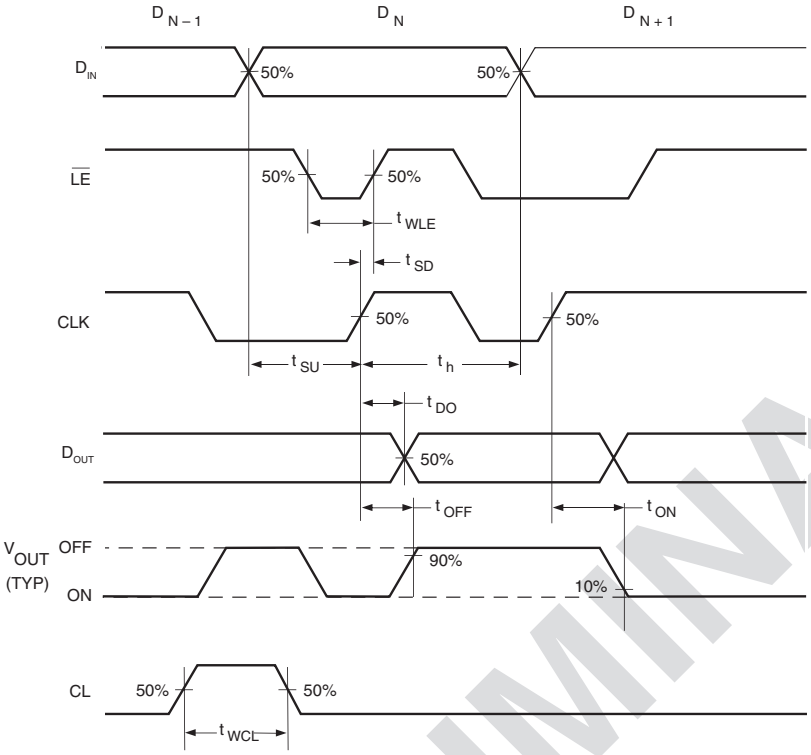


Charge Injection



Output Voltage Spike

Logic Timing Waveforms



Truth Table

D0	D1	D2	D3	D4	D5	D6	D7	$\overline{LE}$	CL	SW0	SW1	SW2	SW3	SW4	SW5	SW6	SW7
L								L	L	OFF							
H								L	L	ON							
	L							L	L		OFF						
	H							L	L		ON						
		L						L	L			OFF					
		H						L	L			ON					
			L					L	L				OFF				
			H					L	L				ON				
				L				L	L					OFF			
				H				L	L					ON			
					L			L	L						OFF		
					H			L	L						ON		
						L		L	L							OFF	
						H		L	L							ON	
							L	L	L								OFF
							H	L	L								ON
X	X	X	X	X	X	X	X	H	L	HOLD PREVIOUS STATE							
X	X	X	X	X	X	X	X	X	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF

Notes:

1. The eight switches operate independently.
2. Serial data is clocked in on the L→ H transition CLK.
3. The switches go to a state retaining their present condition at the rising edge of $\overline{LE}$. When $\overline{LE}$ is low the shift register data flows through the latch.
4. D_{OUT} is high when switch 7 is on.
5. Shift register clocking has no effect on the switch states if $\overline{LE}$ is H.
6. The clear input overrides all other inputs.

Manufacturing Information

Soldering
Recommended soldering processes are limited to 245ºC component body temperature for 10 seconds.

Washing
Clare does not recommend ultrasonic cleaning or the use of chlorinated solvents.

For additional information please visit our website at: www.clare.com

Specification: DS-CPC7220/CPC7221-R00B

5/10/05